

Optimization of Flexible Divider

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Abstract- In this paper an efficient multiband flexible divider for Bluetooth, Zigbee and other wireless standards is proposed based on pulse swallow topology and is implemented using Xilinx ISE 9.1i and modelsim SE10.0b. It consists of a proposed wideband multimodulus 32/33/47/48 prescaler, swallow s-counter, p-counter. As a modification I have implemented a modified multiband flexible divider by replacing nor gate by pass transistor in a wideband single phase PRESCALER clock 2/3 prescaler. Compared to the proposed system modified one will reduce the area, circuit complexity, power consumption, transistor counts.

Index Terms- DFF, dual modulus PRESCALER, E-TSPC, Frequency synthesizer, true single phase clock(TSPC), wireless LAN(WLAN).

I. INTRODUCTION

Now a day's people use a hardware module divider to implement the division algorithm. Conventionally synchronous techniques are applied to implement the divider. The synchronous systems always need system clock signals to trigger the system. However, the system clock of the synchronous system may cause some problems, such as clock skew, dynamic power consumption... etc. Compared to synchronous systems, asynchronous circuits do not need system clock signals and thus the asynchronous system does not have the shortcomings mentioned above. Wireless communication has received increasing interest for military and commercial applications.

With numerous Wireless LAN (WLAN) standards operating in different frequency bands, market leading WLAN solutions must offer multi-mode interoperability with transparent worldwide usage. The demands for fast switching and high operating frequencies make the design of frequency synthesizers a challenging task. The synthesizer can be an integer-N type with programmable Integer frequency dividers or Fractional-N type synthesizer. The wireless communication market has been expanding, resulting in increasingly stringent requirements for low cost, low power consumption, higher operating frequencies and miniaturization on circuits due to limited battery life and highly competitive market environment. Gallium Arsenide

(GaAs) technology was used in the early 80's for implementation of circuits operating in the GHz bands. However, silicon wafers are still preferred for its lower manufacturing cost, and improved unity gain bandwidth over the years via device scaling, new materials for interconnection and additional metal layers. The IEEE 802.11a Wireless local area network (WLAN) is allocated 300-MHz bandwidth at 5 GHz, which can support a data throughput of 54 Mb/s or higher. The lower 20MHz(5.15– 5.35 GHz) is shared with the European high-performance radio LAN band. The upper 100 MHz (5.725–5.825 GHz) falls in the industrial, scientific, and medical band.

However, for multi-standard applications, it is often difficult to cover multiple frequency bands using an integer frequency synthesizer whose step size is limited by the reference frequency. Frequency dividers (FDs) also called prescaler are used in many communications applications such as frequency synthesizers, timing-recovery circuits and clock generation circuits. The prescaler is employed in the feedback path of the synthesizer, takes a periodic signal and generate a periodic output signal whose frequency is a fraction of the input frequency. The prescaler is one of the most critical block in the frequency synthesizer since it operates at the highest frequency and consumes large power. Thus the power reduction in the first stage of the prescaler is important in realizing a low power.

II. BLOCK DIAGRAM

The key parameters of high-speed digital circuits are the propagation delay and power consumption. The maximum operating frequency of a digital circuit is calculated by the method described in [11] and is given by in "Eq.1"

$$F_{max} = \frac{1}{(t_{pLH} + t_{pHL})} \quad (1)$$

where t_{pLH} and t_{pHL} are the propagation delays of the low-to-high and high-to-low transitions of the gates, respectively. The total power consumption of the CMOS digital circuits is determined by the switching and short circuit power. The switching power is linearly proportional to the operating frequency and is given by the sum of switching power at each output node as in "Eq.2"

$$P_{switching} = \sum_{j=1}^n F_{clk} C_{Li} V_{dd}^2 \tag{2}$$

where n is the number of switching nodes, F_{clk} is the clock frequency, $C_{Li}V^2$ is the load capacitance at the output node of the stage, and V_{dd}^2 is the supply voltage. Normally, the short-circuit power occurs in dynamic circuits when there exists direct paths from the supply to ground which is given by "Eq.3"

$$P_{sc} = I_{sc} * V_{dd} \tag{3}$$

where I_{sc} is the short-circuit current. The analysis in [12] shows that the short-circuit power is much higher in E-TSPC logic circuits than in TSPC logic circuits. However, TSPC logic circuits exhibit higher switching power compared to that of E-TSPC logic circuits due to high load capacitance. For the E-TSPC logic circuit, the short-circuit power is the major problem. The E-TSPC circuit has the merit of higher operating frequency than that of the TSPC circuit due to the reduction in load capacitance, but it consumes significantly more power than the TSPC circuit does for a given transistor size. The following analysis shown in figure 1 is based on the latest design using the popular and low-cost 0.18- m CMOS process.

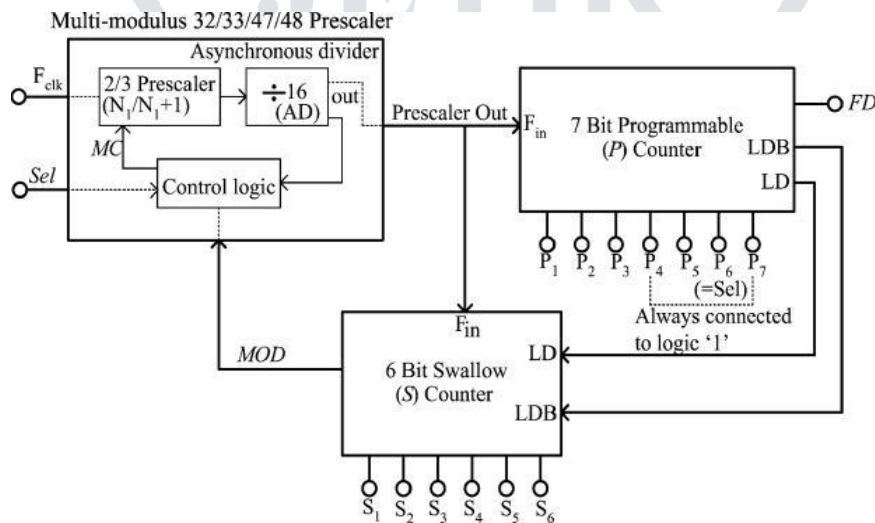


Figure 1 Pre-Scaler

III. WIDEBAND ETSPC 2/3 PRESCALER

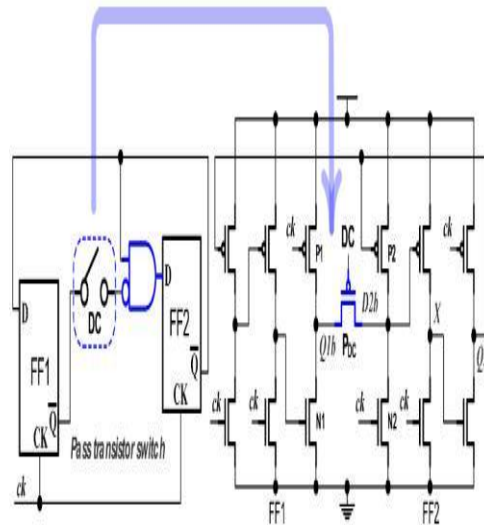


Figure 2 Wideband single-phase clock 2/3 prescaler

A state-of-the-art divide-by-2/3 counter design is given in Fig. 2(a) [7]. It contains two E-TSPC-based FFs and two logic gates i.e., an OR gate and an AND gate. When the divide control signal DC is “0”, the OR gate (merged into output of FF1 design) is disabled. The state of (Q1b , Q2b) cycles through 11, 01, and 00. This corresponds to a divide-by-3 function. Note that state 10 is a forbidden state. If, somehow, the circuit enters this state, the next state will go back to a valid state, 11, automatically. When DC is “1”, the output of FF1 will be disabled and FF2 alone performs the divide-by-2 function. Since the input to FF1 is not disabled, FF1 toggles as usual and causes redundant power consumption in the divide-by-2 mode operation. To overcome this problem, another divide-by-2/3 counter design presented in [8] is shown in Fig. 1(b). By pushing the divide control logic from the output of FF1 to its input, the output of the first stage in FF1 is frozen when DC(inverse) = 0’.

This refrains the following stages from any switching activities for the purpose of power saving. The first stage itself, however, encounters larger power consumption than its counter- part in design [7]. This is because the pull up path is turned on all the time and the short circuit current is drawn repetitively whenever the clock signal turns “1”. The critical path delay, formed by the two FFs and the control logic, is the dominant factor of the prescaler’s maximum operating frequency. In spite of the circuit simplicity in designs [7] and [8], the inverter between FF1 and FF2, which is essential to the logic of divide-by-3, causes extra delay. Merging control logic with FF designs also introduces parallel connected transistors leading to larger parasitic capacitance adverse to both speed and power consumption. In view of these issues, our approach is keeping the circuit simplicity so that the delay and the power consumption problems can be improved at a time.

IV. MULTIMODULUS 32/33/47/48 PRESCALER

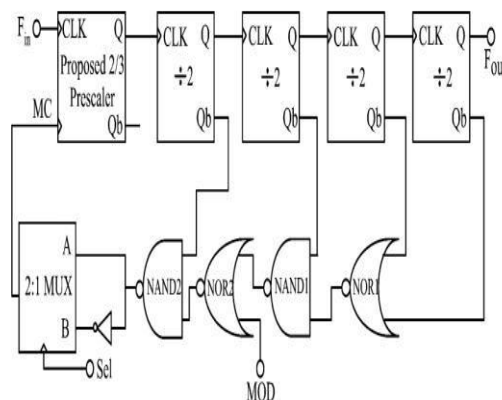


Figure 3 MultiModulus Prescaler

The proposed wideband multimodulus prescaler which can divide the input frequency by 32, 33, 47, and 48 is shown in Figure 2. It is similar to the 32/33 prescaler used in [7], but with an additional inverter and a multiplexer. The proposed prescaler additional divisions (divide-by-47 and divide-by-48) without any extra flip-flop, thus saving a considerable amount of power and also reducing the complexity of multiband divider. The multimodulus PRESCALER as shown in Figure 3 consists of the wideband $2/3(N_1/(N_1+1))$ PRESCALER, four asynchronous TSPC divide-by-2 circuits ((AD)=16) and combinational logic circuits to achieve multiple division ratios. Beside the usual mod signal for controlling divisions, the additional control signal Sel is used to switch the PRESCALER between 32/33 and 47/48 modes.

A. Case 1: Sel='0'

When sel='0', the output from the NAND2 gate is directly transferred to the input of $2/3$ prescaler and the multimodulus prescaler operates as the normal 32/33 prescaler, where the division ratio is controlled by the logic signal MOD. If MC=1 the $2/3$ prescaler operates in the divide-by-2 mode and when MC=0 the $2/3$ prescaler operates in the divide-by-3 mode. If MOD=1, the NAND2 gate output switches to logic "1" and the wideband prescaler operates in the divide-by-2 mode for entire operation. The division ratio N performed by the multimodulus prescaler is given in "Eq.4"

$$N = (AD * N_1) + (0 * (N_1 + 1)) = 32 \quad (4)$$

Where $N_1=2$ and $AD=16$ is fixed for the entire design. If MOD=0, for 30 input clock cycles MC remains at logic "1", where wideband PRESCALER operates in divide-by-2 mode and for three input clock cycles, MC remains at logic "0" where the wide band prescaler operates in the divide-by-3 mode. The division ratio N+1 performed by the multimodulus prescaler is given in "Eq.5"

$$N + 1 = ((AD - 1) * N_1) + (1 * (N_1 + 1)) = 33 \quad (5)$$

B. Case 2: Sel='1'

When Sel='1', the inverted output of the NAND2 gate is directly transferred to the input of $2/3$ prescaler and the multimodulus prescaler operates as 47/48 prescaler, where the division ratio is controlled by the logic signal MOD. If MC=1, the $2/3$ prescaler operates in divide-by-3 mode and when MC=0, the $2/3$ prescaler operates in divide by-2 mode which is quite opposite to the operation performed when Sel='0'. If

MOD=1, the division ratio N+1 performed by the multimodulus prescaler is same except that the wide-band prescaler operates in the divide-by-3 mode for the entire operation given by

$$N + 1 = (AD * (N_1 + 1)) + (0 * N_1) = 48 \quad (6)$$

If MOD=1, the division ratio N performed by the multimodulus prescaler is

$$N = ((AD - 1) * (N_1 + 1)) + (1 * N_1) = 47 \quad (7)$$

V. MULTIBAND FLEXIBLE DIVIDER

The single-phase clock multiband flexible divider consists of the multimodulus 32/33/47/48 prescaler, a 7-bit programmable P-counter and a 6-bit swallow S-counter. The control signal Sel decides whether the divider is operating in lower frequency band (2.4 GHz) or higher band (5-5.825 GHz).

1) A. SWALLOW (S) COUNTER

The 6-bit S-counter shown in Figure 4 consists of six asynchronous loadable bit-cells, a NOR-embedded DFF and additional logic gates to allow it to be programmable from 0 to 31 for low-frequency band and from 0 to 47 for the high-frequency band. The asynchronous bit-cell used in this design shown in Fig. is similar to the bit-cell reported in [13], except it uses two additional transistors M_6 and M_7 whose in-puts are controlled by the logic signal MOD. If MOD is logically high, nodes S1 and S2 switch to logic "0" and the bit-cell does not perform any function. The MOD signal goes logically high only when the S-counter finishes counting down to zero. If MOD and LD are logically low, the bit-cell acts as a divide-by-2 unit. If MOD is logically low and LD is logically high, the input bit PI is transferred to the output.

In the initial state, MOD=0, the multimodulus prescaler selects the divide-by-(N+1) mode (divide-by-33 or divide-by-48) and P, S counters start down counting the input clock cycles. When the S-counter finishes counting, MOD switches to logic "1" and the prescaler changes to the divide-by-N mode (divide-by-32 or divide-by-47) for the remaining (P - S) clock cycles. During this mode, since S-counter is idle, transistors M_6 and M_7 which are controlled by MOD, keep the nodes S1 and S2 at logic "0," thus saving the switching power in S-counter for a period of (N*(P - S)) clock cycles. Here, the Programmable Input (PI) is used to load the counter to a specified value from 0 to 31 for the lower band and 0 to 48 for the higher band of operation.

2) PROGRAMMABLE (P) COUNTER:

The programmable P -counter is a 7-bit asynchronous down counter which consists of 7 loadable bit-cells and additional logic gates. Here, bit is tied to the Sel signal of the multimodulus prescaler and bits and are always at logic “1.” The remaining bits can be externally programmed from 75 to 78 for the lower frequency band and from 105 to 122 for the upper frequency band. When the P -counter finishes counting down to zero, LD switches to logic “1” during which the output of all the bit-cells in S-counter switches to logic “1” and output of the NOR embedded DFF switches to logic “0” (MOD=0) where the programmable divider get reset to its initial state and thus a fixed division ratio is achieved. If a fixed 32/33 dual-modulus prescaler is used, a 7-bit P -counter is needed for the low-frequency band (2.4 GHz) while an 8- bit P -counter would be needed for the high-frequency band (5–5.825 GHz) with a fixed 5-bit s- counter. Thus, the multi modulus 32/33/47/48 prescaler eases the design complexity of the P – counter.

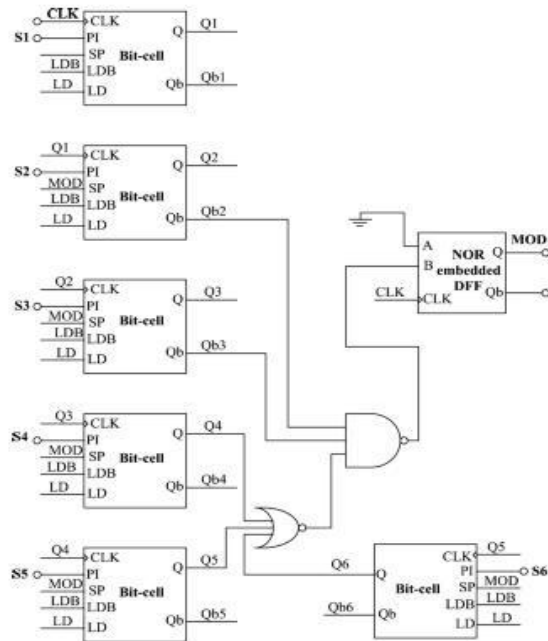


Figure 4 Asynchronous 6-bit S-Counter

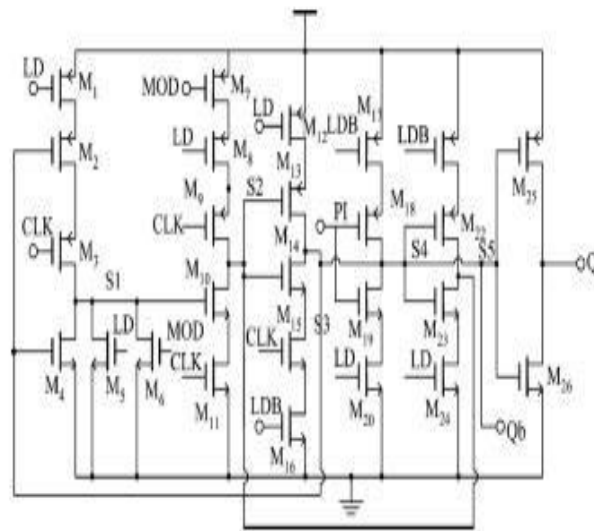


Figure 5 Bit Cell

1) Sel = 0 (2.4–2.484 GHz): When logic signal Sel=0 the multimodulus prescaler acts as a 32/33 prescaler, the P -counter is programmable from 64 to 127 (bit of the P -counter always remains at logic “1”), and the S-counter is programmable from 0 to 31 to accommodate division ratios from 2048 to 4095 with finest resolution of 1 MHz. However, since we are interested in the 2.4-GHz band, bit of the P -counter always remains at logic “0,” since it is tied to the logic signal Sel, allowing it to be programmable from 75 to 78. Bit of the S-counter is kept at logic ‘0’ (to satisfy the conditions $N>S$), allowing a programmable division from 0 to 31 for the low-frequency band of operation to accommodate division ratios between 2400 and 2484 with a resolution of 1 MHz for Bluetooth and Zigbee applications [7] and 5 MHz for the IEEE 802.15.4 frequency synthesizer [8] with a fixed reference frequency of 1 MHz. Since the finest resolution and reference frequency is 1 MHz, different channel spacings can be achieved by programming S-counter in steps of 1. For example, a 5-MHz channel spacing is achieved by programming S-counter in steps of “5” keeping the flexible divider resolution and reference frequency to 1 MHz. The Frequency Division(FD) ratio of the multiband divider in this mode is given as shown in Figure 5.

2) sel='1'(5–5.825 GHz): When logic signal,the multimodulus prescaler acts as a 47/48 ($N/N+1$) prescaler, the P-counter is programmable from 64 to 127 (bit of the P -counter always remains at logic “1”), and the S-counter is programmable from 0 to 48 to accommodate division ratios from 3024 to 6096 with finest resolution of 1 MHz. However, since we are interested in 5–5.825 GHz band, bit of the P -counter always remains at logic “1,” allowing it to be programmable from 105 to 122. The S-counter is programmable from 0 to 48 for the high frequency band of operation to accommodate division ratios between 5000 and 5825 with a resolution of 5 MHz, 10 MHz or 20 MHz for IEEE 802.11a/b/g synthesizers [1]–[3], [6], [9]. Since finest resolution and reference frequency is 1 MHz, S-counter is programmed in steps of ‘5’, ‘10’ or ‘20’, and P -counter programmed from 105 to 122 in steps of ‘1’ to provide channel spacing of 5 MHz, 10 MHz or 20 MHz. The frequency division (FD) ratio of the multiband divider in this mode is given by A dynamic logic multiband flexible integer-N divider is designed which uses the wideband 2/3 prescaler,multimodulus 32/33/47/48 prescaler.Since the multimodulus 32/33/47/48 prescaler has maximum operating frequency of 6.2 GHz,the values of P and S counters can actually be programmed to divide over the frequencies from 1 to 6.2 GHz.

VI. CONCLUSION

In this paper, a wideband 2/3 prescaler is verified in the design of proposed wide band multimodulus 32/33/47/48 prescaler. A dynamic logic multiband flexible divider is designed which uses the wideband 2/3 prescaler , multimodulus 32/33/47/48 prescaler The proposed design successfully simplifies the control logic and one pMOS transistor alone serves the purposes of both mode select and counter excitation logic. The circuit simplicity leads to a shorter critical path and reduced power consumption. Post layout simulation results proved its advantages in power, speed, and layout area against previous designs. The Corresponding power summary is presented in the below report.

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		24
Vccint 1.20V:	5	6
Vccaux 2.50V:	7	18
Vcco25 2.50V:	0	0
Clocks:	0	0
Inputs:	0	0
Logic:	0	0
Outputs:		
Vcco25	0	0
Signals:	0	0
Quiescent Vccint 1.20V:	5	6
Quiescent Vccaux 2.50V:	7	18

Figure 6 Power Report

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