"Design and Analysis of 5GHz Frequency, Low- Phase-Noise, Parasitic Compensated LC Voltage Controlled Oscillator"

[1]Abhishek Patel [2] Vivek Dubey [3] Ravimohan

[1]*Research Scholar of M.Tech, (VLSI Design), Shri Ram Institute of Technology & Sciences, Jabalpur*
[2]*Asst. Professor, Electronics Department, Shri Ram Institute of Technology & Sciences, Jabalpur*
[3] *H.O.D.,Asst. Professor, Electronics Department, Shri Ram Institute of Technology & Sciences, Jabalpur*

***Abstract*—In this work design of a cross coupled topology with switched biasing technique is proposed which can work in high frequency region. The phase noise generated by the voltage controlled oscillator has been reduced by sizing the active devices, because the impact of physical parameter of device is large on the specification of any radio frequency integrated circuit.**

The proposed design is verified through standard 0.18 µm CMOS process supplied by Tanner's EDA simulation software tool. Several designs of voltage control oscillator circuits have been implemented for a comparison and verify that the switched biasing does improve frequency and phase noise performance. These results are then compared Simulation results shows an improvement from 114.3 dBc/Hz to -139.6 dBc/Hz at a 1 MHz offset frequency from the 5 GHz carrier when switched biasing. The relative increase in voltage control oscillator's phase noise performance translates in higher modulation accuracy when used in a transceiver, therefore this increase can be regarded as significant. The power consumption of the simulated VCO is around 746mW

***Keywords*-- CMOS, Cross-coupled, phase noise, Tanner EDA, VCO**

I. INTRODUCTION

A PLL is a control system, where phase is the variable of interest. The block diagram of a PLL is shown in Fig. 1.1. The circuit is called a phase-locked loop because the feedback operation in the loop automatically adjusts the phase of the output signal F_{out} to follow the phase of the reference signal F_{ref}. The prescaler (Frequency Divider in Fig.) divides the VCO frequency (and phase) by a division modulus of N.

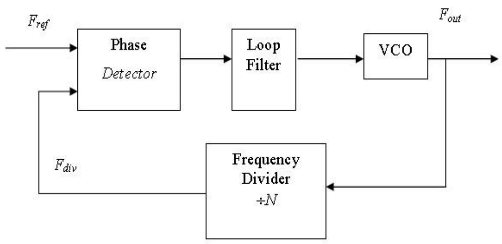

Fig 1. Phase Locked Loop

A. Voltage Controlled Oscillator

VCO is an electronic circuit designed to be controlled in oscillation frequency by a voltage input. The oscillator requires a tank circuit. A parallel resonance tank comprises of inductance (L) and capacitance (C). The principle operation of the VCO is by means of the controlled operation of the LC tank circuit. An oscillator can be described as a positive feedback system and it amplifies its own noise at a selected frequency $\omega 0$, as shown in Fig. 1.

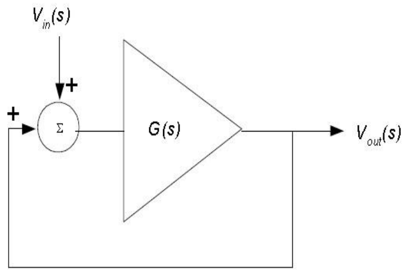

Fig. 2 Feedback diagram of an Oscillator

The transfer function of the oscillator is,

$$A_0 = \frac{V_{out}\,(s)}{V_{in}\,(s)} = \frac{G\,(s)}{1-G\,(s)} \qquad \textbf{1.1}$$

From equation (1.1), it can be concluded that the closed loop gain will approach infinity under the following conditions: (1) the open loop gain is equal to unity, i.e. $G(S) = 1$, and (2) the total phase shift of the loop is equal to 0o, i.e. $\angle G(S) = 0o$, which are called the Barkhausen's Criteria. In an environment with the existence of noise at all frequencies, the Barkhausen's Criteria is satisfied only with the noise at a specific frequency $\omega 0$. When the oscillation is properly started, the noise signal at frequency ω_o is amplified and increased till the amplifying devices are saturated. Hence, the stable oscillation is maintained. In order to ensure the startup of the oscillation in presence of temperature and process variations, the small signal loop gain is typically chosen to be 2-3 times of the required value.

In most applications, it is required that the oscillator to be tunable, where the output frequency is a function of a control input. Thus, a VCO can be described by

$$\omega_{out} = \omega_{fr} + K_{vco}\, V_c \qquad \textbf{1.2}$$

Where, ω_{fr} is the free running frequency of the VCO, is the control voltage of the VCO and is the gain of the VCO specified in rad/s/V. A voltage signal with magnitude of V_m can be described as

$$v_{out}(t) = v_m \cos(\theta(t)) \qquad \textbf{1.3}$$

Where, $\theta(t) = \int \omega_{out}\, dt + \theta_0$. Substituting equation (1.2) into equation (1.3), the sinusoidal voltage output signal of a VCO is given by,

$$v_{out}(t) = v_m \cos\left(\omega_{fr} t + K_{vco} \int v_c \, dt + \theta_0\right)$$

Where, K_{vco} is assumed to be linear.

B. *Phase Noise*

The noise produced by an oscillator is important in practice because it may severely damage the performance of communication receiver sys- tem. Phase noise refers to the short term random fluctuation in the frequency (or phase) of an oscillator signal.

$$\mathcal{L}\{f_m\} = 10 \log\left[\left[\left(\frac{f_0}{2Q_L f_m}\right)^2 + 1\right] \times \frac{FkT_0}{P} \times \left(\frac{f_c}{f_m} + 1\right)\right]$$

The equation describes the dependence of phase noise on the noise factor which ultimately depends on output noise spectral density generated by circuit.

II. TOPOLOGY OF VCO

The topology used for the proposed VCO is a cross coupled topology. Since the full exploitation of differential operation lowers undesirable common-mode effects such as extrinsic substrate and supply noise amplification and up conversion The rise and fall time symmetry is also incorporated to further reduce the *1/f* noise up conversion.

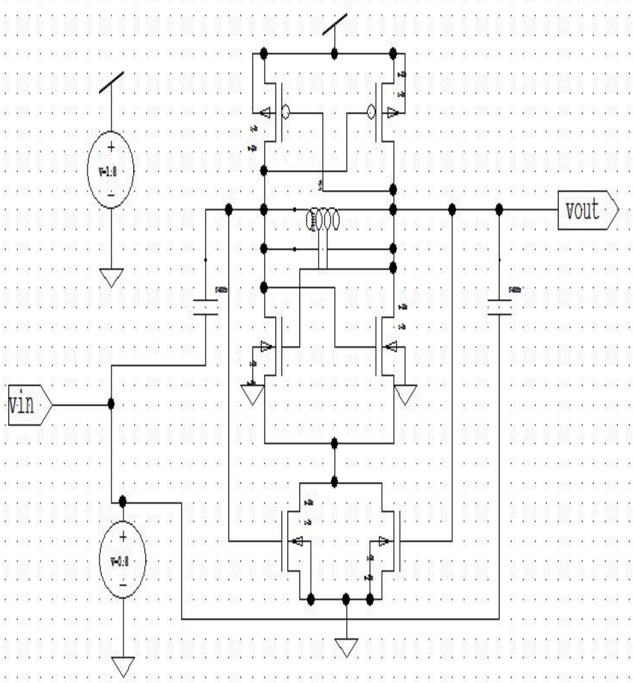

Fig. 2 cross coupled LC VCO

III. RESULT

A. *Transient Analysis Result*

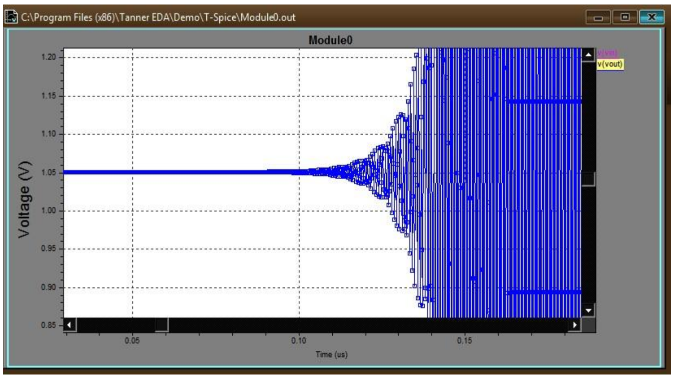

Fig 3.1 transient output of proposed LCVCO simulated through Tanner's EDA

B. *Noise Analysis Result*

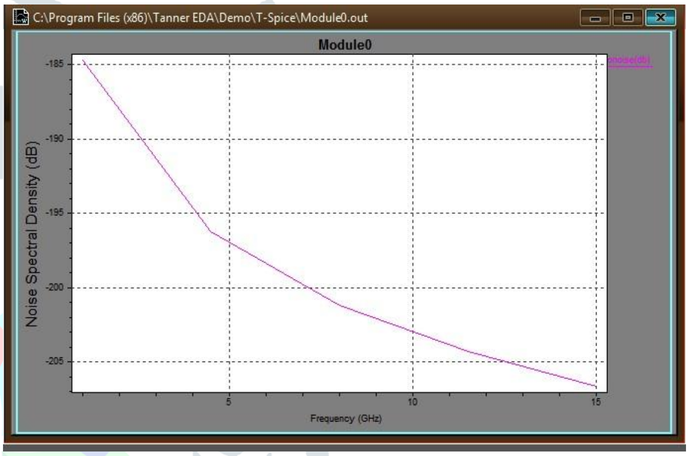

Fig 3.2 noise spectral density output of proposed LCVCO simulated through Tanner's EDA

C. *phase noise Result*

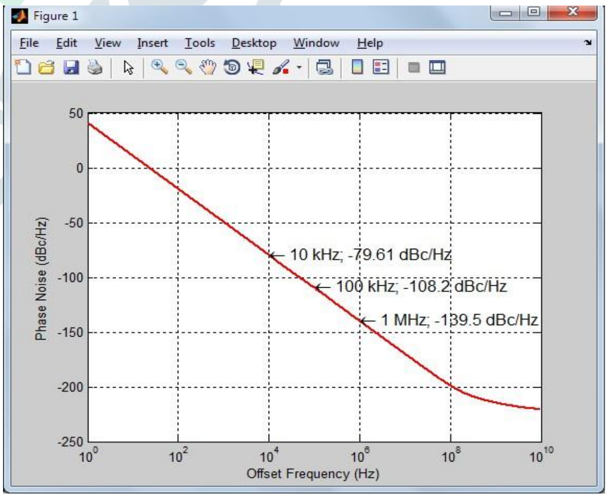

Fig 3.3 Phase noise

IV. CONCLUSION

The LC VCO has been designed with .18µm technology that shows a -139.5dBc/Hz of noise at offset frequency of 1MHz.

REFERENCES

[1] Weilei Feng, Lili Zhoul, Xuwei Yel, Jianhua Feng, Hongfi Ye, Xing Zhangl, "A 2.1mW, LOW Phase Noise Wideband Voltage Controlled Oscillator with Small Kvco Fluctuation", 12th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), 2014.

[2] Nisha Gupta "Voltage-Controlled Ring Oscillator for Low Phase Noise Application" International Journal of Computer Applications (0975 – 8887) Volume 14– No.5, January 2011.

[3] Chunhua WANG, Guanchao PENG, Minglin MA, Zhan LI "A New Low-Power CMOS Quadrature VCO with Current Reused Structure" Radio Engineering, vol. 20, no. 1, April 2011

[4] To Po WANG , Cheng-Yo Chiang "A Low-Power low phase noise wide tuning range k-band VCO in 0.18μm CMOS" IEICE Electronics Express,Vol.8,No.11,780–787, 2011

[5] Ge Yu " A study of two wideband CMOS LC-VCO structures" B.A.Sc., The University of British Columbia, 2009

[6] Chih-Hsiang Chang and Ching-Yuan Yang "A 0.18-μm CMOS 16-GHz Varactorless LC-VCO with1.2-GHz Tuning Range" IEEE Asian Solid-State Circuits Conference November 12-14, 2007

[7] S. Gribaldo, R. Boudot, G. Cibiel, V. Giordano, O. Llopis "Phase noise modelling and optimization of microwave SiGe amplifiers for sapphire oscillators applications" 19th European Frequency and Time Forum, Besançon : France (2005)

[8] Ali Hajimiri and T.H. Lee, "A general theory of phase noise in electrical oscillator," IEEE Solid-State Circuits, vol.33, pp. 179-194, Feb.1998.

[9] H. T. Friss, Fellow, IRE, "Noise Figure of Radio Receiver", proceedings of IRE, 1994

[10] Seyed Reza Hadianamrei, Masoud Sabaghi, Maziyar Niyakan Lahiji, Mehdi Rahnama, " Noise Phase CMOS Quadrature VCO with Superharmonic Coupling Using Cross-Couple Pair Low", Circuits and Systems, 2011, vol. 2, Pp. 281-285, Scientific Research, October 2011.

[11] J.M. Golio, The RF and Microwave Handbook, New York, NY: John Wiley & Sons,1st ed., 2000.

[12] J. Mukherjee and P. Roblin, "An Analytical Circuit-Based Model for White and Flicker Phase Noise in LC Oscillators," IEEE Trans. on Circuits and Systems I: sRegular Papers, vol. 54, no. 7, pp. 1584-1598, Jul. 2007.

[13] Gordana Dodig-Crnkovic, Theory of Science, Mälardalens Högskola, Sweden: 2003.

[14] L. Jia, Y. B. Choi and W. G. Yeoh, "A 5.8GHz VCO with Precision Gain Control," Proc. of IEEE RF IC Symposium, Honolulu, pp. 701-704, 3-5 Jun. 2007.

[15] O. Mazouffre, H. Lapuyade, J. Begueret, A. Cathelin, D. Belot and Y. Deval, "A 5 GHz Low-Power Quadrature SiGe VCO with Automatic Amplitude Control," Proc. of the Bipolar/CMOS Circuits and Technology meeting, Toulouse, pp. 57-60, 28-30 Sept. 2003.

[16] P. Delatte, G. Picun, L. Demeus and P. Simon, "A low-power 5 GHz CMOS LC-VCO Optimized for High Resistivity SOI Substrates," Proc. of 31st European Solid-State Circuits Conf. ESSCIRC 2005, Grenoble, pp. 395-398, 12-16 Sept. 2005.

[17] J. O. Plouchart, B. Klepser, H. Ainspan and M. Soyuer, "Fully Monolithic 3V SiGe Differential Voltage Controlled Oscillators for 5 GHz and 17 GHz Wireless Applications," Proc. of 24th European Solid-State Circuits Conference, Hague, pp. 332-335, 22-24 Sept. 1998.

[18] D. I. Sanderson and S. Raman, "5-6 GHz SiGe VCO with Tunable Polyphase Output for Analogue Image Rejection and I/Q Mismatch Compensation," Proc. of IEEE RF IC Symposium, San Jose, pp. 683-687, 8-10 Jun. 2003.

[19] L. Zhang, Z. Wang and H. Chen, "A 5-GHz CMOS VCO for IEEE 802.11a WLAN application," Proc. of 7th Int. Conf. on Solid-State and IC Tech., Beijing, vol. 2, pp. 1311-1314, 18-21 Oct. 2004. s

[20] S. Levantino, S. Samori, A. Gierkink and V. Boccuzzi, "Frequency Dependence on Bias Current in 5 GHz CMOS VCOs: Impact on Tuning Range and Flicker Noise Upconversion," IEEE J. Solid-State Circuits, vol. 37, no. 8, pp. 1003-1011, Aug. 2002.

[21] P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, Analysis and Design of Analogue Integrated Circuits, New York, NY: John Wiley & Sons, 4th ed., 2001.

[22] E. Hegazi, H. Sjoland and A. A. Abidi, "A Filtering Technique to Lower LC Oscillator Phase Noise," IEEE J. Solid-State Circuits, vol. 36, no. 12, pp. 1921-1930, Dec. 2001.

[23] D. J. Comer and D. T. Comer, Advanced Electronic Circuit Design, New York, NY: John Wiley & Sons, 2003.

[24] A. Hajimiri and T. H. Lee, "Oscillator Phase Noise: A Tutorial," IEEE J. Solid-State Circuits, vol. 35, no. 3, pp. 326-336, Mar. 2000.

[25] G. Niu, "Noise in SiGe HBT RF Technology: Physics, Modeling, and Circuit Implications," Proc. of the IEEE, Invited Paper, vol. 93, no. 9, pp. 1583-1597, Sep. 2005.

[26] X. Huang, F. Tan, W. Wei and W. Fu, "A Revisit to Phase Noise Model of Leeson," Proc. of IEEE Frequency Control Symposium, Geneva, pp. 238-241, 29 May - 1 Jun. 2007.

[27] D. B. Leeson, "A Simple Model of Feedback Oscillator Noise Spectrum," Proc. of the IEEE, vol. 54, no. 2, pp. 329-330, Feb. 1966.

[28] U. L. Rohde, A. K. Poddar and G. Bock, The Design of Modern Microwave Oscillators for Wireless Applications: Theory and Optimization, New York, NY: John Wiley & Sons, 2005.

[29] C. S. Vaucher, Architectures for RF Frequency Synthesizers, Springer, 1st ed., 2002.

[30] J. Terry and J. Heiskala, OFDM Wireless LANs: A Theoretical and Practical Guide, Pearson Technology Group Canada, 1st ed., Dec. 2001.

[31] I. Zamek and S. Zamek, "Crystal Oscillators Jitter Measurement and its Estimation of Phase Noise," Proc. of 2003 IEEE Int. Frequency Control Symposium and PDA Exhibition, Tampa, pp. 547-555, 5-8 May 2003.

[32] K. Hosaka, S. Harase, S. Izumiya and T. Hadachi, "A Cascode Crystal Oscillator Suitable for Integrated Circuits," Proc. of 2002 IEEE Int. Frequency Control Symposium and PDA Exhibition, New Orleans, pp. 610-614, 29-31 May 2002.

[33] K. K. Clarke and D. T. Hess, Communication Circuits: Analysis and Design, London, Addison-Wesley Publishing Company, 1974.

[34] C. W. Zhang and L. Forbes, "Simulation of Timing Jitter in Ring Oscillators," Proc. of the 15th Biennial Microelectronics Symposium, Boise, pp. 356-359, 30 Jun.-2 Jul. 2003.

[35] A. Hajimiri, S. Limotyrakis and T. H. Lee, "Phase Noise in Multi-Gigahertz CMOS Ring Oscillators," Proc. of IEEE 1998 Custom IC Conference, Santa Clara, pp. 49-52, 11-14 May 1998.