A Step-Down Transformer less Single Stage Single Switch Ac/Dc Converter

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***Abstract*-This paper presents a step-down transformer less single-stage single-switch ac/dc converter suitable for universal line applications. The topology integrates a buck-type power-factor correction (PFC) cell with a buck–boost dc/dc cell and part of the input power is coupled to the output directly after the first power processing. With this direct power transfer feature and sharing capacitor voltages, the converter is able to achieve efficient power conversion, high power factor, low voltage stress on intermediate bus and low output voltage without a high step-down transformer. The absence of transformer reduces the component counts and cost of the converter. Unlike most of the boost-type PFC cell, the main switch of the proposed converter only handles the peak inductor current of dc/dc cell rather than the superposition of both inductor currents. Detailed analysis and design procedures of the proposed circuit are given and verified by experimental results**

***Index Terms*-Direct Power Transfer (DPT), Integrated Buck Boost Converter (IBuBuBo), Single Stage (SS), Power Factor Correction (PFC)**

I. INTRODUCTION

Many industrial applications make use of controlled DC power, like in steel rolling mills, paper mills and textile mills, which employ DC motor drives. The basic advantages of DC motor are high starting torque, high accelerating and decelerating torque. DC motor is easily adaptable for drives requiring wide range speed control and quick reversals. So DC machine possesses high degree of flexibility and versatility. The losses like eddy current loss, hysteresis loss are also absent in DC applications. For some industrial applications a versatile AC to DC converter is indispensable. Direct current is used to charge batteries, and in nearly all electronic systems as the power supply. Very large quantities of direct-current power are used in production of aluminum and other electrochemical processes. Direct current is also used for some railway propulsion, especially in urban areas. High voltage direct current (HVDC) is used to transmit large amounts of power from remote generation sites or to interconnect alternating current power grids.

The aim of the project is to obtain a controlled DC output from a standard single phase 230V, 50Hz power supply. For this we first rectified the AC voltage using four diodes. Then the rectified DC voltage is used to get controlled DC voltage output using an MOSFET with a pulse of variable duty cycle, by varying the duty cycle of the square wave pulse the average output DC voltage is regulated. Here we are used a single stage circuit because Single-stage (SS) AC to DC converters have received much attention in the past decades because of its cost effectiveness, compact size, and simple control mechanism. Among existing SS converters, most of them are comprised of a boost power-factor correction (PFC) cell followed by a dc/dc cell for output voltage regulation. Their intermediate bus voltage is usually greater than the line input voltage and easily goes beyond 450 V at high-line application. Although there are a lot of efforts to limit this bus voltage, it is still near or above the peak of the line voltage due to the nature of boost-type PFC cell. For application with low output voltage (e.g.,≤48V), this high intermediate bus voltage increases components stresses on the DC to DC cell. With a simple step-down DC to DC cell (i.e. buck or buck–boost converter), extremely narrow duty cycle is needed for the conversion. This leads to poor circuit efficiency and limits the input voltage range for getting better performance.

II. Proposed circuit & its Operating Principle*:*

Single-stage (SS) AC to DC converters has received much attention in the past decades because of its cost effectiveness, compact size, and simple control mechanism. Among existing SS converters, most of them are comprised of a boost power-factor correction (PFC) cell followed by a DC to DC cell for output voltage regulation. Their intermediate bus voltage is usually greater than the line input voltage and easily goes beyond 450 V at high-line application. Although there are a lot of efforts to limit this bus voltage, it is still near or above the peak of the line voltage due to the nature of boost-type PFC cell. For application with low output voltage (e.g., ≤48V), this high intermediate bus voltage increases components stresses on the dc/dc cell. With a simple step-down dc/dc cell (i.e. buck or buck–boost converter), extremely narrow duty cycle is needed for the conversion. This leads to poor circuit efficiency and limits the input voltage range for getting better performance. Therefore, a high step-down transformer is usually employed even when galvanic isolation is not mandatory. For example, LED drivers without isolation may satisfy safety requirement.

This greatly increases the difficulty in its implementation due to the minimum on-time of pulse-width-modulation (PWM) IC and rise/fall time of MOSFET. More details on comparing different approaches will be given in the Section V. In this paper, an integrated buck–buck–boost (IBuBuBo) converter with low output voltage is proposed. The converter utilizes a buck converter as a PFC cell. It is able to reduce the bus voltage below the line input voltage effectively. In addition, by sharing voltages between the intermediate bus and output Capacitors, further reduction of the bus voltage can be achieved.

Therefore, a transformer is not needed to obtain the low output voltage. To sum up, the converter is able to achieve
1) Low intermediate bus and output voltages in the absence of transformer;
2) Simple control structure with a single-switch;
3) Positive output voltage;
4) High conversion efficiency due to part of input power is processed once and
5) Input surge current protection because of series connection of input source and switch.

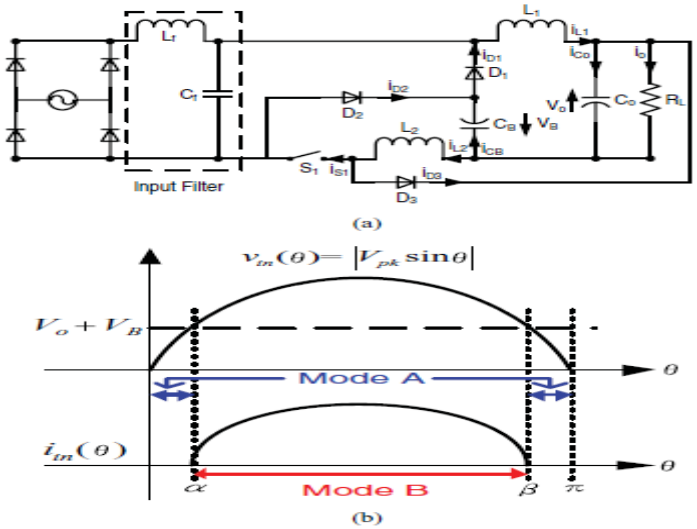

Fig:. (a) IBuBuBo SS ac/dc converter. (b) Input voltage and current waveforms.

ModeA(vin (θ)≤VB + Vo): When the input voltage vin (θ) is smaller than the sum of intermediate bus voltage VB , and output voltage Vo , the buck PFC cell becomes inactive and does not shape the line current around zero-crossing line voltage , owing to the reverse biased of the bridge rectifier. Only the buck–boost dc/dc cell sustains all the output power to the load. Therefore, two dead-angle zones are present in a half-line period and no input current is drawn as shown in Fig. 4.1(b). The circuit operation within a switching period can be divided into three stages and the corresponding sequence is Fig. 4.2(a),(b), and (f). Fig. 4.3(a) shows its key current waveforms.

1) Stage 1 (period d1Ts in Fig. 4.3) [see Fig. 4.2(a)]: When switch S1 is turned ON, inductor L2 is charged linearly by the bus voltage VB while diode D2 is conducting. Output capacitor Co delivers power to the load.
2) Stage 2 (period d2Ts in Fig. 4.3) [see Fig. 4.2(b)]: When switch S1 is switched OFF, diode D3 becomes forward biased and energy stored in L2 is released to Co and the load.
3) Stage 3 (period d3Ts - d4Ts in Fig. 4.3) [see Fig. 4.2(f)]: The inductor current iL2 is totally discharged and only Co sustains the load current.

Mode B (vin (θ) > VB + Vo): This mode occurs when the input voltage is greater than the sum of the bus voltage and output voltage. The circuit operation over a switching period can be divided into four stages and the corresponding sequence is Fig. 4.2(c), (d), (e), and (f). The key waveforms are shown in Fig. 4.3(b).

1) Stage 1 (period d1Ts in Fig. 4.3) [see Fig. 4.2(c)]: When switch S1 is turned ON, both inductors L1 and L2 are charged linearly by the input voltage minus the sum of the bus voltage and output voltage (vin (θ) − VB − Vo), while diode D2 is conducting.
2) Stage 2 (period d2Ts in Fig. 4.3) [see Fig. 4.2(d)]: When switch S1 is switched OFF, inductor current iL1 decreases linearly to charge CB and Co through diode D1 as well as transferring part of the input power to the load directly. Meanwhile, the energy stored in L2 is released to Co and the current is supplied to the load through diode D3. This stage ends once inductor L2 is fully discharged.
3) Stage 3 (period d3Ts in Fig. 4.3) [see Fig. 4.2(e)]: Inductor L1 continues to deliver current to Co and the load until its current reaches zero.
4) Stage 4 (period d4Ts in Fig.4.3) [see Fig. 4.2(f)]: Only Co delivers all the output po

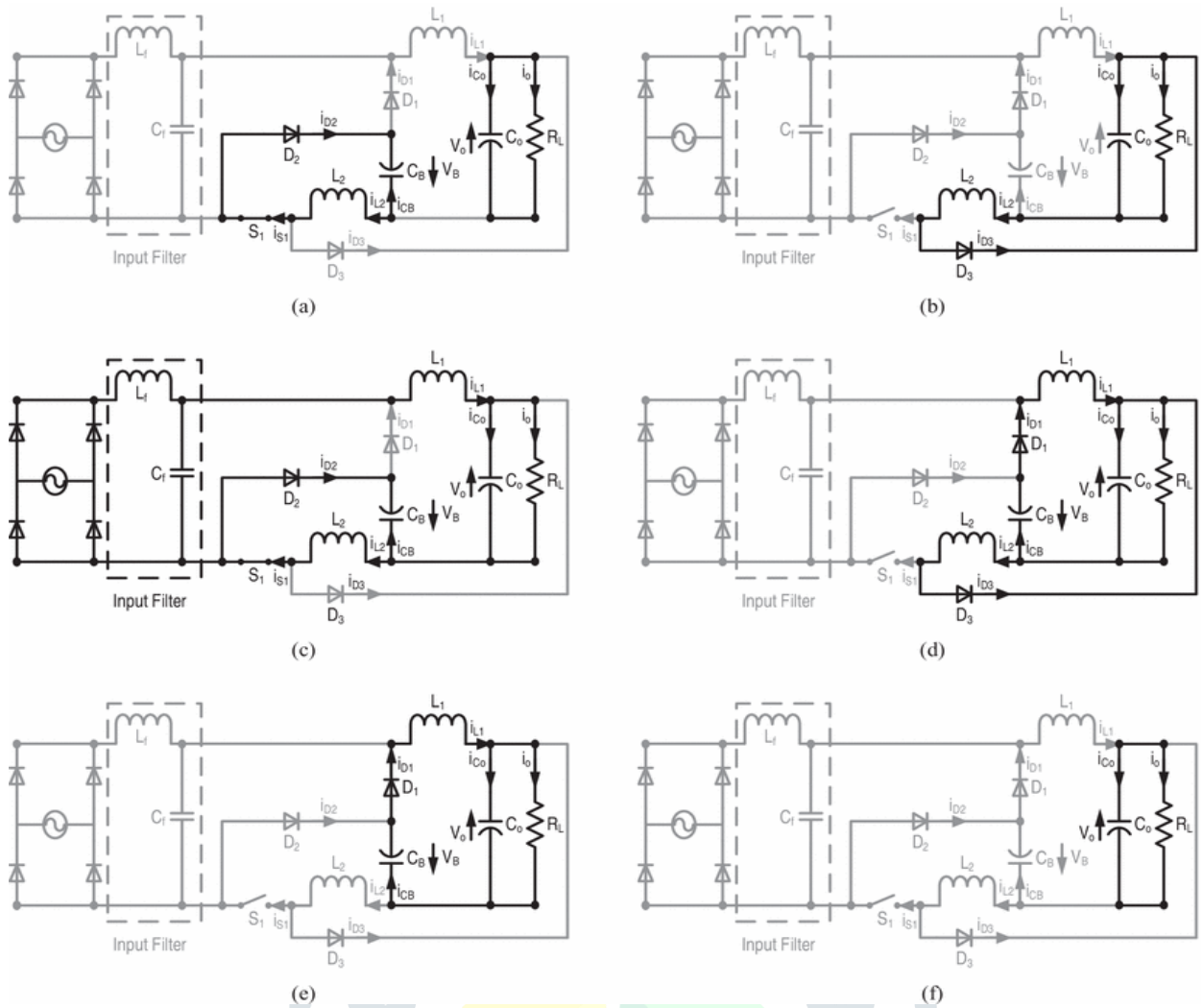

Figure: Circuit operation stages of the proposed ac/dc converter.

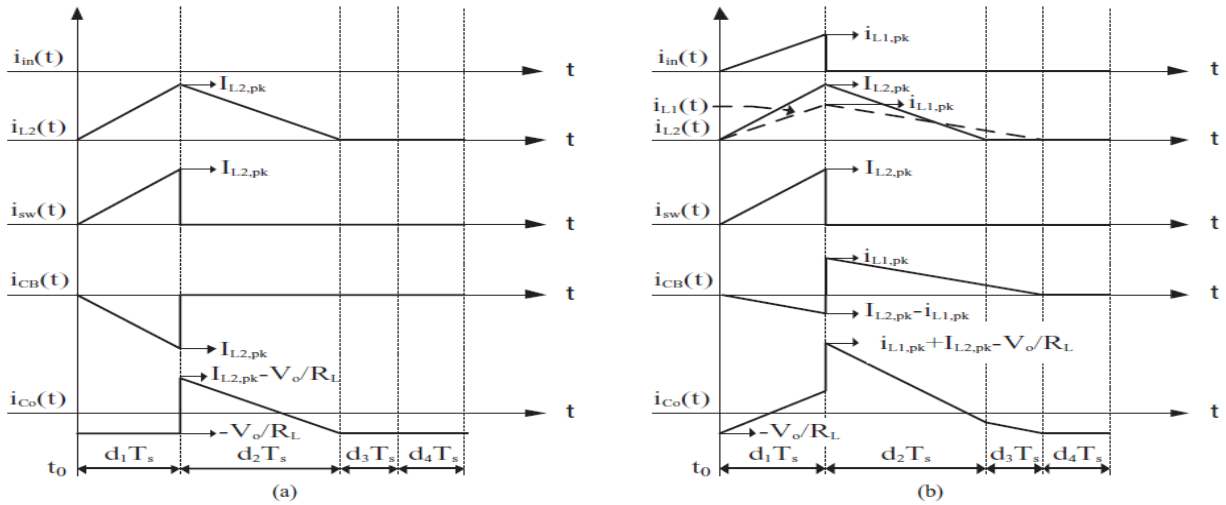

Figure. . Key waveforms of the proposed circuit

Design Considerations:

To simplify the circuit analysis, some assumptions are made as follows:

1) All components are ideal;

2) Line input source is pure sinusoidal, i.e. $v_{in}(\theta) = V_{pk}\sin(\theta)$ where V_{pk} and θ are denoted as its peak voltage and phase angle, respectively;

3) Both capacitors CB and Co are sufficiently large such that they can be treated as constant DC voltage sources without any ripples;

4) The switching frequency fs is much higher than the line frequency such that the rectified line input voltage $|vin(\theta)|$ is constant within a switching period.

Circuit Characteristics

There is no input current drawn from the source in Mode A, and the phase angles of the dead-time α and β can be expressed as

$$\alpha = \arcsin\left(\frac{V_T}{V_{pK}}\right)$$

$$\beta = \pi - \alpha = \pi - \arcsin \ldots\ldots\ldots\ldots\ldots\ldots(1)$$

Where V_T is the sum of V_B and Vo . Thus, the conduction angle of the converter is

$$\gamma = \beta - \alpha = \pi - 2\arcsin\left(\frac{V_T}{V_{PK}}\right) \ldots\ldots (2)$$

From the key waveforms the peak currents of the two inductors are

$$i_{L1-PK} = \left\{\frac{v_{in}(\theta) - V_T}{L_1} d_1 T_s, \quad \alpha < \theta < \beta \right. \quad \ldots\ldots\ldots (3)$$

Other wise

$$i_{L2-PK} = \frac{V_B}{L_2} d_1 T_s \quad \ldots\ldots\ldots\ldots\ldots\ldots (4)$$

Where T_s (1/fs) is a switching period of the converter. The dependency of iL1 pk on θ has been omitted for clarity. It is noted that L_2 does not contribute in (3) even though it is on the current return path of the PFC cell. In addition, by considering volt–second balance of the L_1 and L_2 , respectively, the important duty ratio relationships can be expressed as follows:

$$d_2 + d_3 = \left\{ \frac{v_{in}(\theta) - V_T}{V_T} d_1, \alpha < \theta < \beta \right. \quad \ldots\ldots\ldots (5)$$

Experimental Results:

The performance of the proposed circuit is verified by the prototype. To ensure the converter working properly with constant output voltage, a simple voltage mode control is employed. To achieve a high performance of the converter for universal line operation in terms of low bus voltage (<150V) and high power factor (> 96 %), the inductor ratio has to be optimized. The lower bus voltage of the converter, the lower voltage rating capacitor (150 V) can be used. In this circuit we can change the output voltages by changing the duty cycle of pulse generator.

TABLE

Parameters	Value
Input filter inductor L_f	2 mH
Input filter capacitor C_f	2μF
Inductor L_1	90 μH
Inductor L_2	46 μH
Inductance ratio (M = L2/L1)	0.434
C_b	5mF
C_0	40Mf

Table depicts all the components used in the circuit, and its specifications is stated as fallows

1) Output voltage : 12 V_{DC}
2) Power factor : > 96%
3) Line input power : 230 V_{AC} / 50 Hg
4) Switching frequency : 20 KHz

The direct power transfer ration under this condition coupled is V_O/V_T. It can be seen that the portion of direct power transfer from input to output decreases when V_B becomes larger resulting in increase of V_T. In other words, the direct power transfer decreases when the line input voltage increases. The increase of V_B will lower the conversation efficiency of dc/dc cell due to larger voltage conversion around ten times at high –line conditions. On the other hand decrease of V_B extends the conduction angle of the converter leading to higher power factor. However, the lower V_B requires decrease of inductance ratio resulting in higher peak inductor, bus voltage, power factor, the converter is capable to be used under high – line condition with the full load efficiency around 84% at 540 V_{rms}. The waveform shows fig 5.6.1 input voltage under full load condition at 230 Vac / 50HZ, measured current and voltages are shown in the fig So the proposed converter circuit gives the maximum efficiency of the circuit is around 89 % at low line applications.

III.SIMULATION RESULTS:

Simulink Circuit

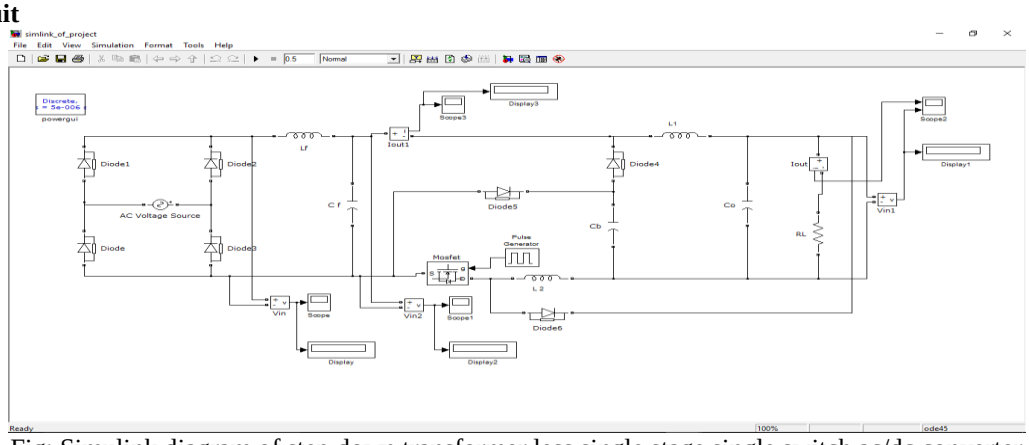

Fig: Simulink diagram of step down transformer less single stage single switch ac/dc converter

5.2 INPUT VOLTAGE SIGNAL IN SCOPE:

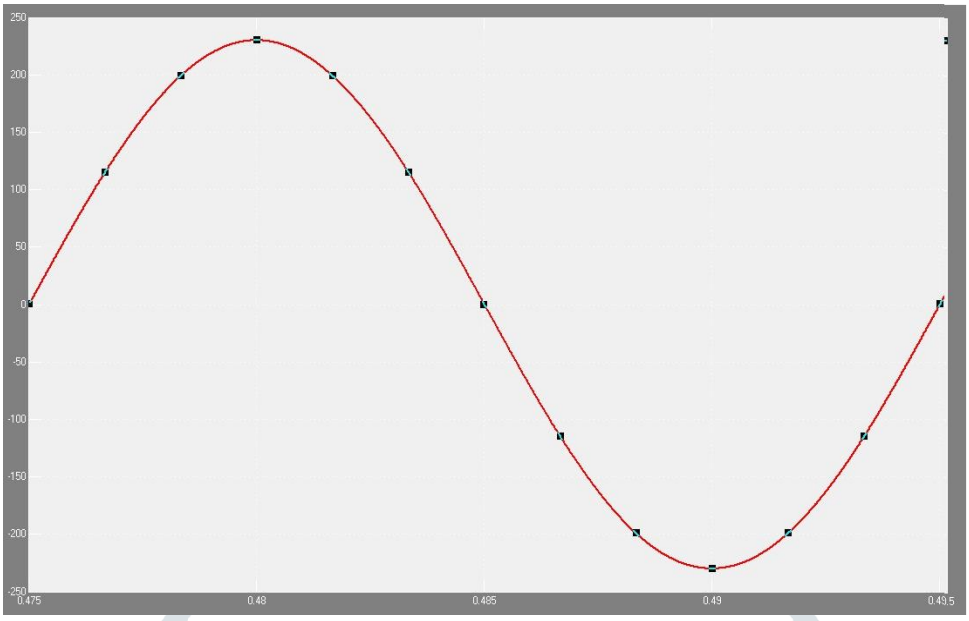

Fig: Simulink input voltage applied to circuit

5.3 OUTPUT WAVEFORM ACROSS THE LOAD

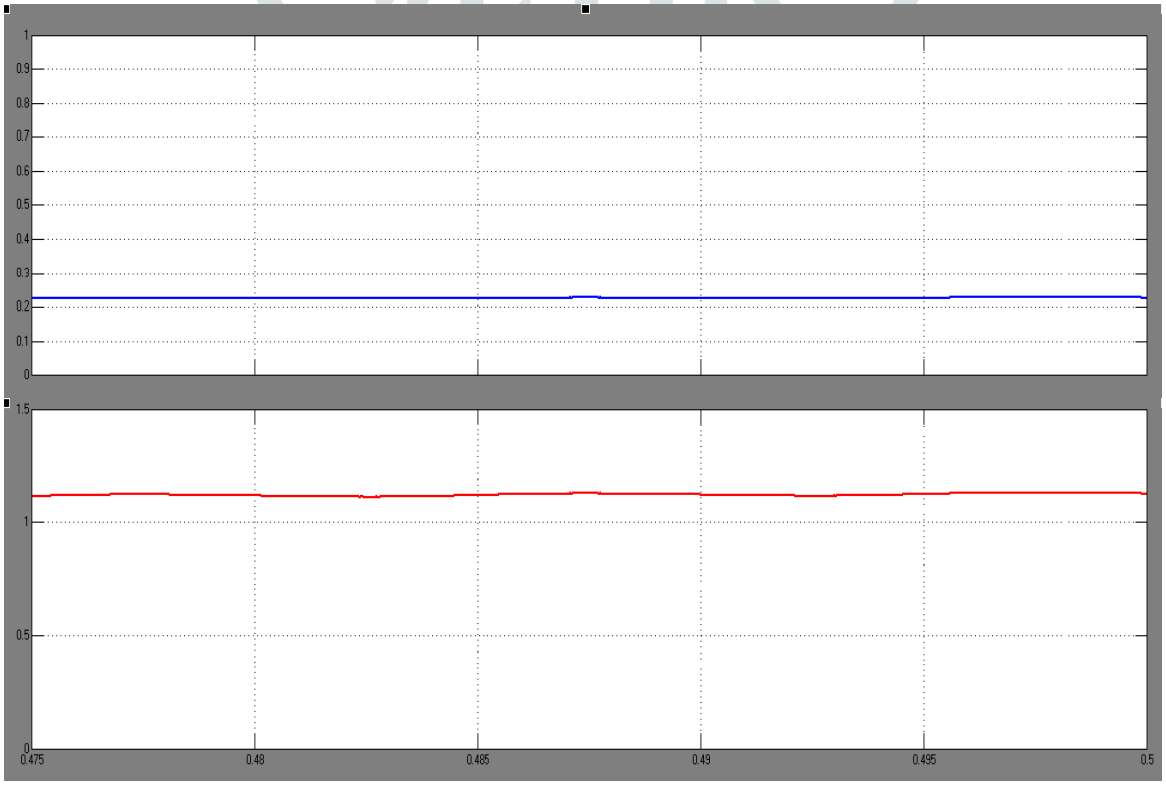

Fig: output waveforms of current and voltages across the load on scope

Conclusion:

The proposed IBuBuBo single-stage ac/dc converter has been experimentally verified, and the results have shown good agreements with the predicted values. The intermediate bus voltage of the circuit is able to keep below150Vat all input and output conditions, and is lower than that of the most reported converters. Thus, the lower voltage rating of capacitor can be used. Moreover, the topology is able to obtain low output voltage without high step-down transformer. Owing to the absence of transformer, the demagnetizing circuit, the associated circuit dealing with leakage inductance, and the cost of the proposed circuit are reduced compared with the isolated counterparts. In addition, the proposed converter can meet IEC 61000-3-2 standard, and provide both input surge current and output short-circuit protection. Thanks to the direct power transfer path in the proposed converter, it is able to achieve high efficiency around 89%.

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