A NOVEL 4-Bit ARITHMETIC LOGIC UNIT DESIGN FOR POWER AND AREA OPTIMIZATION

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***Abstract*- In the modern era, power dissipation and area of the circuit under fabrication has become a major and vital constraint in the electronic industry. The objective of this paper is to reduce the power dissipation in the circuit by using gate diffusion input technique. The purpose of this paper is to design and implementation of Arithmetic & logic unit (ALU) using Gate Diffusion Input (GDI) which is area optimized techniques. Design consist of 4-bit arithmetic and logic unit by GDI technique where the logical operation perform by GDI and arithmetic operations are perform via proposed design. Arithmetic operation such as ADDITION, SUBTRACTION, INCREMENT and logical operation like AND, OR, etc., GDI technique reduces average power consumption and number of transistor than CMOS transistor. The simulation tool used is TANNER EDA 15.0 using 250nm technology with 3.2V as a supply voltage**.

***Keywords*: - ARITHMETIC & LOGIC UNIT, GATE DIFFUSION INPUT, FULL ADDER**

I. INTRODUCTION

With the rapid use of portable device in electronic devices the power dissipation is the main constraints now a day. As the technology grows rapidly and the device size scales down to nanometer, power dissipation, area and path delay are the major factors considered. The tremendous proliferation in battery powered devices like mobile, laptop put a tight requirement on low power consumption to achieve consistent heat dissipation over period of operating cycle .The evolution in integrated circuit increases the number of transistor in a chip thereby complexity increased in multi fold. As per the Moore's Law the number of transistor in a year is getting doubled for every eighteen month. To validate this statement the size of the transistor is getting shrink down as the technology advances. While increasing the transistor count and decrease in the size directly impacts on the increase in power consumption. The main contributors of power dissipation are static, dynamic and leakage power consumption [9]. Static is due to direct path exists when the supply rails are shortened the input transition is a key factor for charging and discharging the node capacitance which produces dynamic power consumption. ALU is a basic building block of an arithmetic circuit. It is not only used for addition and also used for subtraction, multiplication and division. It is used in microprocessor and implementation of address generation circuits. So the optimization in design of ALU yields better performance of system as a whole. The optimization can be carried out in two stage system level and circuit level. In the system level the optimization can be carried out by input pattern such way to minimize the number of transition, architectural realization, gate level optimization, minimizing the critical path i.e. longest path takes reaching the output from an input. These approaches lead to minimize the number of transition, transistor count and increase the speed respectively. In the circuit level, the implementation logic style decides the power consumption, speed of the circuit, minimum number of transistor, full swing output, good driving capability for different load conditions and regular layout.

1.1 GATE DIFFUSION INPUT TECHNIQUE

Morgenshtein has proposed basic GDI cell for low power digital combination circuit this is the new approach which is shown in fig1.GDI cell provide in-cell swing restoration under certain operating condition basically GDI is a two transistor implementation of complex logic function. This approach leads to reduction in power consumption, propagation delay and area of digital circuits is obtained while having low complexity of logic design. Source of the PMOS in a GDI cell is not connecting to VDD it is an important feature of a GDI cell.

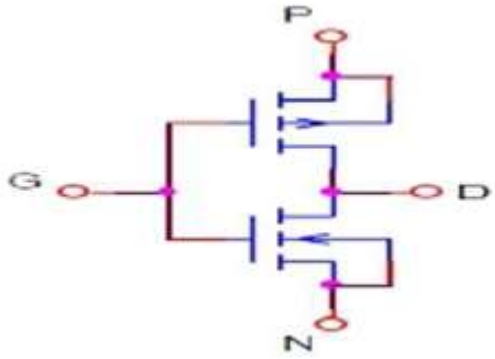

Fig. 1 BASIC GDI CELL

GND is not connected to source of NMOS; hence GDI cell gives two extra input pins for input which makes the GDI design more flexible as the input can connect to any terminal. There are three inputs in a GDI cell - G which is common gate input of NMOS and PMOS, P as a input to the source/drain of PMOS and N as a input to the source/drain of

NMOS. Bulks of NMOS connected to N and bulk of PMOS is connected to P. Table 1 shows different logic functions implemented by GDI logic based on different input values. So, various logic functions can be implemented with less power and high speed with GDI technique as compared to conventional CMOS design.

S.No.	N I/P	P I/P	G I/P	Output	Function
1.	0	B	A	A'B	F_1
2.	B	1	A	A'+B	F_2
3.	1	B	A	A+B	OR
4.	B	0	A	AB	AND
5.	C	B	A	A'B+AC	MUX
6.	0	1	A	A'	NOT

Table 1 BASIC FUNCTION OF GDI CELL

From table 1 most of the fundamental circuits can be made.

1.2 TRANSMISSION GATE

CMOS transmission gate consist of the NMOS and PMOS connected in parallel. The gate voltage applied to input to these two transistors are set to be complimentary signals. So CMOS TG operates as a bidirectional switch between the node Input and node Output which is controlled by input. (As shown in fig. 2)

If the controlled signal is logic high then both transistor turn on and provide low resistance current path between the node input and output. IN other hand if controlled signal is low i.e., 0 then both transistors will be OFF and path between input and output will be open circuit. By using this operation we can design multiplexers hence 2:1 mux and 4:1mux are design using TG. It consist of high switching characteristics so that it consume low power and result in lower power dissipation.

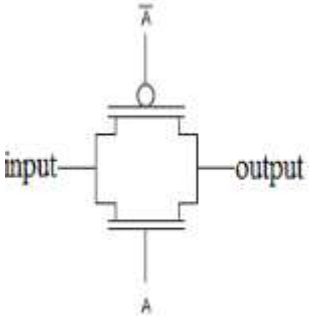

Fig. 2 Basic representation of Transmission Gate

II IMPLEMENTATION

A} Full Adder

The basic GDI cell for 180nm is shown in Fig 3 This circuit is similar to the invertor but P and N terminals are not connected with VDD and Ground terminal always. When Vdd and Ground terminals are connected to P and N respectively it act as a normal invertor but its bulk is connected. Result where obtained while GDI act as a invertor.

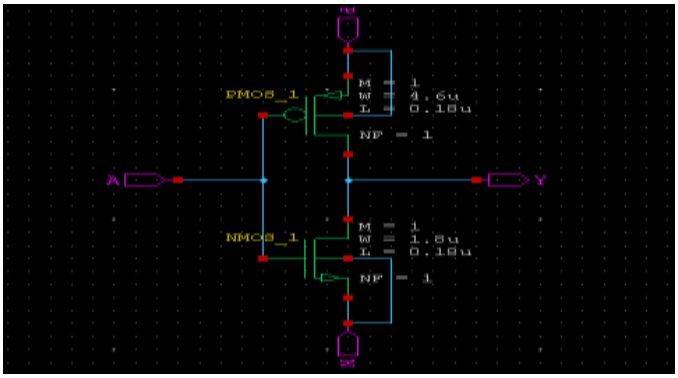

Fig.3 GDI CELL

For 250nm technology the parameter selected for PMOS and NMOS are 4.6um and 1.8um respectively. Test made on 3.2v supply voltage

Simulated Output GDI CELL:-

Avg. Power- 58.19nw
Delay- 0.3ns
Number of Transistor - 2

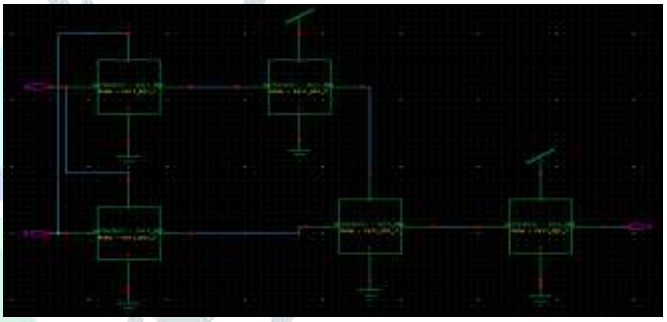

Fig. 4 XOR GATE USING F1 FUNCTION

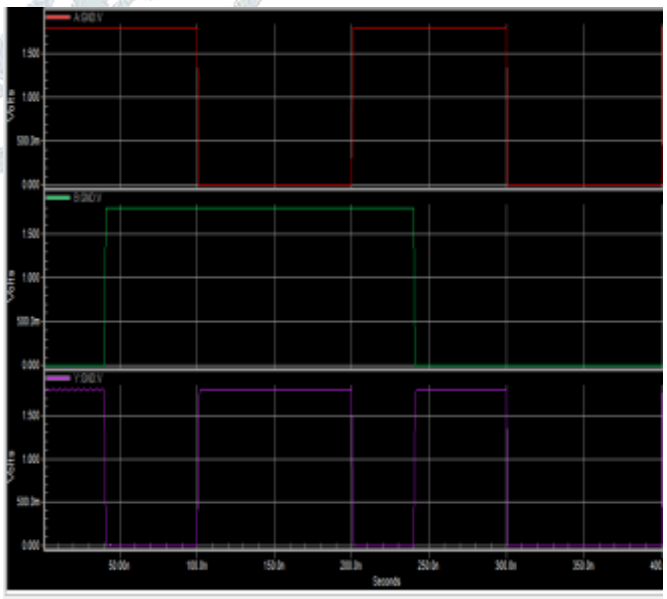

Fig.5 W-EDIT of XOR GATE

EXOR function is the key variable in adder equations. If the generation of them is optimized, this could greatly enhance the performance of the full adder cell. The GDI EXOR gate requires only 10 transistors by using F1 function shown in fig. 4. The propose GDI EXOR gate use less transistor when compared with CMOS counterpart. Input voltage is given as 3.2V. W-Edit of GDI EXOR Gate is shown in Fig 5.

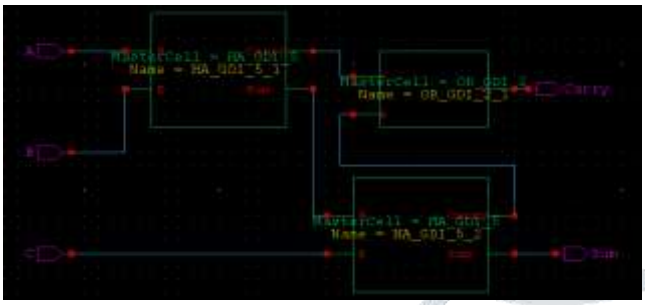

Fig.6 1-BIT FULL ADDER BY GDI

The transistor level implementation of GDI Full Adder using 34 transistors is shown in Fig 6. We propose a Novel Full Adder using 34 Transistors. This full adder consists of two modules one half adder and a OR Gate both are implemented by F1 function of GDI technique. These Full adders use fewer transistors when compared with CMOS counterpart. Due to the advantages of GDI cell, less transistor count this circuit can achieve its benefit of low power consumption. GDI Full Adder is shown in Fig 6.

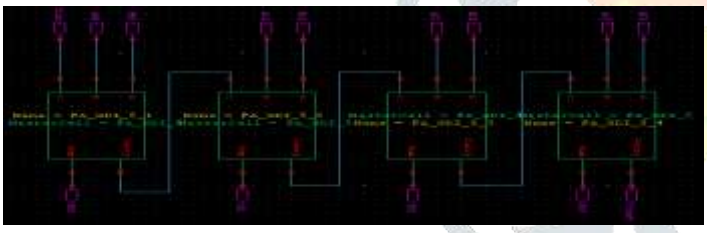

Fig.7 4-BIT FULL ADDER

Fig. 7 Shown the cascaded formation of 1-bit FA and it act as a 4-bit Full Adder in which A0,A1,A2,A3, B0,B1,B2,B3 and Cin are the input signals to the circuit which are taken as a bit format. Also the S0, S1, S2, S3 are the output as a sum in Full adder and Cout as a Carry in the circuit.

SUM = (A) XOR (B) XOR (Cin)

CARRY = AB+BC+ACin

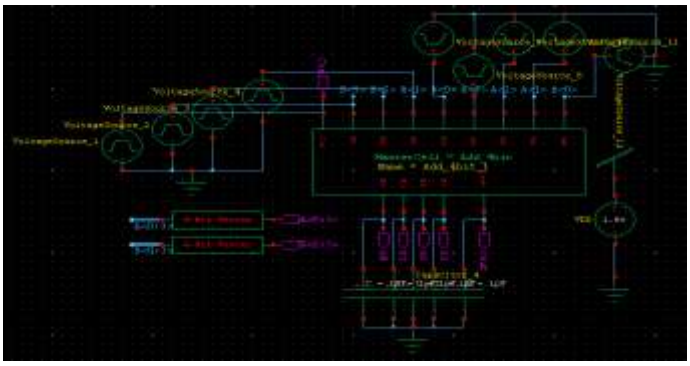

Fig.8 4-BIT FULL ADDER TEST

Fig. 8 shows the test vector for the 4bit FA where inputs are access to the circuit and output obtained as SUM (4-bit) and Cout.

Fig. 9 shows W-edit of the test where 4-bit are given as a input. All parameters are shown in table 2 and 3 for comparative study with conventional CMOS design and GDI design.

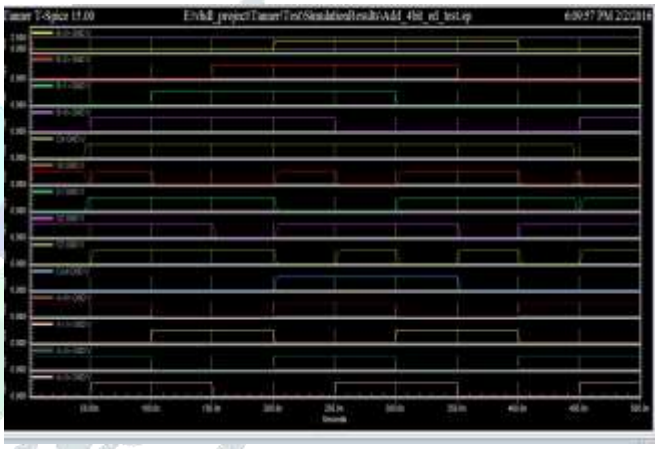

Fig.9 W-edit 4-BIT FULL ADDER

B} Multiplexers

Multiplexers are made by using transmission gate to reduce delay and power. Fig.10 shows the 4:1Mux I which s0 and s1 are the select line from which output y obtained.

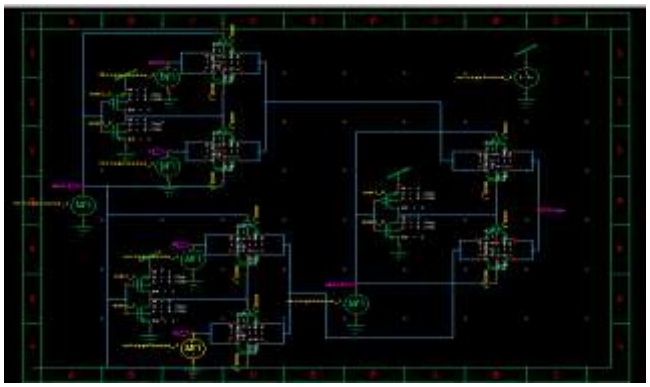

Fig. 10 4:1 Multiplexer Schematic Via TG

C} Arithmetic and Logic Unit

The arithmetic and logic unit is the main fundamental block of the microprocessor it mainly perform the logical & arithmetic operations such as logical AND, logical OR, Logical XOR. ALU is essential building block of the Control processing unit.The ALU have mainly five stages consist of the three main stages 1) Input multipliers 2) Full adders 3) Output multipliers . The ALU performs the four arithmetic operation like DECREMENT ADDITION SUBTRACTION & INCREMENT. And rest of the logical operation like AND, XOR, XNOR & OR. At input terminal one 4:1 mux is present to fetch the input according to our requirement of logic. At output section consist of 4:1 and 2:1 multiplexers. The multiplexers are made by the transmission gate and full adder is designed by using GDI technique (Gate Diffusion input). Fig. 11 shows the ALU design consisting of eight 4:1mux , four full adders and four 2:1mux. The 4-Bit ALU was designed by using 250nm n-well CMOS technology. All of the Full adders are made by Gate diffusion input.

Each stage of ALU consist of four inputs at input section fig.11 shows the block diagram of ALU. All the working principle is based on the vale Logic '1' and Logic '0' which correspond to 'Vdd' 'Vss'. An INCREMENT operation is analyzed as adding a '1' to the addend for DECREMENT operation all value of Vdd is provided to Full adder so the input A0A1A2A3 can be DECREMENT. Same manner ADDITION. The output of the half adder and or gate are result in the AND, EXOR, EXNOR, OR. Based on the condition of the select signals the multiplier stages select appropriate input and gives it to output section. Table 2 shows the status of select signals.

SELECTION LINES			OPERATIONS
S2	S1	S0	
0	0	0	DECREMENT
0	0	1	ADDITION
0	1	0	SUBSTRACTION
0	1	1	INCREMENT
1	0	0	AND
1	0	1	EXOR
1	1	0	EXNOR
1	1	1	OR

Table 2 Select Line Operation For ALU

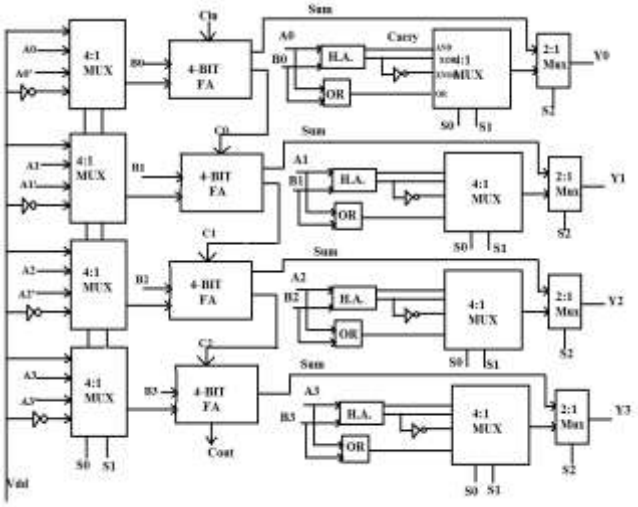

Fig. 11 Block Diagram of 4-Bit ALU

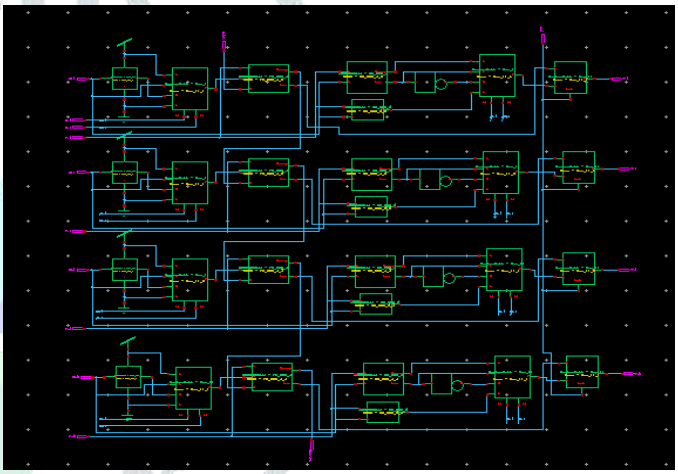

Fig. 12 Schematic Diagram of 4-Bit ALU

The ALU design is simple and efficient in terms of area and timing. The gate diffusion input design reduces the parasitic capacitance and result in lower power dissipation and fast circuit.

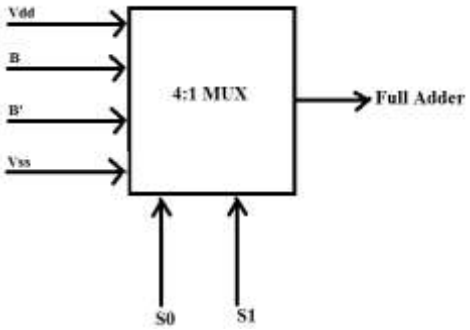

Fig. 13 Block Diagram of Input Stage

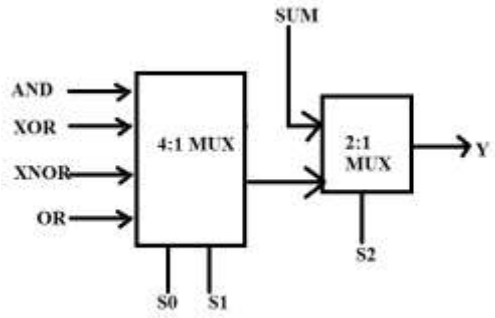

Fig. 14 Block Diagram of Output Stage

The input and output stages have a combination of 4:1 multiplexer to select one signal from set of four signals. The select signals s0 s1 pick from the 4:1mux and s2 pick from the 2:1mux according to logic supplied to select signals the operations are perform for ALU. The approach gives better result in terms of delay, area as well as power consumption.

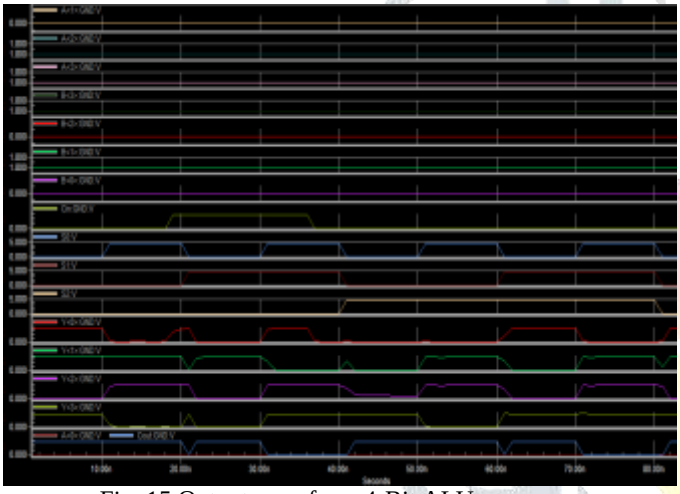

Fig. 15 Output waveform 4-Bit ALU

TABLE 3. Comparison Between existing and Proposed 4-BIT ALU

S. NO.	DESIGN TYPE	Technology	AVG POWER (µ W)	NO. OF TRANSISTOR
1.	CMOS	250nm	4204.5	592
2.	Gate Diffusion Input	250nm	1030.5	232
3.	PRAPOSED ALU Design	250nm	930.7	400

III. CONCLUSION

Power consumption in modern devices are a growing concern on demand for increased battery life , lower heat dissipation and increased device reliability is on the rise. In this paper the power optimization at architecture level is demonstrated by design of 4-bit Arithmetic and logic unit using GDI technique. Also reduction number of transistor automatically leads to minimum possible area of the circuit i.e. reduced surface area of silicon. Proposed design proves that it have better result in terms of performance characteristics.

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