Modeling and Analysis of Trap-Assisted Gate Tunneling in Dual-Layer High-k Gate Dielectrics

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Abstract

This paper presents a detailed modeling and analysis of trap-assisted gate tunneling in dual-layer high-k gate dielectric structures such as SiO_2/HfO_2 and SiO_2/ZrO_2. The study explores the effects of interface traps, trap density, and temperature on the gate leakage current characteristics of nanoscale MOS devices for sub-45 nm technology node. The analytical model is developed by considering electron injection into dual dielectric layers with a single trap energy level below the conduction band edge. The simulation results show that the incorporation of high-k materials reduces gate leakage significantly compared to single oxide layers, while the presence of traps increases leakage depending on trap density and position. The SiO_2/HfO_2 stack demonstrates the lowest leakage and the best thermal stability, making it a potential dielectric stack for future CMOS scaling.

Keywords

High-k dielectric, Trap-assisted tunneling, Gate leakage current, Interface traps, Temperature dependence, Dual-layer structure

I. Introduction

Metal Oxide Semiconductor Field Effect Transistors has enabled the unparalleled advancement of the semiconductor electronics industry. In order to follow Moore's Law [1], device scaling is the key attribute for planar MOSFET circuitry. Device scaling is ultimately the reduction in device dimensions. As lengths and widths are reduced, thickness of the gate dielectric must also be reduced. There are a number of issues in scaling MOSFET devices, particularly for the sub-45 nm technology evolution. The most critical issue is the gate dielectric, because very thin gate oxides are required for sub-45 nm generations. For such thin oxides, gate leakage current due to direct tunneling becomes unacceptably large. In order to decrease the leakage current due to tunneling, the physical thickness of the dielectric must increase, while the equivalent oxide thickness must continue to be reduced. Use of alternate gate materials with dielectric constant higher than that of silicon dioxide is the leading projected solution to reduce the gate leakage current to more tolerable levels. Therefore, modeling of the thin oxide related issue such as gate direct tunneling current is crucial for further gate oxide scaling. Modeling and simulation can play a critical role in overcoming difficult challenges for future technology. In this paper, device physics issues on nanoscale MOSFETs are discussed. Aggressive scaling of MOSFET devices has resulted in ultra-thin gate dielectrics, which in turn have increased the gate leakage current due to direct tunneling through the conventional SiO_2 layer. To address this limitation, high-k dielectrics such as HfO_2 and ZrO_2 have been introduced to replace SiO_2, providing higher capacitance at the same equivalent oxide thickness (EOT) and allowing thicker physical layers. However, challenges such as interfacial layer formation, trap generation, and poor thermal stability arise when integrating high-k materials [2-4]. Among the various leakage mechanisms, trap-assisted tunneling plays a dominant role, especially in dual-layer gate stacks where traps within the dielectric facilitate carrier transport. Therefore, understanding and modeling trap-assisted tunneling in dual high-k stacks is essential for the design of low-leakage CMOS technologies.

II. Theoretical Modeling of Trap-Assisted Gate Tunneling

The electron injection into a dual-layer dielectric structure is analyzed by assuming traps at a single energy level (φt) below the conduction band of the high-k material. The overall gate current density (Jg) depends on applied bias, trap density (Nt), dielectric thickness, and effective masses. The potential drops across SiO_2 and high-k layers are calculated using voltage division, and tunneling probabilities are obtained using the Wentzel–Kramers–Brillouin (WKB) approximation. Trap-assisted current is modeled as a two-step process involving electron capture by traps followed by emission into the conduction band of the high-k material. The effect of traps is incorporated into the total tunneling current using analytical equations validated with previously reported data [5].

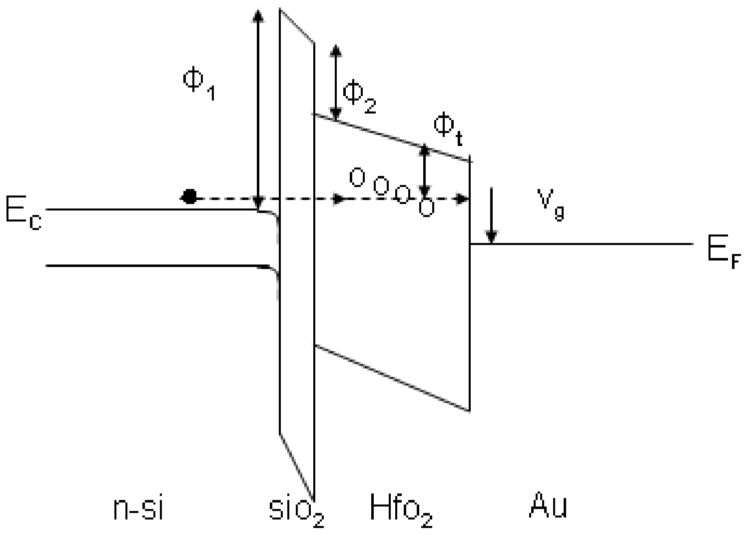

Fig. 3.1 Energy band diagram of the n-Si/SiO_2/HfO_2/Au system illustrating the trap-assisted tunneling mechanism in HfO_2 layer.

The band diagram shown in Fig. 3.1 represents the dual dielectric stack, where traps located within the high-k layer provide an intermediate energy level for electrons to tunnel through.

The gate current density for this structure is given by [6]

$$J_G(V,T) = C\int_0^{x_m} \frac{T_{ox}(V)T_{hk}(V,x)(qV)^{3/2}}{1+\exp(qV/k_BT)}dx \qquad (1)$$

Where $C = \frac{8q}{3\hbar}\left(\frac{m_s}{m_{ox}}\right)^{5/2}\frac{N_t}{\phi_1^{1/2}}$ (2)

$$x_m = \frac{(\phi_1-\phi_2-\phi_t-qV_{ox})}{qV_{hk}}t_{hk} \qquad (3)$$

And $qV = \phi_1-\phi_2-\phi_t-qV_{ox}-(qV_{hk}/t_{hk})x$ (4)

In the above equations, m_s and m_{ox} are the effective masses of the electron in the Si substrate and the SiO_2 layer respectively, N_t is the trap density, V_{ox} and V_{hk} are the voltages across the SiO_2 and high-K gate dielectric layer respectively, t_{hk} the thickness of the high-K gate dielectric layer; T_{ox} and T_{hk} are the direct tunneling transmission probabilities in the SiO_2 and high-K gate dielectric layer respectively.

$$T_{ox}(V) = \exp\left(-\frac{4\sqrt{2m_{ox}}}{3\hbar q V_{ox}} t_{ox} \left[(\phi_1 - qV)^{3/2} - (\phi_1 - qV - qV_{ox})^{3/2} \right] \right) \qquad (5)$$

$$T_{hk}(V,x) = \exp\left(-\frac{4\sqrt{2m_{hk}}}{3\hbar q V_{hk}} t_{hk} \left[(\phi_t + q\frac{V_{hk}}{t_{hk}} x)^{3/2} - \phi_t^{3/2} \right] \right) \qquad (6)$$

When the device is biased, electrons from the silicon substrate tunnel into the traps within HfO_2 and are subsequently emitted toward the gate. This two-step process enhances the tunneling probability, especially at low gate voltages, compared to direct tunneling through SiO_2 alone. The presence of these traps leads to an increased leakage current that depends on trap energy level and density [7-8].

III. Results and Discussion

The analysis of trap-assisted gate tunneling and interfacial effects has been carried out for dual-layer gate stacks consisting of SiO_2 combined with high-k materials (HfO_2, ZrO_2, and Si_3N_4). The simulation results which illustrate the variation in gate current density, trap effects, temperature dependence, and interfacial layer thickness are discussed below.

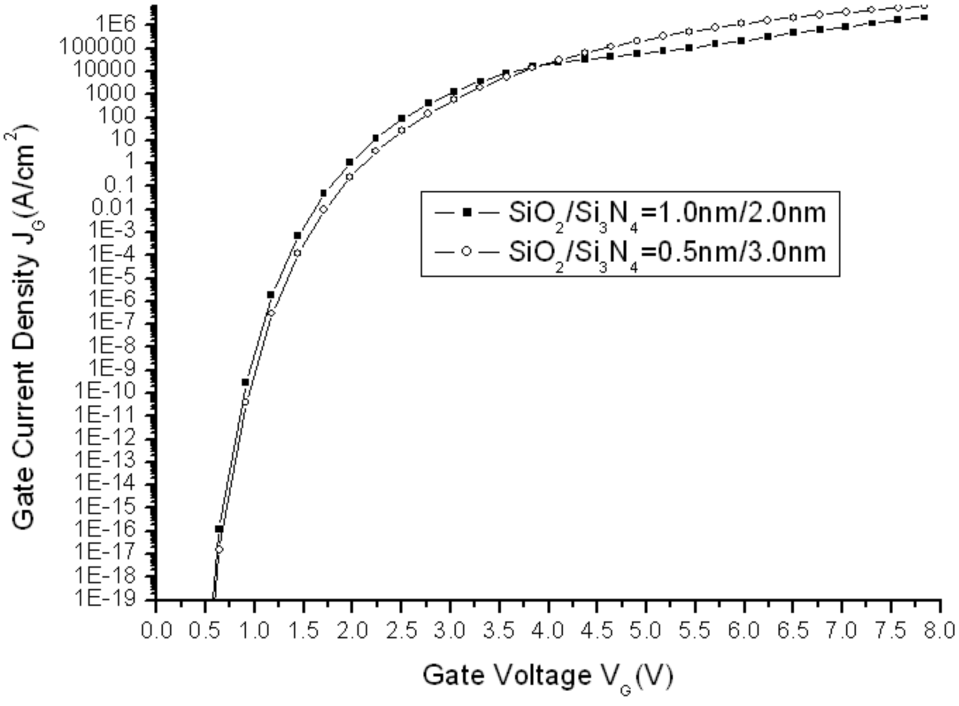

Fig. 3.2 Gate current density with gate voltage for the variation of interfacial layer thickness for same EOT = 2.0 nm.

Fig. 3.2 demonstrates that decreasing the interfacial SiO_2 layer thickness leads to reduced leakage at lower voltages, due to increased high-k thickness for the same EOT. For thicker interfacial layers, leakage becomes relatively insensitive to voltage changes, but overall current is higher due to lower capacitance.

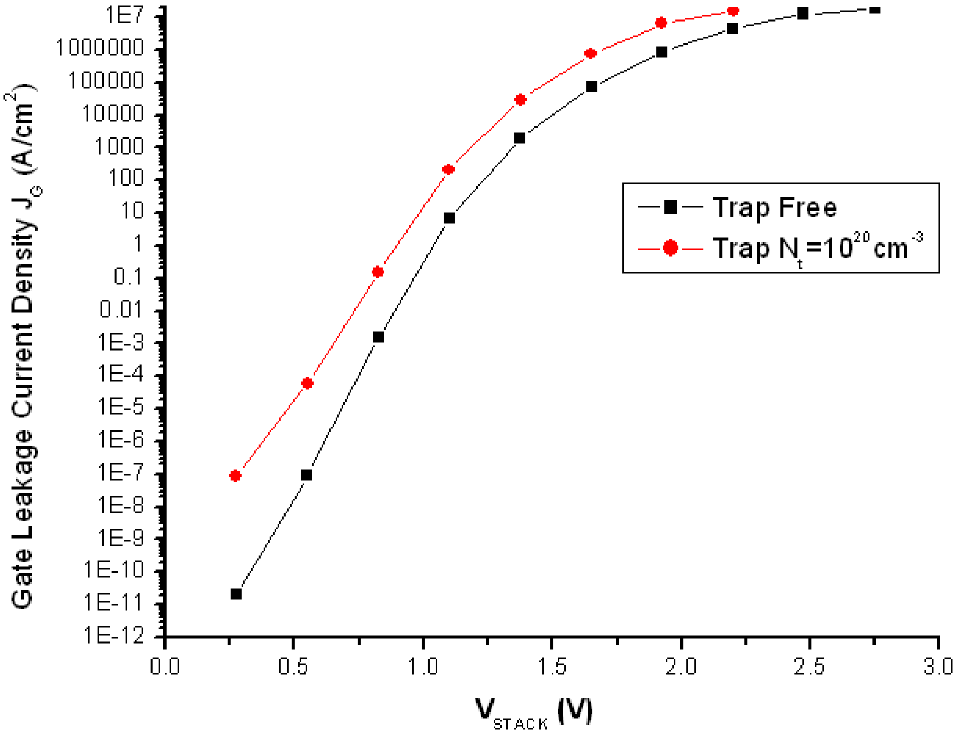

Fig. 3.3 Comparison of trap-assisted and trap-free gate tunneling current for SiO_2/HfO_2 dual stack structure.

Fig. 3.3 highlights that the trap-assisted current is consistently higher than trap-free tunneling. This occurs because trap states introduce intermediate energy levels within the dielectric, enabling a two-step conduction process — electron capture into traps followed by emission toward the gate. These localized states shorten the effective tunneling barrier, leading to greater current even at modest voltages. The slope of the I–V curve for the trap-assisted case is also smoother, indicating distributed trap participation across the oxide depth. As traps become active, they modify the local electric field, further enhancing conduction. The dominance of this mechanism underlines the importance of trap control during high-k film growth and annealing. If not minimized, trap-assisted leakage can degrade subthreshold behavior, increase standby power, and accelerate time-dependent dielectric breakdown.

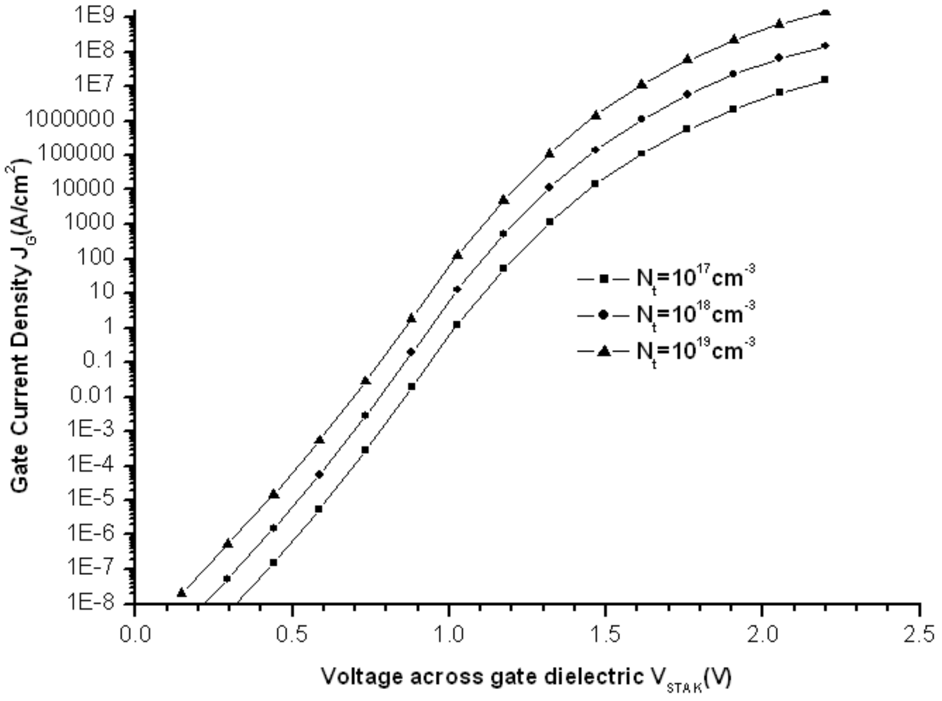

Fig. 3.4 Effect of trap density in SiO_2/HfO_2 dual structure for 2.0 nm EOT at constant trap level energy = 0.2 eV.

The impact of trap density (N_t) on gate leakage is shown in Fig. 3.4. An increase in N_t results in higher gate current because more trap sites are available for electron tunneling. The effect is more pronounced at moderate to high gate voltages.

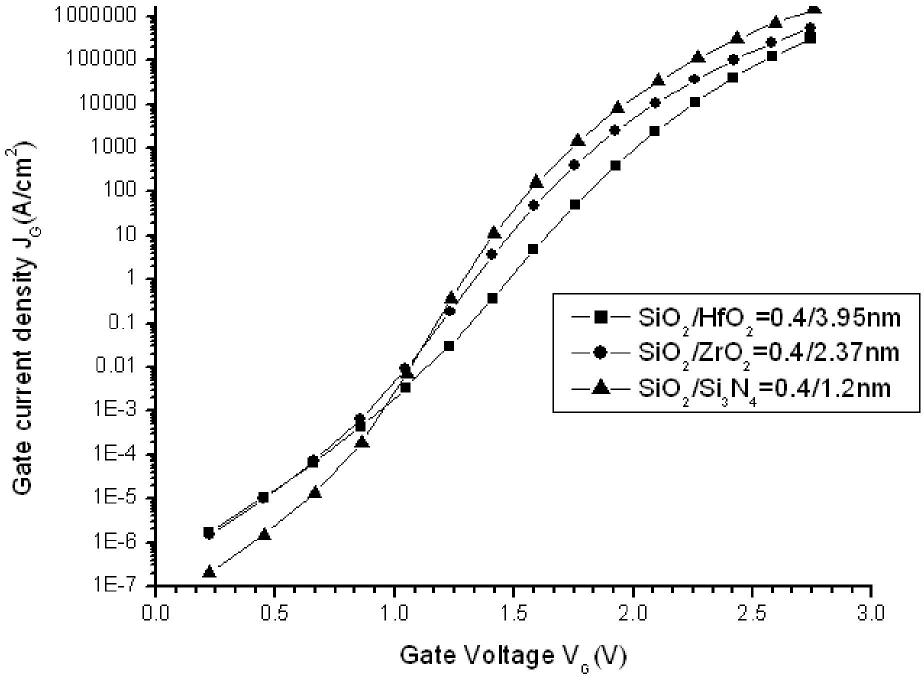

Fig. 3.5 Variation of gate leakage current with gate voltage across various dual structures for trap-assisted model.

Fig. 3.5 shows the variation of gate leakage current with gate voltage across various dual structures for trap-assisted model. From this figure it is clear that HfO_2 again shows lower leakage compared to Si_3N_4 due to its larger dielectric constant and favorable energy alignment. The SiO_2/HfO_2 structure, however, exhibits relatively stable behavior with lower leakage despite increased trap density, indicating its robustness. In contrast, SiO_2/ZrO_2 shows greater sensitivity to trap-induced leakage.

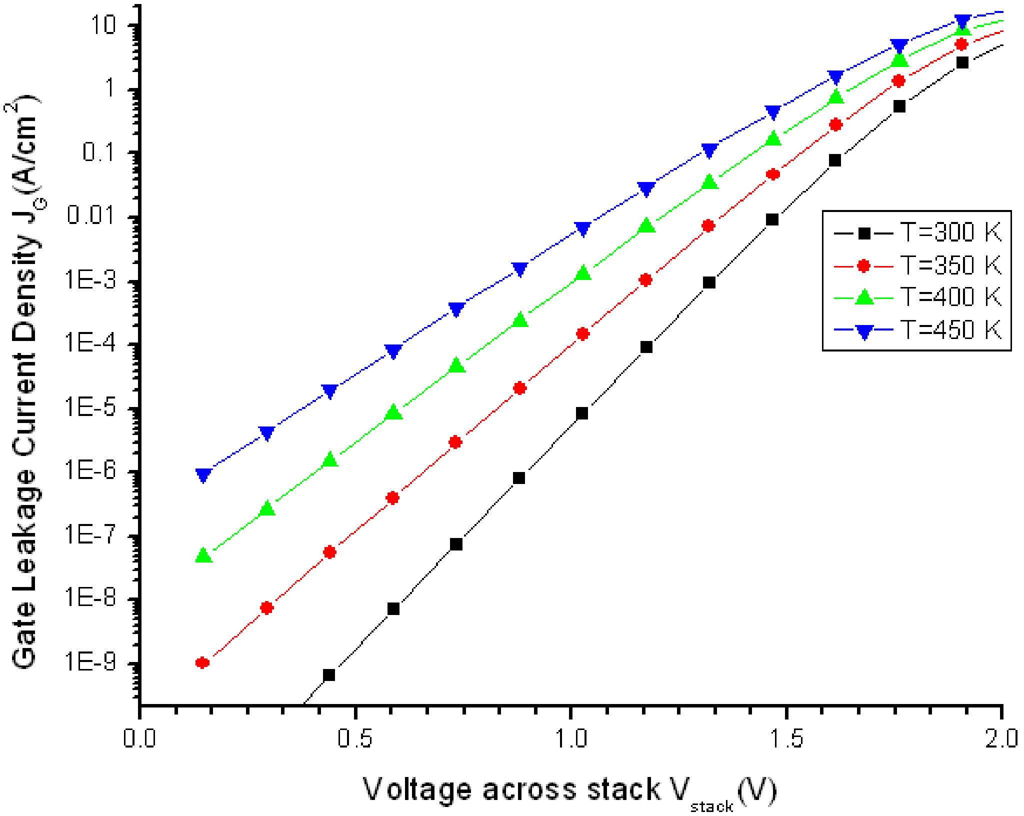

Fig. 3.6 Effect of temperature on trap-assisted gate tunneling current in dual-layer ZrO_2/SiO_2 structure.

The temperature dependence of trap-assisted tunneling is analyzed in Fig.3.6. As the temperature increases from 300 K to 450 K, the gate leakage current rises due to enhanced carrier energy and reduced potential barriers. This behavior is consistent with the theoretical prediction from the tunneling model. The study concludes that HfO_2-based dual-layer dielectrics are more suitable for high-performance applications where thermal effects can otherwise cause reliability degradation.

IV. Conclusion

A comprehensive analytical investigation of trap-assisted gate tunneling in high-k dual-layer structures has been presented. The study highlights the crucial role of interfacial oxide thickness, trap density, and temperature in determining gate leakage behavior. The comparison between trap-assisted and trap-free tunneling clearly shows that traps accelerate current conduction through the gate stack, underlining the importance of minimizing trap formation during high-k deposition and annealing processes. The results confirm that the SiO_2/HfO_2 structure provides superior leakage suppression and temperature resilience compared to other dual dielectrics. These findings support its potential as an optimal gate stack for sub-45 nm CMOS nodes.

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