

All-Optical Fredkin Gate using Semiconductor Optical Amplifier assisted Mach-Zehnder Interferometer

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Abstract: Reversible logic becomes immense important in the field of computation. Reversible circuits are those circuits that do not lose information. A system capable of reversible computation consists of reversible gates. Irreversible hardware computation results in energy dissipation due to information loss. Reversible logic supports the process of running the system in both forward and backward directions. This means that reversible computations can generate inputs from outputs and can stop and go back to any point in the computation history. This chapter presents an optical circuit for realization of Reversible Logic Gate in all-optical domain. Simulation has been done with Mathcad-7.

IndexTerms— Reversible Logic, Irreversible hardware, all-optical (*Keywords*)

I. INTRODUCTION

A circuit is said to be reversible if there is a one-to-one correspondence between the inputs and the outputs. Thus, any reversible gate has the same number of input and output lines, and it implements a permutation from input values to output values. Neither feedback nor fan-out is allowed in reversible logic [1-5]. Consequently, synthesis of reversible logic is different from irreversible logic synthesis. One of the major constraints in reversible logic is to minimize the number of reversible gates used and garbage outputs produced. Garbage output refers to the output that is not used for further computations. Semiconductor optical amplifier (SOA) based MZI can play a significant role in this field of ultrafast all-optical signal processing. These circuits can generate unique output vector from each input vector, and vice versa, that is, there is a one-to-one mapping between input and output vectors. The classical set of gates such as AND, OR, and EXOR are not reversible as they are all multiple-input single output logic gates. Therefore, a reversible gate's inputs can be uniquely determined from its outputs. Reversible logic gates must have an equal number of inputs and outputs, inputs can be uniquely determined from its outputs unlike conventional gates. The output that is not used for further computations is called garbage output.

Reversible logic supports the process of running the system in both forward and backward directions. This means that reversible computations can generate inputs from outputs and can stop and go back to any point in the computation history. Thus, reversible logic circuits offer an alternative that allows computation with arbitrarily small energy dissipation. Furthermore, reversible circuits are of major interest in optical computing, low power design, quantum computing and nanotechnology based systems. It is not possible to realize quantum computing without reversible logic. Reversible computation in a system can be performed if the system is composed of reversible gates [6-11].

II. METHODOLOGY: MACH-ZEHNDER INTERFEROMETER (MZI) AS AN OPTICAL SWITCH

A Mach-Zehnder interferometer (MZI) switch is a very powerful technique to realize ultrafast switching. The block diagram of a Symmetric SOA-assisted MZI switch is shown in Fig. 1. In this switch two SOAs (SOA-1 and SOA-2) are inserted in each arm of a MZI [7-14]. It has two input ports (port-1 and port-2) and two output ports (port-3 and port-4). The incoming signal pulse at the wavelength λ_2 enters port-1, is split equally by coupler C1 (50:50) and propagates simultaneously in the two arms of the interferometer. At the same time, pulsed signal at the wavelength λ_1 enters to the upper arm, through coupler C2 (90:10) such that

most power passes through upper arm. It saturates the SOA-1 and changes its index of refraction, while the SOA-2 gets the unsaturated gain. As a result, a differential phase shift can be achieved between the data signal of two arms. Hence, light is present in the bar port (port-3), as shown in Fig. 1. In this case no light is present in the cross port (port-4), this is called the ‘switched state’. In ‘no-switched state’, when control signal is absent, both SOAs (SOA-1 and SOA-2) get the same unsaturated gain. In this case no light is present in the bar port (port-3), then light is present in the cross port (port-4). Optical filters (F) are placed in front of the output ports for blocking the λ_1 signal (control signal). The MZI scheme is preferable over cross-gain saturation as it does not reverse the bit pattern and results in a higher ON–OFF contrast simply because nothing exits from bar port during 0 bits. Now, it is clear that in the absence of control signal, the signal exits through the cross port (port-4) of MZI as shown in Fig. 4. In this case no light is present in the bar port (port-3). But in the presence of control signal, the incoming signal exits through the bar port of the MZI as shown in Fig. 2. In this case no light is present in the cross port. In the absence of incoming signal, the bar port and cross port receive no light as the filter blocks the control signal. Schematic block diagram of MZI is shown in Fig. 2.

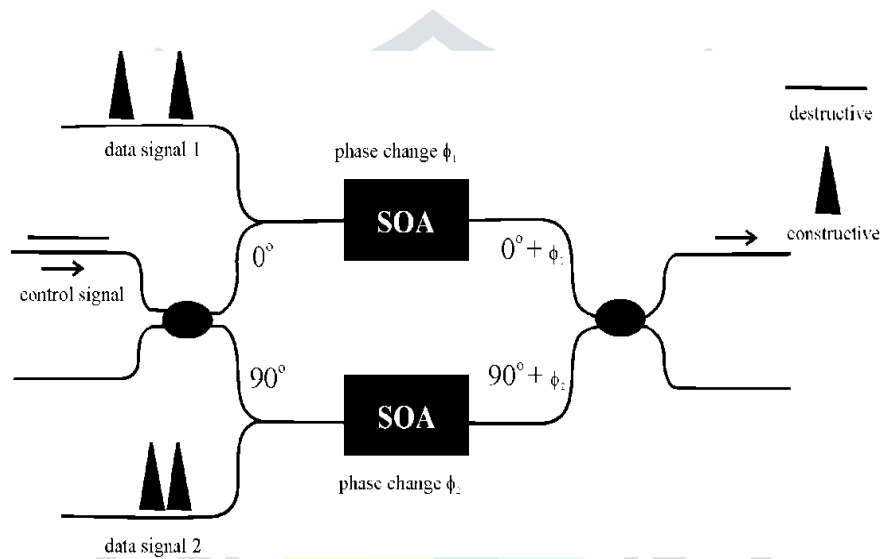


Fig. 1: SOA based MZI optical switch

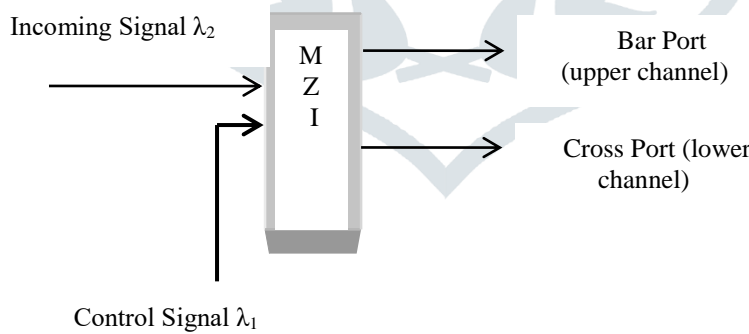


Fig. 2: Schematic diagram of SOA based MZI optical switch

III. MZI-BASED RFREDKIN GATE: PRINCIPLE AND DESIGN

Fredkin gate is a (3:3) conservative reversible gate [12-14]. The truth table of Fredkin gate is given in Table 1, which after simplification using K-map can be represented as Boolean function.

Table 1: Truth table of Fredkin Gate

| Inputs | | | Outputs | | |
|--------|---|---|---------|---|---|
| A | B | C | X | Y | Z |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 |

Fredkin Gate has three inputs (A, B, C) and three outputs (X, Y, Z) and they satisfy the relation as follows:

$$\begin{aligned}
 X &= A \\
 Y &= \bar{A}.B + A.C \\
 Z &= A.B + \bar{A}.C
 \end{aligned}
 \tag{1}$$

The MZI based circuit for all optical reversible Fredkin gate is given in Fig. 3. Here the output X is directly taken from the input pulse A through a beam splitter (BS). Light from A incidents on beam splitter and split into two part. A part of light is passed through wavelength converter that converts the wavelength of light from λ_2 to λ_1 . Finally they are connected with MZI switches MZI-1 and MZI-2 through erbium doped fibre amplifier (EDFA) so that they can act as control signal to the switches. Other two inputs B and C are the two incoming signals of the MZI-1 and MZI-2.

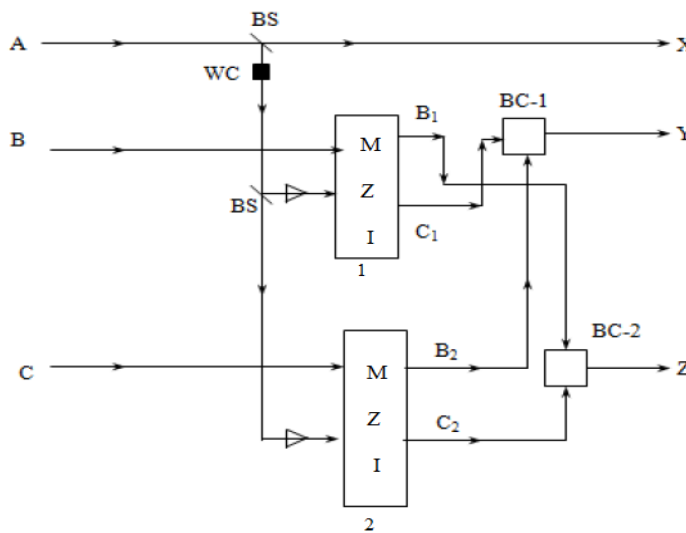


Fig. 3: Circuit for all-optical Fredkin Gate (FG).

BC: Beam Combiner EDFA: Erbium Doped Fiber Amplifier Wavelength Converter (WC)

The bar port of MZI-1 (B₁) and cross port of MZI-2 (C₂) is combined by a beam combiner BC-1 to get the output Y and also the bar port of MZI-2 (B₂) and cross port of MZI-1 (C₁) is combined by BC-2 to get the final output Z. Let us discuss the operation in details. In this paper, the presence and absence are indicated by state 1 and state 0, respectively.

Case 1: When A=B=C=0, i.e. no light is present at input, then the final outputs receives no light i.e. X=Y=Z=0.

- Case 2: When $A=B=0$ and $C=1$, according to the working principle of MZI described in the section-2, only the lower channel of MZI-2 receives the light. Hence, $C2=1$ and $B2=0$ (as the control signal of MZI-2 is 0). In this case upper and lower channel of MZI-1 receive no light (as the input signal of MZI-1 receives no light). Hence, $C1=B1=0$. Therefore $X=0, Y=1, Z=0$. It satisfies the second row of the truth Table1.
- Case 3: When $A=C=0$ and $B=1$, control signal is absent but incoming signal is present at MZI-1. So lower channel receive light and hence $B1=0$ and $C1=1$. In this case both incoming and control signal is absent in MZI-2. Therefore, $B2=C2=0$. Hence $X=Y=0, Z=1$.
- Case 4: When $A=0$ and $B=C=1$, both the MZI switches receive light in the incoming signal but receive no light at control signals. So $B1=B2=0$ and $C1=C2=1$. Hence $X=0, Y=Z=1$.
- Case 5: When $A=1$ and $B=C=0$, both the MZI receive no light as incoming signal. So $B1=B2=0$ and $C1=C2=0$. Hence $X=1, Y=Z=0$.
- Case 6: When $A=1, B=0$ and $C=1$, MZI-1 receive no light as incoming signal and MZI-2 receive light pulse in both the incoming and control signal. So $B1=C1=0$ and $B2=1, C2=0$. Hence $X=1, Y=0$ and $Z=1$.
- Case 7: When $A=1, B=1$ and $C=0$, MZI-2 receive no light as incoming input signal and MZI-1 receive light pulse as both the incoming and control signal. So $B2=C2=0$ and $B1=1, C1=0$. Hence $X=1, Y=1$ and $Z=0$.
- Case 8: When $A=1, B=1$ and $C=1$, both the MZI-1 and MZI-2 receive light pulse as incoming and control signal. So $B1=1, C1=0$ and $B2=1, C2=0$. Hence $X=1, Y=1$ and $Z=1$.

IV. PERFORMANCE EVALUATION THROUGH NUMERICAL SIMULATION

The result of simulation using Mathcad-7 is shown in Fig. 4. The power of the input pulse is taken $A=2.28$ dBm, $B=C=1.17$ dBm.

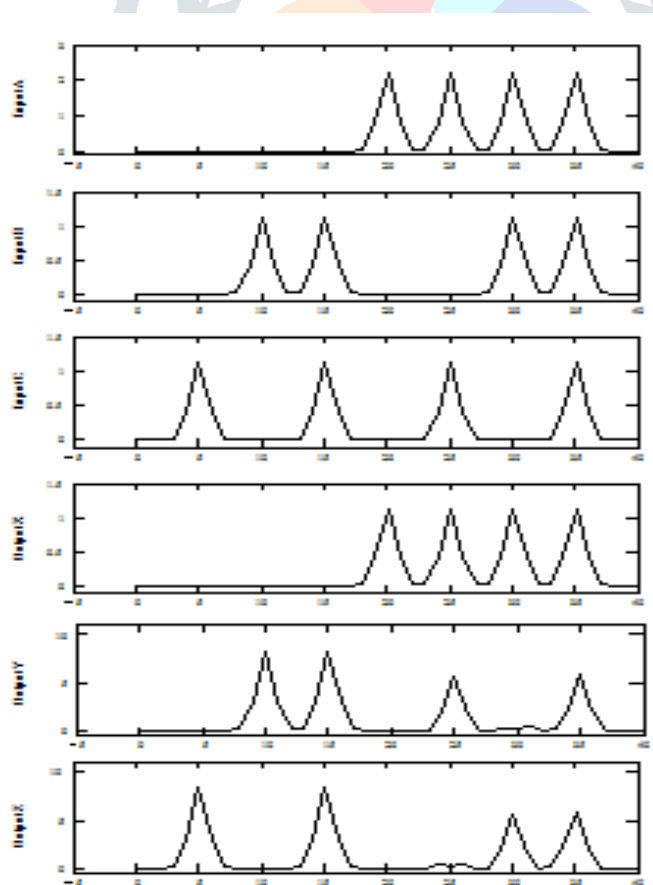


Fig. 4: Simulation result: [x- axis: Time (ps) and y-axis: Power (dBm)]

The timing instant for the occurrence of bit pattern are at 0,5,10,15,20,25,30,35 ps. Upper three set waveforms indicate the input bit sequences, 00001111, 00110011, 01010101 for the input variables A, B, C, respectively. Similarly, the lower three waveforms indicate bit sequences 00001111, 00110101, 01010011, bit pattern change of output variables X, Y, Z, respectively. Let us test the reversible operation from the simulation results with chosen arbitrary time at 15 ps. The output signals are X=0, Y=1, Z=1. Using these specific outputs we gate from equation (1), A=0, B=1 and C=1. Similarly, from different output bit patterns gives the different input bit combinations which satisfies the reversibility condition.

V. CONCLUSIONS

Reversible logic offers lossless operation of digital data processing. From this study it is obvious that MZI based optical switch is a promising device for implementation of Fredkin gate. There is enough scope for implementation of other reversible logic gates.

References

- [1] J. W. Bruce, M. A. Thornton, L. Shivakumaraiah, P. S. Kokate and X. Li, "Efficient adder circuits based on a conservative reversible logic-gate," IEEE, 83-88, 0-7695-1486-3/02, 2002.
- [2] M. Perkowski, P. Kerntopf, A. Buller, M. Chrzanowska-Jeske, A. Mishchenko, X. Song, A. Al-Rabadi, L. Jozwiak, A. Coppala and B. Massery, "Regular realization of symmetric functions using reversible logic," IEEE, 245-252, 0-7695-1239-9/01, 2001.
- [3] T. Saso and K. Kinoshita, "Conservative logic elements and their Universality," IEEE Trans. on computers, 28(9), 682-685, 1979.
- [4] J. Shamir, H. J. Caulfield, W. Micelli and R. J. Seymour, "Optical Computing and Fredkin gates," Applied Optics, 25(10), 1604-1607, 1986.
- [5] D. P. Vasudavan, P. K. Lala, J. Di and J. P. Parkerson, "Reversible –logic design with online testability," IEEE Trans. on Instrumentation and Measurement, 55(2), 406-414, 2006.
- [6] R. Landaur, "Irreversibility and heat generation in the computational process," IBM Journal or Research and Development, 5, 183-91, 1961.
- [7] C. H. Bennett, "Logical reversibility of computation," IBM Journal or Research and Development, 17, 525-32, 1973.
- [8] C. H. Bennett and D. P. DiVincenzo, "Quantum information and computation," Nature 4014, 247-55, 2000.
- [9] P. A. Picton, "Universal architecture for multi-valued reversible logic," Multiple valued Logic Journal, 5, 27-37, 2000.
- [10] H. Thapliyal and M. B. Srinivas, "A beginning in the reversible logic synthesis of sequential circuits," In: MAPLD, 1012. p. 1-5, 2005.
- [11] R. K. James, K. P. Jakob and S. Sasi, "Fast reversible binary coded decimal adders," International Journal of Electrical and Electronic Engineering, 4(3), 254-266, 2008.
- [12] M. Luke, M. Perkowski and H. Gol, "Evolutionary approach to quantum and reversible circuit synthesis," Artificial intelligence Review, 20(3-4), 361-17, 2003.
- [13] P. Zuliani, "Logic reversibility," IBM Journal of Research and Development, 45, 807-17, 2001.
- [14] E. Fredkin and T. Toffoli, "Conservative logic," International Journal of Theoretical Physics, 21(3-4), 219-53, 1982.