2-BIT MAGNITUDE COMPARATOR DESIGN USING DIFFERENT LOGIC STYLES

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ABSTRACT: 2-bit magnitude comparator is designed using different logic styles. Comparator is most fundamental component that performs comparison operation. Comparison is the most basic arithmetic operation that determines if one is greater than, lesser than or equal to the other input. The work also focuses on comparison between different logic styles used to design a 2-bit magnitude comparator. comparison between different designs is calculated by simulation that is performed using DSCH tool.

Keywords- Binary comparator, digital arithmetic, high speed, low power, DSCH.

1. INTRODUCTION

In olden days size of the electronic devices were huge, required more power dissipation, were not so reliable. So there was certainly a need to reduce the size of the devices, this led to the invention of integrated circuits. Integrated circuits are a set of transistors on one single chip of semiconducting material. The transistor was introduced by William B Shockley Walter H. The very first IC emerged at the beginning of 1960.

The invention of these integrated circuits is classified based on number of transistors embedded on a single chip.

The first level of integration is SSI's where in which number of active devices per chip is less than 100 followed by MSI which ranges from 100 to 10000 active devices per chip the third level of integration is LSI which varies from 1000 to 100000 then comes the VLSI(very large scale integrated circuits) where over 100000 active devices per chip and in ULSI more than 1 million active devices per chip.

Nowadays fast growing electronic industry is pushing towards low powered comparators due to its simple circuit and low power consumption compared to other logic families with resistive loads. The high speed devices like ADC and operational amplifiers are of greater importance and for its high speed application a major thrust is given towards low power methodologies. This high speed low power comparators is required to satisfy future demands.

Comparators are mainly used in the addressing decoding circuitry in computers and microprocessor based device such as temperature, position values are compared with reference value than the outputs from the comparators are used to drive the actuators so as to make the physical variables closest to the set of reference value. they are also used in servomotor control and process controllers. The present work is about designing of a 2-bit magnitude comparator using CMOS, PTL logic style using which comparison of two inputs is done to determine if one input is greater than, less than ,or equal to other. The block diagram is shown in figure 1.

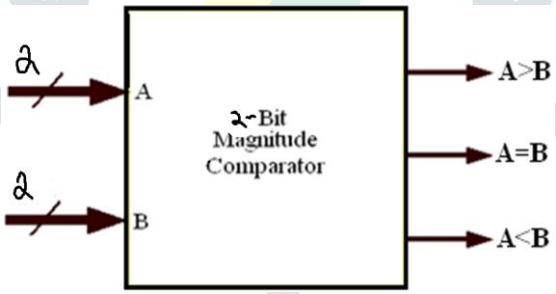


Figure1: Block diagram of 2-bit magnitude comparator

Block diagram has two input terminals V+ and V- and one binary digital output(0 or1) V0.A 2 bit magnitude comparator compares two numbers each having 2 bits(A1,A0 & B1,B0). Therefore it has 4 inputs and 16 entries from this input and output lines truth table figure 2 is written and K's maps are constructed to minimize Boolean function obtained from truth table. From these logic functions logic diagram will be drawn in a compact and efficient way with below mentioned logic design. The logic style used in logic gates basically influences the speed, size, power dissipation, and the wiring complexity of a circuit. Circuit size depends on the number of transistors and their sizes and on the wiring complexity. The wiring complexity is determined by the number of connections and their lengths. All these characteristics may vary considerably from one logic style to another and thus proper choice of logic style is very important for circuit performance. In order to differentiate designs, simulations are carried out for power.

1.2 DSCH

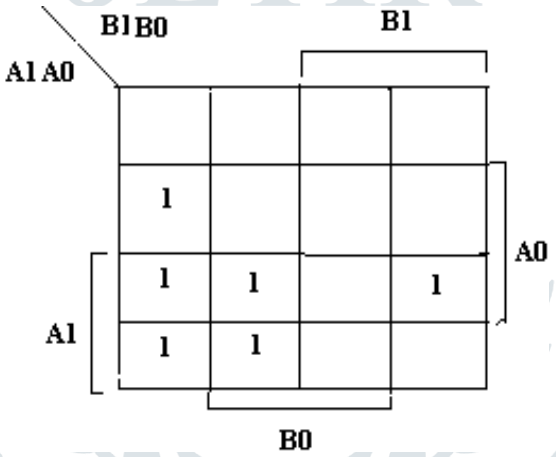
It is a logic editor and simulator. It provides a friendly environment for hierarchical logic design. The main advantage of software is its fast simulation with delay analysis. It is used to validac the architecture of the logic circuit before micro- electronics is started.

A1	A0	B1	B0	A>B	A=B	A<B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

Figure 2

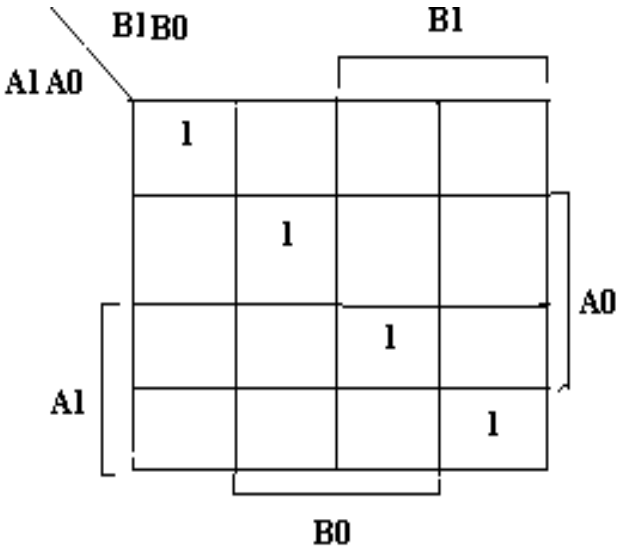
K Map for A>B

A1B1'+A0BO'(X1)



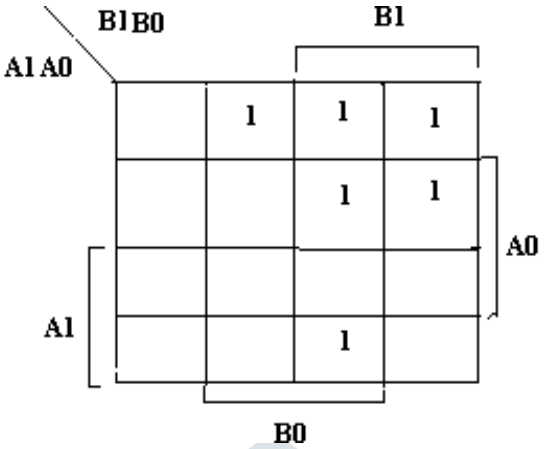
(A1'B1'+A1B1)(A0'B0'+A0B0)

K Map for A=B



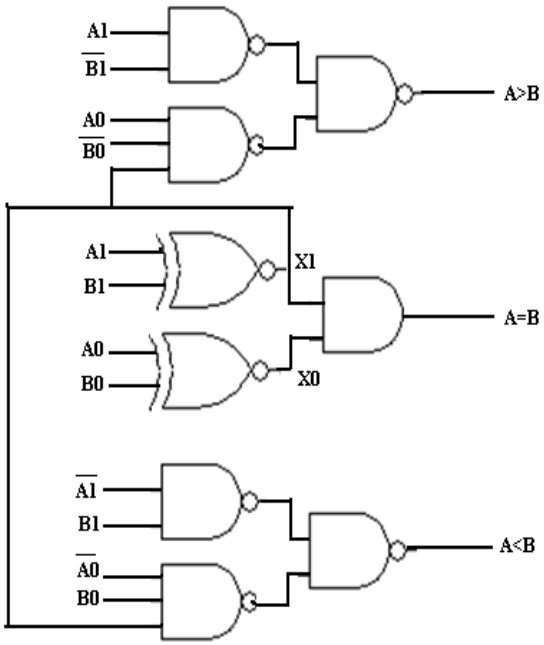
K map for A<B

A1’B1+A0’B0X1

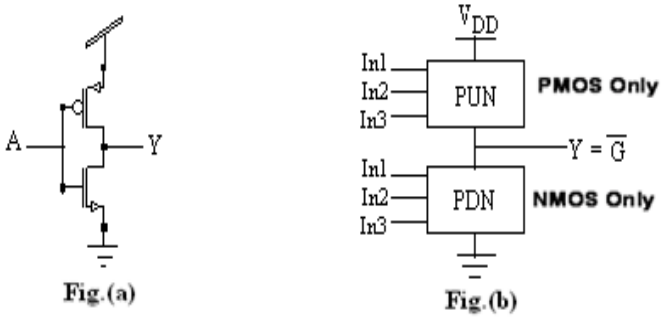


From these K Maps the equations which are obtained according to that a logic diagram is proposed as shown below.

2. PROPOSED CIRCUIT

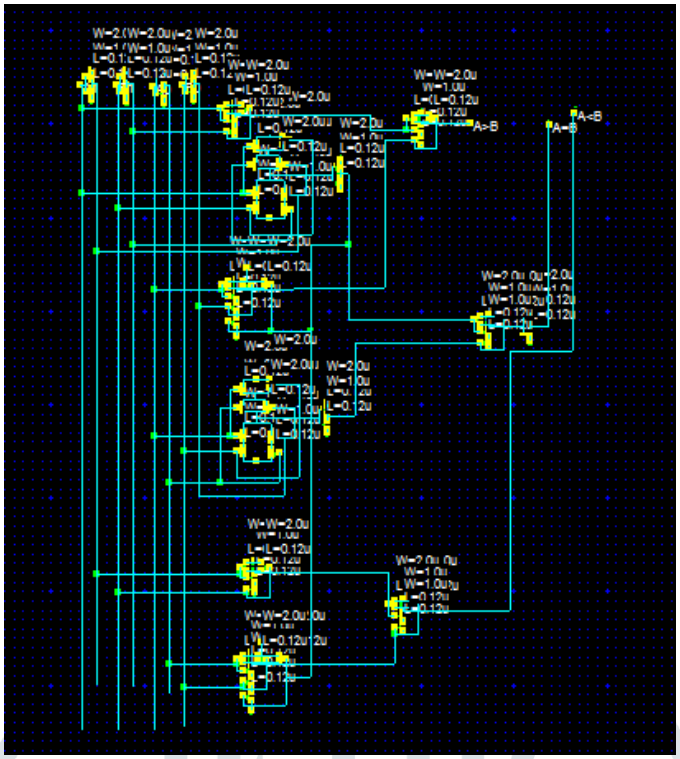


3. CMOS LOGIC STYLE



(a)Symbol of CMOS Inverter (b) Logic Network of CMOS Style

The figure above represents symbol of CMOS inverter it consists of one NMOS and one PMOS transistor. If input A=0(logic low) then both gates are at zero potential and PMOS is on and provide low impedance path from VDD to output (Y). Therefore output Y approaches to high level of VDD. If input A=1 (logic high) then both gates are at high potential but NMOS is ON and provide low impedance path between ground and output. Therefore, output Y approaches to low level of zero volt. The substrate for the NMOS is always connected to ground, while the substrate for the PMOS always connected to VDD.



Advantages

1. Design provides full output voltage swing between 0 and VDD.
2. It provides high noise immunity because it has low sensitivity to noise.

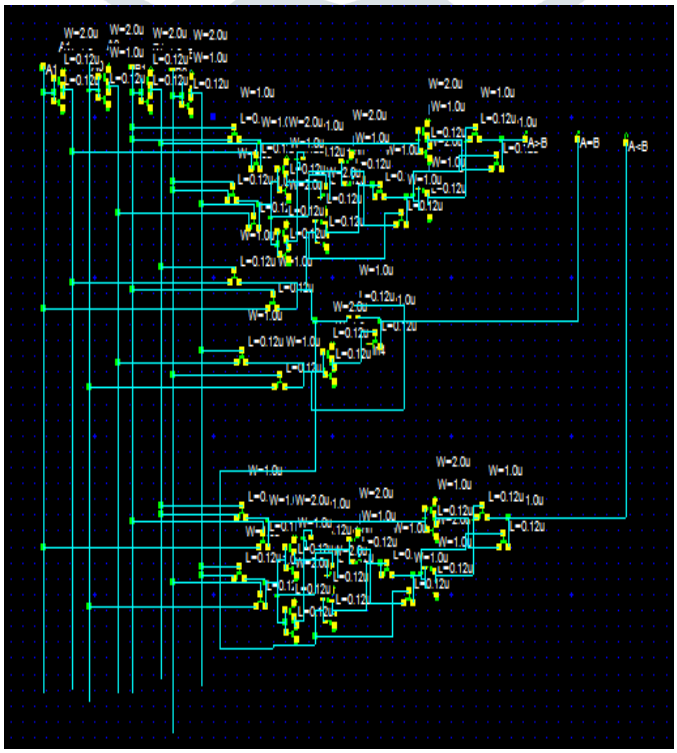
Disadvantages

1. Design produces Large Power dissipation in comparison to other logics
2. Design requires large number of transistor.

4. PASS TRANSISTOR LOGIC

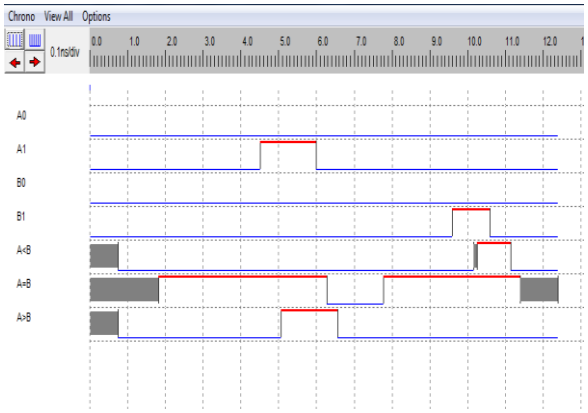
A popular and widely used alternative to complementary CMOS is pass transistor logic. Pass transistor logic attempts to reduce the number of transistors required to implement logic by allowing the primary inputs to drive gate terminals as well as source/drain terminals. The potential advantage of pass transistor is that a fewer number of transistors are required to implement a given function. Pass transistor logic uses fewer devices and therefore has lower physical capacitance.

Unfortunately, in pass transistor logic, the pass transistors are used to pass high and low voltages. Therefore, when the pass transistor pulls a node high, the output only charges up to VDD. The devices experience body effect since there is a significant source to body voltage when pulling high since the body is tied to GND and the source charge up close to VDD. The pass transistor is charging up a node to VDD where the gate and drain terminals are set at VDD.



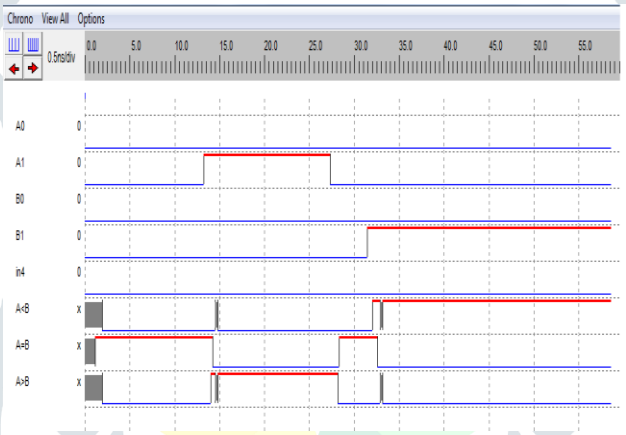
5.RESULTS & DISCUSSIONS

5.1 TIMING DIAGRAM OF CMOS



From the above timing diagram of Comparator designed in CMOS logic style we can see that when the input given are logic low (0) according to the operation of comparator the output of comparator should be zero as shown in the waveform. When the input line A1 was logic high the output line A>B is high and next when input line B1 was made logic high the output line A<B is high.

5.2 TIMING DIAGRAM OF PTL



From the above timing diagram of Comparator designed in PTL logic style we can see that when the input given are logic low (0) according to the operation of comparator the output of comparator should be zero as shown in the waveform. When the input line A1 was logic high the output line A>B is high and next when input line B1 was made logic high the output line A<B is high.

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