DESIGN OF FOLDED CASCODE OPERATIONAL AMPLIFIER USING 1.8MICRON CMOS TECHNOLOGY

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Abstract— This paper presents the design and simulation of Low Voltage Folded Cascode CMOS Operational Amplifier using gpdk 0.18µM CMOS technology. The proposed op-amp consists of pair of NMOS transistors as an input differential gain stage, the NMOS differential pair is chosen for low power consumption and also to maintain good UGF. The design is simulated using cadence spectre simulator, under ±1V supply voltage. The proposed design shows 68.6dB gain, Phase margin of 50^0, UGF of 13.1MHz, with power consumption of 30µW.

IndexTerms—Folded Cascode Operational Amplifier, Op-Amp, 180nM CMOS Op-Amp.

I. INTRODUCTION (HEADING 1)

Operational amplifier is an integral part of analog and mixed signal system. The design of high-performance op-amp has always been one of the hot spots of analog integrated circuit design as its performance directly affects the overall performance of circuits and system. Hence, proper design of the op-amp is necessary according to the application where it is needed. With the continuous development of integrated circuit technology, high-performance op-amp is widely used in high-speed ADC, DAC, switched capacitor filter, band-gap voltage reference circuits, LDO regulators, precision comparators and other electronic devices [1].

The folded cascode Operational-Amplifier is a single stage Op-amp, which consists of a common source configured transistor in cascoded & opposite polarity with a common gate transistor. In this type of amplifier implementation, a differential pair is used as the input stage to the amplifier, acting as the common source portion of the cascade. The drains of the input transistors are then linked to two opposite polarity common gate transistors. The common gate transistors are then connected to an active current source load to complete the circuit. The goal of using this topology is to achieve the simplicity and small size of a single stage amplifier, while achieving the gain of a multi-stage amplifier. By "folding" the cascode over into a pair of opposite polarity transistors, this decreases the required headroom for the circuit, giving the same performance as a typical cascode amplifier, but with a lower required supply voltage. The cascoded transistors in this design serve to increase the output resistance of the circuit, which increases the small signal gain of the amplifier. This is the main benefit of the topology. Since the current mirror's output resistance appears in parallel with the output resistance of the amplifying portion of the circuit, it is important that the current source be cascoded as well, so as not to extinguish all of the benefits that were gained by the cascode in the first place[2].

In general most commonly used op-amp topology is two stage CMOS op-amp with NMOS differential pair or PMOS differential pair but among all the topologies each topology has its own application such as folded cascode op-amp has better high frequency Power Supply Rejection Ratio (PSRR), The power consumption of this design is approximately same as that of the two-stage design, Compared to the telescopic topology they have less gain and speed and dissipate more power. But they have found their place in a wide range of applications due to their larger output swing and their extended input CM level range, the main part of the folded cascode operational-amplifier is its differential pair which acts as an input stage, so proper matching is important. The proposed op-amp consists of NMOS transistors as a input differential gain stage, the NMOS differential pair is chosen for low power consumption and also to maintain good UGF and better PSSR.

Generally an op-amp consists of a differential pair in the first stage and a common source in the second stage so as to increase the overall gain of op-amp. But this requires an additional capacitance for the frequency compensation. Moreover, additional capacitance introduces a second pole in the amplifier system. The proposed design shown here is set to achieve overall gain in the first stage [2]. The advantages and disadvantages of this topology are:

Advantages:

1) This design has corresponding superior frequency response than two – stage operational Amplifiers.
2) It has better high frequency Power Supply Rejection Ratio (PSRR).
3) The power consumption of this design is approximately the same as that of the two-stage design.

Disadvantages:

1) Folded cascode has two extra current legs, and thus for a given settling requirement, they will double the power dissipation.
2) The folded cascode stage also has more devices, which contribute significant input Referred thermal noise to the signal.

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II. FOLDED CASCODE OP-AMP

Most difficult part and challenging task for a designer in the op-amp design was optimization of NMOS and PMOS transistors optimal dimensions such as widths and lengths for proper operation and also finding different gains, maintaining the tradeoffs, finding currents in all the branches of the selected topology. The transistor level circuit diagram of proposed folded cascode operational amplifier is given by:

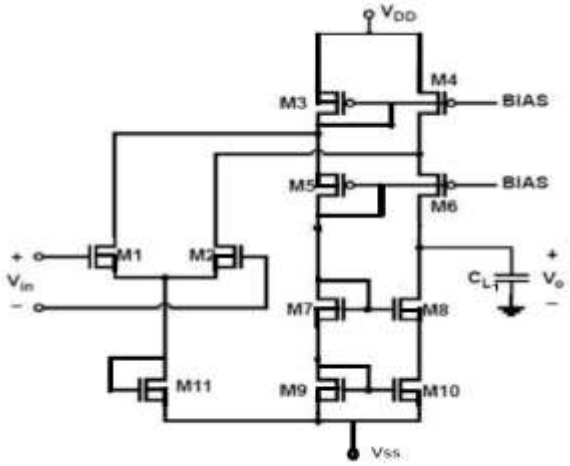

Figure 1: Transistor level circuit diagram of Folded Cascode Operational Amplifier

In the above circuit it consists of a common source configured transistor in cascoded and opposite polarity with a common gate transistor. NMOS differential pair is used as the input stage to the amplifier, acting as the common source portion of the cascade. The drains of the input transistors are then linked to two opposite polarity common gate transistors. The common gate transistors are then connected to an active current source load to complete the circuit.

III. DESIGN SPECIFICATIONS AND OBTAINED RESULTS

Considered W/L values of the proposed folded cascode op-amp are

Table 1 Transistor Dimensions

Transistor	Considered Values for simulation	
	W	L
M1	0.70	1.11
M2	0.70	1.11
M11	1.25	1.07
M3	0.98	0.56
M4	0.98	0.56
M5	0.57	1.14
M6	0.57	1.14
M7	1.34	1.05
M8	0.94	0.99
M9	0.94	0.99
M10	0.94	0.99

The simulation setup of folded cascod op-amp is

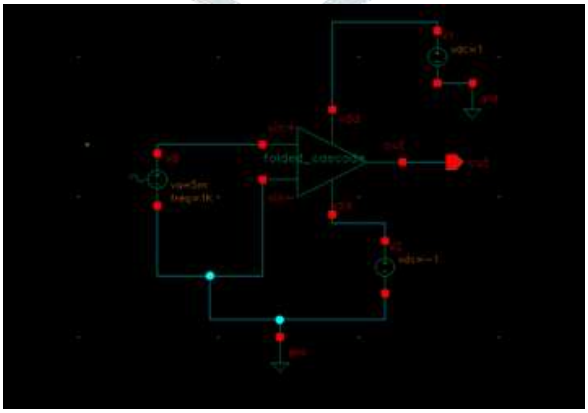

Figure 2: Test setup of folded cascode op-amp in cadence

The transient response of the above circuit is

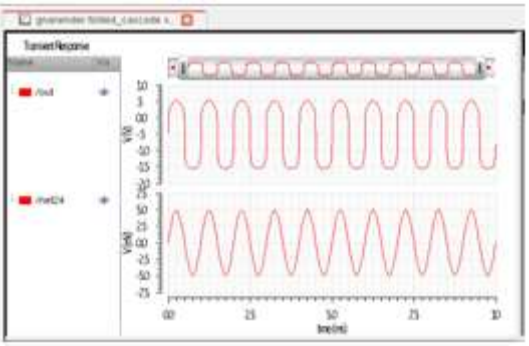

Figure 3: Transient Response

IV. SIMULATED RESULTS COMPARISON WITH OTHER PUBLISHED RESULTS

The simulation results and comparison with previously published results are as follows:

Table 1: Comparison of the results

Parameter	Paper[1]	Paper[3]	This work
Technology	180nM	130nM	180nM
Power Supply	1.8V	1.8V	1V
C_L	2pF	1pF	1pF
Gain	72.04dB	62.69dB	68.6 dB
Phase Margin	62.46^0	68.38^0	50^0
UGF	13.3MHz	133.1MHz	13MHz
Power Consumption	0.13mW	0.3mW	30µW

V. CONCLUSION

In this paper the design and simulation of folded cascode operational amplifier has been presented. This op amp structure is used for many applications such as data converters ADCs / DACs, Buffers, LDOs etc., results shows that this op amp exhibits good tradeoff between the output specifications like high DC gain, UGF, PM and Power consumption. The simulated values for the designed folded cascode op-amp is DC gain is 68.6dB, Phase margin of 50^0, UGF of 13.1MHz, and power consumption of 30µW. The designed op amp fulfills all the other requirements with a good margin to be used in data converter applications.

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