

DESIGN AND PERFORMANCE ANALYSIS OF CMOS BASED RING OSCILLATOR

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Abstract : *The more we are heading towards the future the demand for low power and small size of electronic devices is growing rapidly. CMOS (complementary metal oxide semiconductor) integrated circuits are the digital flourishing technology for the modern information era. Ring oscillator find perspective applications in biomedical devices, RFID tags and wireless sensor networks. In this paper CMOS based 7 stage ring oscillator has been designed and simulated by using LT spice for various parameters such as power consumption, frequency and delay.*

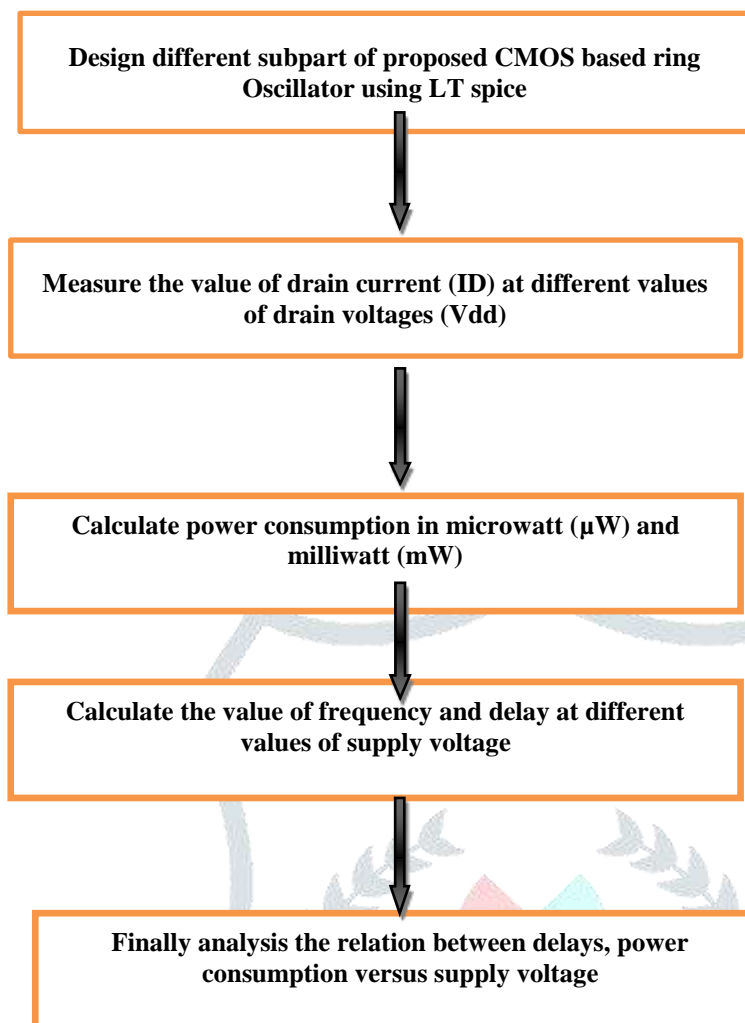
Index Terms - *Complementary metal oxide semiconductor (CMOS), Radio frequency identification (RFID), Ring Oscillator.*

I. INTRODUCTION

An oscillator is a device which operates without any external signal and gives the output that is continuous in nature means repeated pattern like alternating waveform. The unidirectional current likewise the D.C signal is transforms into the A.C signal have a need of frequency by the oscillators (Mandal M.K and Sarkar, 2010), moreover the production is depends upon components of circuits. Oscillating signals are seen in all distinct varieties of electrical systems. The synchronization function is required in digitally operated electronic systems and this condition is fulfilled by using oscillating signal produced by oscillators as clock signal (Bako N. and Baric A., 2013). The oscillatory signals can also be utilized in radio and communication systems. Electronic oscillators are manufactured in order to produce these signals. Linear/harmonic and nonlinear/relaxation are two main category of oscillators (Sikarwar V. et al, 2013). A ring oscillator is device comprise of odd number of NOT gates, the gates between their outputs two different voltage levels represent logic 1 and logic 0 (Shivhare A. and Gupta M.K, 2016). The NOT gates or inverters are attached in a series and the last inverter's output is observed from the initial gate. There is no difference between sole ended ring oscillator and the digital oscillator, produce by tumble of odd, n number of CMOS inverter in a ring (Sikarwar V. et al, 2013). To produce the specific output, the system is comprised of peculiar number of stages, which otherwise cannot be attained through by the usage of even number of stages. In this circuit, sustainable CMOS inverter stages having 'T' delay are used in ring oscillators, and provides the oscillation frequency as:

$$F = \frac{1}{2 * N * T} \quad (1)$$

In comparison to LC & RC oscillators, Wien bridge oscillator, the ring oscillators proved to be the closely packed device (Masten H.). The ring oscillator is advantageous in form of: covering minute space, having high speed and easily designable along with integrated circuit technology(IC) (Khatoon, F., et al, 2014). At the low voltage the oscillations are generated by ring oscillator, and low power is dissipated in order to produce high frequency oscillations. It can be electrically tuned and immense tuning range is provided. Because of there simplistic structure the multiphase outputs are provided (Bako N. and Baric A., 2013). To measure the voltage and temperature on a chip the application of ring oscillator is used. The ring oscillators prove to be useful in hardware irregular number generators. The jitter of the ring oscillator in the hardware irregular number generator is commonly used (Hajimiri A. et al 1999). It is used as a part of PLL for clock and data recovery, clock synchronization and frequency synthesis. A ring oscillator has digital as well as analog features which make them functional for data conversion tasks such as phase and phase width modulation. It used in biomedical circuits and systems, Radio frequency identification tags in addition to wireless sensor able networks (Nayak et al, 2017). In ring oscillator CMOS inverter is used. The function of inverter is the computation of its input to the logical NOT and it is analyzed that when inverters are connected in odd numbers then the last obtained output is same as the output of the initial inverter (Sikarwar V. et al, 2013). The span of time remain finite between the period when the introductory input is asserted and the ultimate output is obtained, in addition to this oscillations are caused when a part of the final output signal is fed back to the input signal (Hajimiri A. et al 1999). In case, when the even number of inverters are connected for designing the ring oscillators, the output attained at last stage is similar to that of initial stage input, so it is not feasible to design the oscillator with even number of stages. There are two frequent methods used for prompting the oscillation's frequency (Michal, V., 2012). First of all, the applied voltage can be increased which consequently increment the oscillation's frequency and consumption of the current (Bansal G. et al, 2017). The maximum allowable voltage employed to the circuit confines the speed of a given oscillator. Secondly, some small number of inverters has been used to generate ring as a result of high frequency of oscillation. A CMOS inverter incorporated of a PMOS transistor attached at drain terminal whereas NMOS transistor is connected with gate terminal. The VDD supply voltage and ground is adjoined to the source terminal of PMOS and NMOS transistors respectively (Kumar, S. and Kaur, G., 2012). For both type of transistors, VIN is provided at gate terminal whereas VOUT is given at drain terminals. CMOS inverter is one of the most widely used and adjustable MOSFET inverters used in chip design. They work with very little power deficit and at a relatively high speed. CMOS inverters have good logic buffer properties, in which low and high noise margins are both large (Abdul-Latif et al, 2012).

II. METHODOLOGY:**III. CIRCUIT DESIGN AND SIMULATION:****3.1 CMOS inverter:**

In order to verify the performance of ring oscillator single CMOS inverter was simulated. The inverter had given the drain voltage i.e. V_{dd} ranging from 0.065 to 1.7V. Fixed voltage of 1V had been fed as supply voltage and output voltage was measured with reference to the variation in the value of drain voltage (V_{dd}) (Rout, P.K et al, 2011). As we increase the input voltage given to inverter, the output result of it is varied from high voltage level to low voltage level, which verifies that the design of inverter is appropriate. Alternation of supply voltage consequently results into reaching up to the maximum value of output voltage (V_{out}) (Abdul-Latif, et al, 2012). If the v_{dd} is fixed to 1.7V then the V_{out} will deviate from 0.5 to 0V.

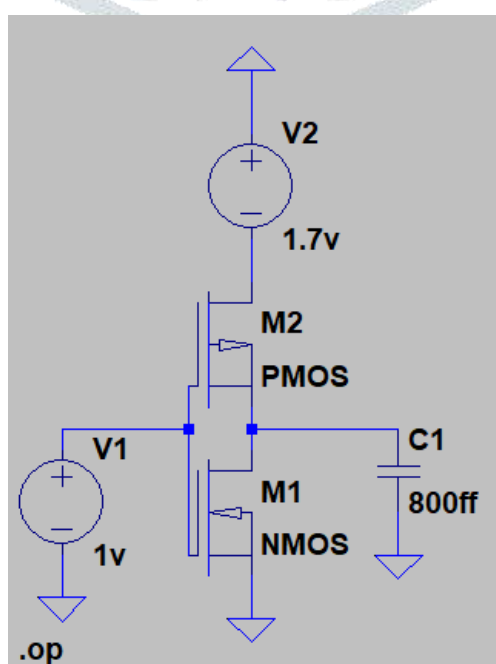


Fig. 1 Schematic of CMOS inverter

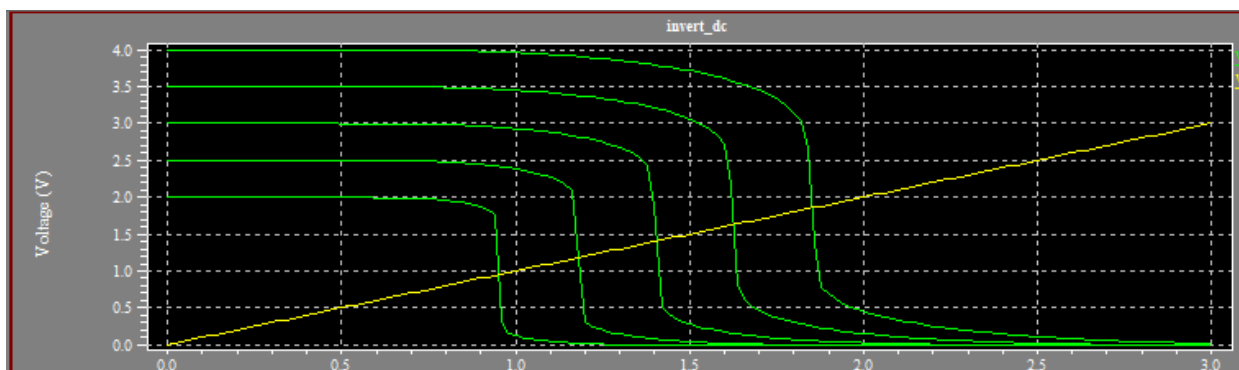


Fig. 2 waveform of CMOS inverter

3.2 Ring oscillator:

The ring oscillator is design with 7 inverting gate. The output of the last stage inverter is linked to the source of the first inverter. Supply voltage (Vdd) is connected and assigned to a changing value. GNDs are linked to the ground and the output is captioned as Vout. Ring oscillator schematic is shown in figure. The value, 7, the number of gates was chosen because it requires a peculiar number and large amounts, there by delaying the output voltage (Sikarwar, et al 2013).

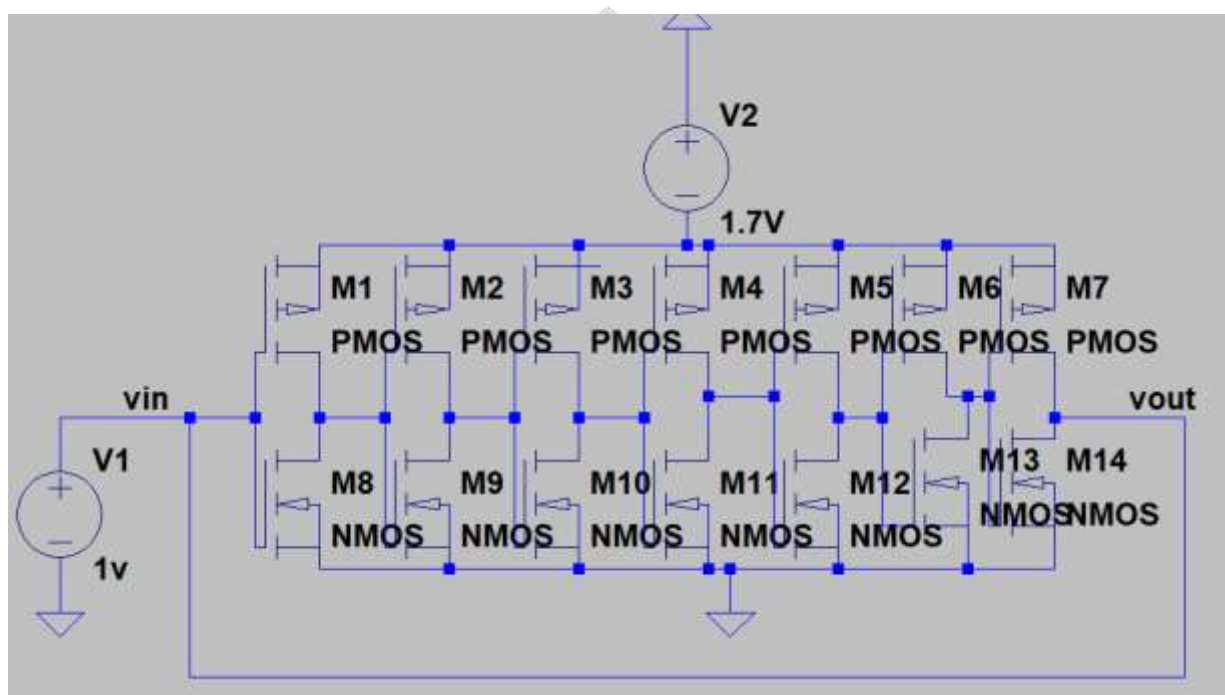


Fig. 3 Schematic of 7-stage ring oscillators

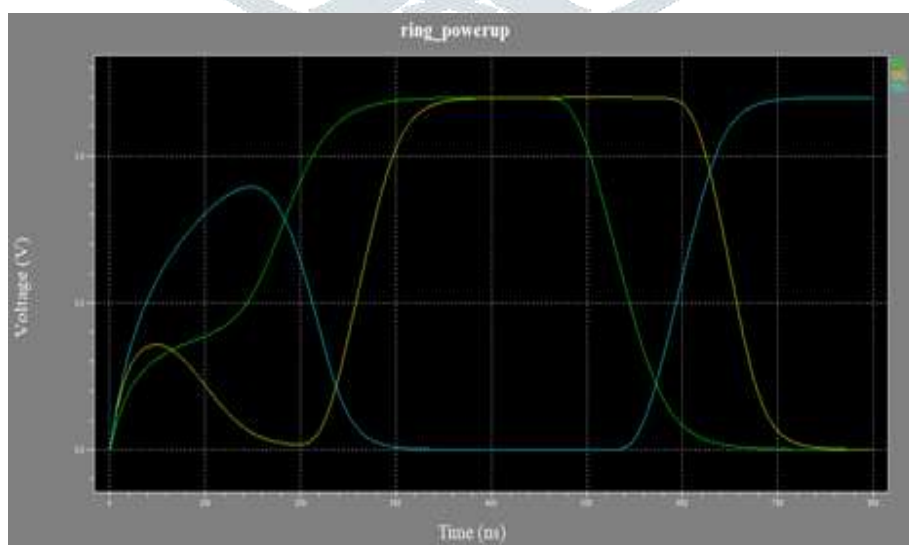


Fig.4 Waveform of 7-stage ring oscillator

3.3 RESULT:

The supply voltage was varied from 0.065V to 1.7V. This category was selected because the low voltage will not produce an inhibitory signal and the higher voltage will generate a signal without reaching the maximum voltage. Then the frequency and power

absorptions were made for these Vdd values (Masten, H.). Frequency is related to delaying the equation, so the delay of one oscillation was measured for each Vdd value.

$$\text{Frequency} = \frac{1}{\text{delay}} \quad (2)$$

Table 1 Measured frequencies and delays

Vdd	Frequency(MHz)	Delay(μ s)
1.7	3.6	0.277
1.5	2.069	0.48
1.3	0.6658	1.5
1.2	0.134	7.46
0.1	0.05425	18.43

Table 2 Measured power consumption

Vdd	ID	P(μ W)	P(mW)
1.7	4.90E-06	8.33	0.05831
1.5	2.50E-06	3.7525	0.02625
1.3	9.00E-07	0.9002	0.0081
1.1	1.00E-07	0.13000026	0.00013003
1	1.88E-12	2.0662E-05	0.0017
0.9	1.68E-12	1.6817E-05	0.0002075
0.7	1.29E-12	1.1605E-05	0.0000145
0.5	1.29E-12	9.0361E-06	0.00001187
0.3	5.18E-13	2.592E-06	8.123E-06
0.1	1.59E-13	0.00043403	0.00000633
0.065	1.01E-13	0.00022045	0.0001814

Power consumption of CMOS inverters is calculated using equation 2. In this simulation, the load capacity of the inverter was unknown. The RMS value of the present was recorded from the power supply at each voltage level. Power consumption of a single CMOS inverter is therefore multiplied by the number of gateways, 7, to the power consumption of the entire circuit (Bako, N. and Baric A., 2013). The one gate is fixed for current and power consumption of RMS of entire circuit. The power consumption of the ring oscillator is different and varies from 0.05831 mW at a vdd of 1.7V and 181.4 nW at vdd of 0.0675V.

$$\text{Power} = c * vdd^2 * f \quad (3)$$

$$\text{Power} = I(\text{rms}) * vdd \quad (4)$$

The simulation showed in figure 5 there is a negative relationship with delay in the supply of voltage and positive relationship with power consumption that voltage supply has a negative correlation with delay and a positive correlation with power consumption. These results agree that what was expected was based on the concept of low power design. Power consumption of a CMOS inverter is dependent on the supply voltage as shown in equation 3. While frequency is also a factor and shows an increase as the supply voltage decreases, the consumption of this low supply voltage decreases the total power consumption. As Vdd decreases the delay will increase. The delay is also dependent on the supply voltage.

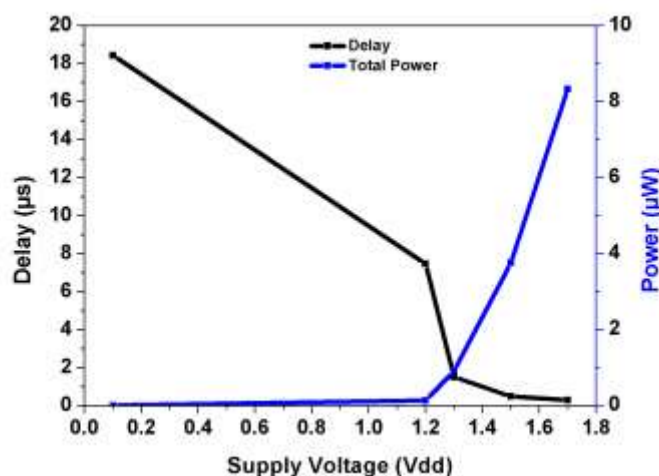


Fig.5 Delay and Power Consumption vs. Supply voltage

IV. CONCLUSION:

A 7 stage ring oscillator is designed using CMOS technology and simulated in LT spice. The power consumption, frequency, delay were measured for different values of supply voltage. As the Vdd increased, the delay reduced and power consumption

increased and the frequency increased. The frequency range is measured to be from 3.6 MHz and 0.0754 MHz, a delay of 0.27 μ s and 18.43 μ s, and a power consumption of 8.3 μ W and 0.4mW.

Further research can be done in the future to reduce the power consumption of the ring oscillator. This proposed circuit can be further improved by adding current starving techniques and process compensation circuit.

References:

- [1] Abdul-Latif, M.M. and Sánchez-Sinencio, E., 2012. Low phase noise wide tuning range N-push cyclic-coupled ring oscillators. *IEEE Journal of Solid-State Circuits*, 47(6):1278-1294.
- [2] Bako N. and Baric A., 2013. A low-power, temperature and supply voltage compensated current starved ring oscillator. *Microelectronics Journal*, 44(12):1154-1158.
- [3] Bansal, G., Agrawal, S. and Saxena, N., 2017. Analysis of ultra-high frequency CMOS ring oscillator and study the supply voltage variation on performance parameter. *International Journal of Innovative Research in Engineering and Applied Sciences*, 2-2.
- [4] Hajimiri, A., Limotyrakis, S. and Lee, T.H., 1999. Jitter and phase noise in ring oscillators. *IEEE Journal of Solid-state circuits*, 34(6):790-804.
- [5] Khatoon, F., Tarana A chandel, 2014. Design of Ring VCO using nine stages of Differential Amplifier. *International Journal of Research in Engineering and Technology*, 120-123.
- [6] Kumar, S. and Kaur, G., 2012. Design and performance analysis of nine stages CMOS based ring oscillator. *International Journal of VLSI design & Communication Systems*, 3(3):57.
- [7] Mandal, M.K. and Sarkar, B.C., 2010. Ring oscillators: characteristics and applications.
- [8] Masten, H., Ring oscillator design in 32nm CMOS with frequency and power analysis for changing supply voltage.
- [9] Michal, V., 2012. On the low-power design, stability improvement and frequency estimation of the CMOS ring oscillator. In *Radio elektronika (RADIOELEKTRONIKA)*, 22nd International Conference, 1-4.
- [10] Nayak, R., Kianpoor, I. and Bahubalindrani, P.G., 2017. Low power ring oscillator for IoT applications. *Analog Integrated Circuits and Signal Processing*, 93(2):257-263.
- [11] Rout, P.K. and Acharya, D.P., 2011. Design of CMOS ring oscillator using CMODE. In *Energy, Automation, and Signal (ICEAS)*, 1-6.
- [12] Shivhare, A., and Gupta, M.K., 2016. Low power ring Oscillator at 180nm CMOS Technology. *International Journal of Computer Applications*, 0975-8887
- [13] Sikarwar, V., Yadav, N. and Akashe, S. 2013. Design and analysis of CMOS ring oscillator using 45 nm technology. In *Advance Computing Conference (IACC)*, 1491-1495.
- [14] Yodprasit, U., Botteron, C., Farine, P.A. and Heubi, A., 2007, December. Shunt-feedback ring oscillator: a new topology for wideband multiphase signal generations. In *Radio-Frequency Integration Technology*, 78-81.

