IMPLEMENTATION OF VARIOUS LOW POWER TECHNIQUES IN A CHAIN OF FOUR INVERTERS

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Abstract:

While designing a VLSI system, power dissipation is one of the major concerns. Up to a certain time dynamic power was the single largest concern; however as the technology feature size shrinks static power has become an important issue as dynamic power. A well-known previous technique called the sleep transistor technique cuts off V_{dd} and/or Gnd connections of transistors to save leakage power consumption. However, when transistors are allowed to float, a system may have to wait a long time to reliably restore lost state and thus may experience seriously degraded performance. Therefore, retaining state is crucial for a system that requires fast response even while in an inactive state. The two common approaches are sleepy stack and sleepy keeper. Both methods are excellent in this regard. The static and dynamic power of sleepy stack is considerably low. But it has a delay penalty and its area requirement is maximum compared with other processes. Again the sleepy keeper process possesses excellent speed criteria but it requires more static and dynamic power than sleepy stack. Our goal is to trade off between these limitations and thus propose new methods which reduce both leakage and dynamic power with minimum possible area and delay trade off.

Key words: VLSI system, power dissipation, static power, dynamic power, sleep transistor technique, sleepy keeper process.

1. INTRODUCTION

For the most recent CMOS feature sizes (e.g., 65nm and 45nm), leakage power dissipation has become an overriding concern for VLSI circuit designers. International technology roadmap for semiconductors reports that leakage power dissipation may come to dominate total power consumption. Power consumption of CMOS consists of dynamic and static components. Dynamic power is consumed when transistors are switching, and static power is consumed regardless of transistor switching. Dynamic power consumption was previously the single largest concern for low-power chip designers since dynamic power accounted for 90% or more of the total chip power. Therefore, many previously proposed techniques, such as voltage and frequency scaling, focused on dynamic power reduction. However, as the feature size shrinks, e.g., to 0.065µ and 0.045µ, static power has become a great challenge for current and future technologies.

There are many reasons for which power losses occur in CMOS circuit. Figure 1 shows different types of leakage components. They are:

1. Sub-threshold leakage (weak inversion current)
2. Gate oxide leakage (Tunneling current)
3. Channel punch through
4. Drain induced barrier lowering

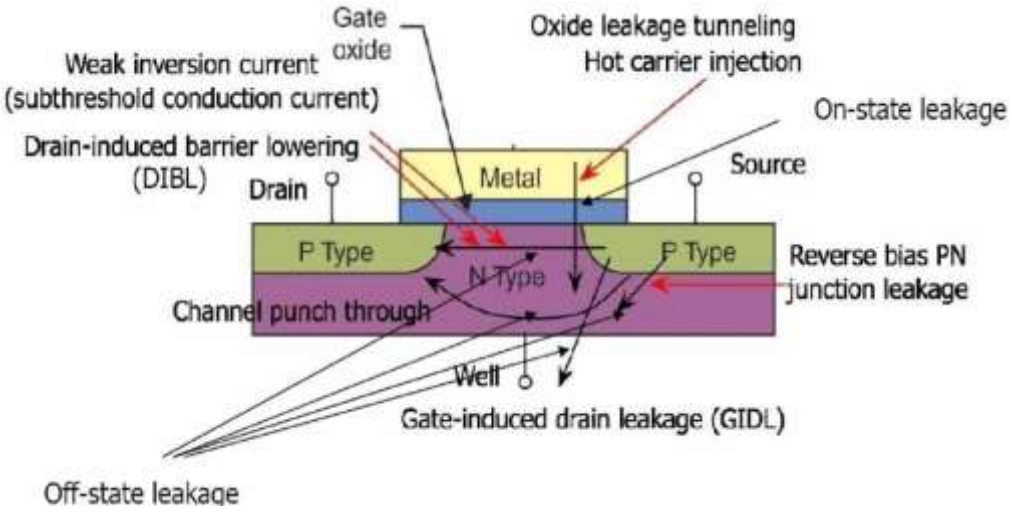

Figure 1: Leakage power components in CMOS

One of the main reasons causing the leakage power increase is increase of sub-threshold leakage power [1]. The Sub-threshold conduction or the sub-threshold leakage or the sub- threshold drain current is the current that flows between the source and drain of a MOSFET when the transistor is in sub-threshold region that is, for gate-to- source voltages below the threshold voltage. The sub-threshold region is often referred to as the weak inversion region. When technology feature size scales down, supply voltage and threshold voltage also scale down. Sub-threshold leakage power increases exponentially as threshold voltage decreases which increases the sub-threshold leakage power. Next the gate oxide leakage, the gate oxide, which serves as insulator between the gate and channel, should be made as thin as possible to increase the channel conductivity and performance. But as the gate oxide is made thinner the barrier voltage of the oxide changes. For the positive gate voltage thus some positive charges get stuck in the oxide. Therefore, current flows through the oxide. This is also known as tunneling current.

Punch through in a MOSFET is an extreme case of channel length modulation where the depletion layers around the drain and source regions merge into a single depletion region. The field underneath the gate then becomes strongly dependent on the drain-source voltage, as is the drain current. Punch through causes a rapidly increasing current with increasing drain-source voltage. This effect is undesirable as it increases the output conductance and limits the maximum operating voltage of the device.

Drain induced barrier lowering or DIBL is referred to the reduction of threshold voltage of the transistor at higher drain voltages. The combined charge in the depletion region of the device and that in the channel of the device is balanced by three electrode charges: the gate, the source and the drain. As drain voltage is increased, the depletion region of the p-n junction between the drain and body increases in size and extends under the gate, so the drain assumes a greater portion of the burden of balancing depletion region charge, leaving a smaller burden for the gate. As a result, the charge present on the gate retains charge balance by attracting more carriers into the channel, an effect equivalent to lowering the threshold voltage of the device.

2. Literature review

In this section we analyze the previous approaches which are closely related to our work. Here we discuss previous low power technique that primarily target for reducing leakage. This technique for leakage reduction can be grouped into two categories:
(i) State saving (ii) state destructive. The previous approaches that are adopted in VLSI design are:

2.1 Base Case

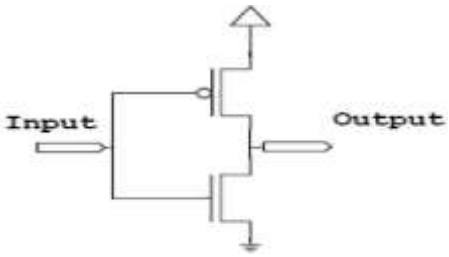

Figure 2.1: Base Case

The base case circuit contains only the PMOS network and the NMOS network and there exists no method to reduce leakage. A base case inverter is shown Figure 2.1. It is a state- saving technique and minimum area requirement.

2.2 Sleep Transistor Technique

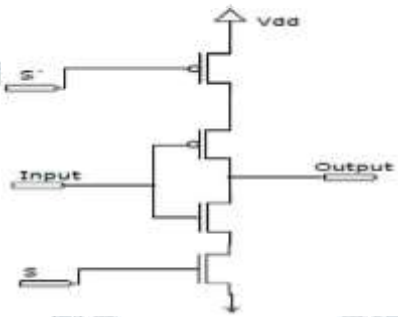

Figure 2.2 Sleep Transistor Technique

State -destructive techniques cut off transistor (pull-up or pull-down or both) networks from supply voltage or ground using sleep transistors. These types of techniques are also called gated V_{dd} and gated-GND. Mutoh et al. propose a technique they call Multi-Threshold- Voltage CMOS (MTCMOS) [6], which adds high-V_{th} sleep transistors between pull-up networks and V_{dd} and between pull-down networks and ground as shown in Figure 2.2 while logic circuits use low- V_{th} transistors in order to maintain fast logic switching speeds. The sleep transistors are turned off when the logic circuits are not in use. By isolating the logic networks using sleep transistors, the sleep transistor technique dramatically reduces leakage power during sleep mode. However, the additional sleep transistors increase area and delay [2]. Furthermore, the pull-up and pull-down networks will have floating values and thus will lose state during sleep mode. These floating values significantly impact the wakeup time and energy of the sleep technique due to the requirement to recharge transistors which lost state during sleep.

2.3 Forced stack

Another technique to reduce leakage power is to stack the transistors. Figure 2.3 shows a forced stack inverter. The effect of stacking the transistor results in the reduction of sub- threshold leakage current when two or more transistors are turned off together.

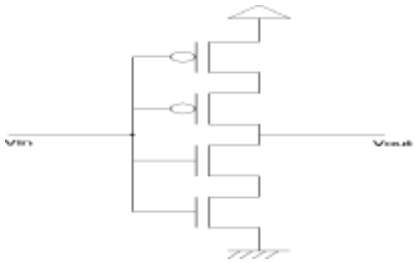

Figure 2.3: Forced stack inverter

The stacking effect [3] can be understood from the forced stack inverter shown in figure 2.3. In the generic inverter there are only two transistors. But here in case of forced stack inverter two pull up transistors and two pull down transistors are used. All inputs share the same input in the forced stack circuit.

2.4 Sleepy stack approach

In the sleepy stack structure the forced stack and the sleep transistor techniques are combined together [8]. Hence the names sleepy stack. Figure 2.4 shows a sleepy stack inverter.

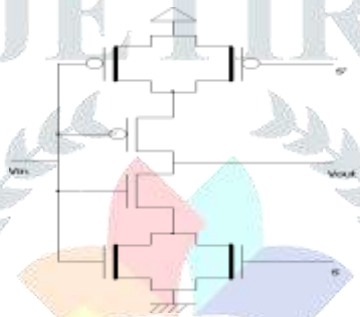

Figure 2.4: Sleepy stack inverter

The sleepy stack inverter in figure 2.4 uses the aspect ratio W/L = 3 for the pull up transistors and W/L =1.5 for the pull down transistors. At the same time the conventional inverter with the same input capacitance uses the aspect ratio W/l = 6 for the pull up transistors and W/L = 3 for the pull down transistors.

2.5 Sleepy keeper approach

In the traditional CMOS design the NMOS are placed always at the pull down network because it is well known that NMOS transistors are not efficient at passing V_{dd} shown in Figure 2.5. On the other hand PMOS transistors are placed at the pull up network because PMOS transistors are not efficient at passing GND.

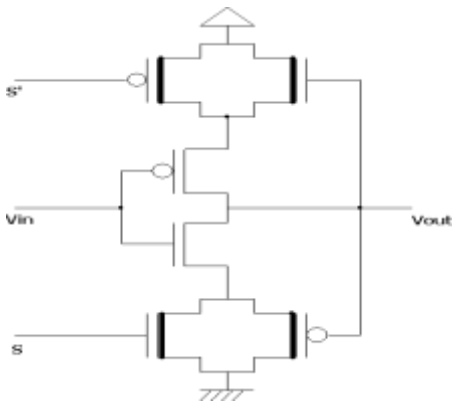

Figure 2.5: Sleepy keeper approach

Let us maintain a value of '1' in sleep mode and assume that the value has already been calculated. The sleepy keeper [4] circuit in figure 2.5 uses this output value of '1' and an NMOS transistor maintains this value during sleep mode. An additional NMOS transistor is added in parallel to the pull up sleep transistor connected to V_{dd}. At sleep mode this NMOS transistor is the only source of V_{dd} to the pull-up network since the sleep transistor is off. Similarly, to maintain a '0' value, assume that the value is already calculated. The sleepy keeper approach [5] uses this output value of '0' and a PMOS transistor maintains the value during sleep mode.

2.6 Dual Sleep approach

Sleep transistors are crucial part in any low leakage power design. In dual sleep method [6] shown in figure 2.6, two sleep transistors in each NMOS or PMOS block are used. One sleep transistor is used to turn on in ON state and the other one is used to turn on in OFF state. Again in OFF state a block containing both PMOS and NMOS transistors are used in order to reduce the leakage power.

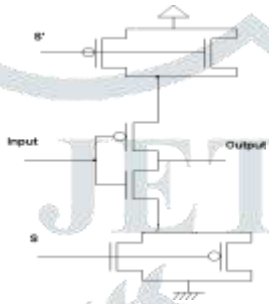

Figure 2.6: Dual sleep method

3. PROPOSED METHODS

Forced sleep approach, Stack sleep approach and Variable body biasing techniques are the proposed methods and can successfully be implemented in logic design i.e., in a chain of four inverters which is chosen as a logic circuit. A chain of four inverters is chosen because an inverter is the most basic logic circuit in CMOS technology.

3.1 Forced sleep approach

Figure 3.1 depicts a chain of four inverters using forced sleep method. We size the transistor of the inverter to have equal rise and fall times in each state. In this method we use aspect ratio W/L = 1.5 for all the NMOS transistors and W/L = 3 for all the PMOS transistors.

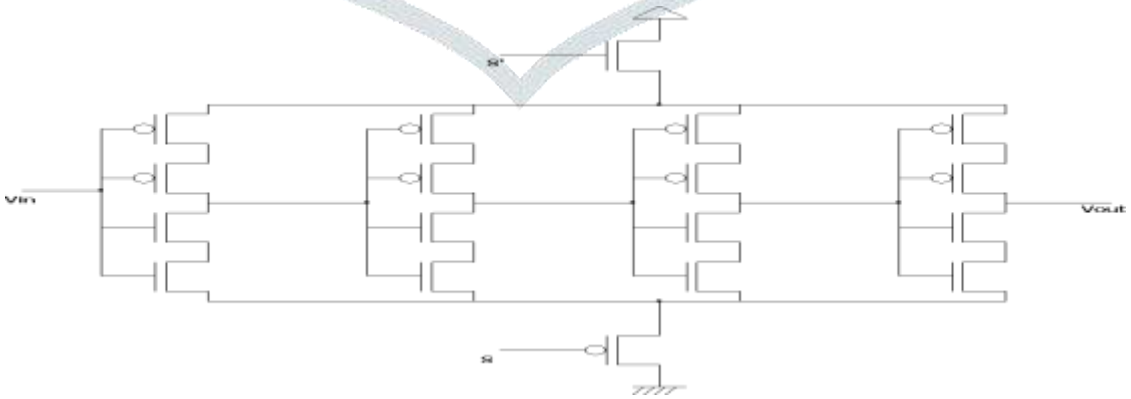

Figure 3.1: Forced sleep method using a chain of 4 inverters

3.2 Stacked sleep approach using a chain of 4 inverters

In this stacked sleep approach we size the transistors of the inverter to have equal rise and fall times in each state. Figure 5.1.2 depicts a chain of four inverters using stacked sleep approach. This method uses aspect ratio W/L = 3 for all nmos transistors and W/L = 6 for all pmos transistors in the main inverter circuit. For the sleep transistors and extra transistors it

uses aspect ratio W/L = 1.

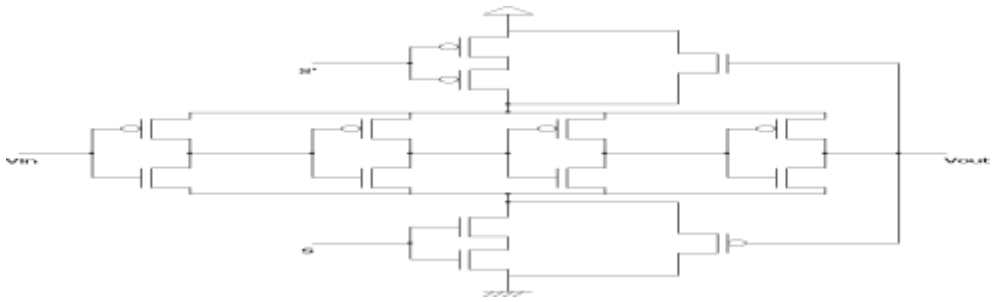

Figure 3.2: Stacked sleep approach using a chain of 4 inverters

3.3 Variable body biasing technique using a chain of 4 inverters

In variable body biasing technique we size the transistors of the inverter to have equal rise and fall times in each state. Figure 5.1.3 depicts a chain of four inverters using variable body biasing technique. This method uses aspect ratio W/L = 3 for all nmos transistors and W/L = 6 for all pmos transistors in the main inverter circuit. For the sleep transistors and extra transistors it uses aspect ratio W/L = 1.

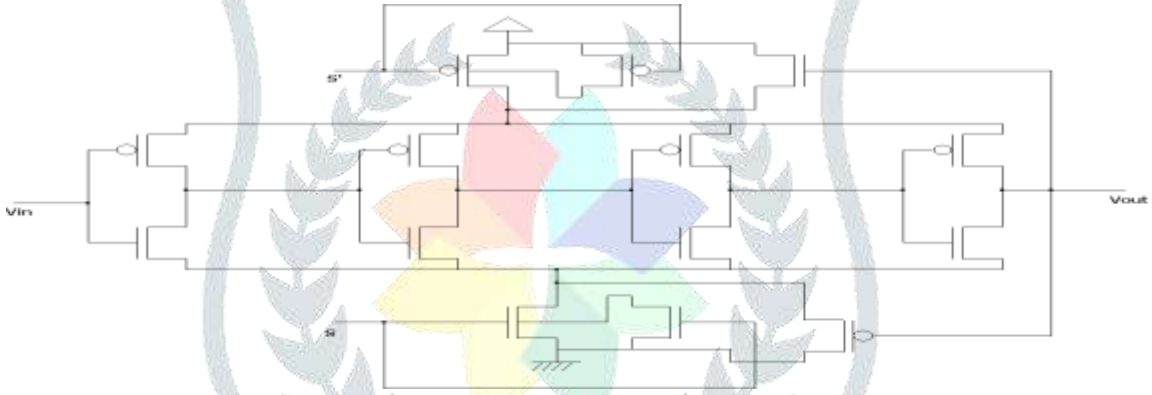

Figure 3.3 Variable body biasing technique using a chain of 4 inverters

Table (1) : Result analysis of previous work

Method	Prop. Delay (s)	Static power (w)	Dynamic power (w)	Area (μm^2)
Base case	2.4484E-11	8.7649E-08	3.6138E-06	1.20
Sleep	3.6201E-11	1.6272E-09	2.7774E-06	2.45
Forced stack	1.3511E-10	3.9920E-10	8.0436E-07	1.38
Sleepy stack	5.8477E-11	7.0533E-10	1.4503E-06	2.07
Sleepy keeper	4.0711E-11	1.4976E-09	2.8465E-06	1.83
Dual sleep	3.8831E-11	1.1840E-09	2.0870E-06	1.28

Table (1) : Result analysis of proposed work

Method	Prop. Delay (s)	Static power (w)	Dynamic power (w)	Area (μm^2)
Stacked sleep	1.3128E-10	1.9640E-10	7.2014E-07	1.54
Variable body biasing	7.8629E-11	3.6360E-10	1.0344E-06	1.54
Forced sleep	3.3781E-09	5.9908E-12	1.3517E-07	1.78

4 . Conclusion

Consider the case of a chain of four inverters, sleepy stack method shows 7.5802% improvement and 92.8275%, 58.8095% degraded performance than stacked sleep method in propagation delay, dynamic power and static power, respectively. When compared to variable body biasing technique, sleepy stack method shows 49.1254%, 87.6638% and 42.7778% degraded performance in propagation delay, static power and dynamic power, respectively. Again in comparison with sleepy stack approach, forced sleep technique gives 93.35% degraded performance in propagation delay, but gives comparatively good performance in static and dynamic power.

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