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CHANNEL THICKNESS DEPENDENCE OF DIBL EFFECT IN DOUBLE GATE MOSFET

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Abstract : Among the many novel device geometries for continuing the process of downscaling in future technology nodes, the double-gate MOSFET (DG-MOSFET) is a potential candidate to replace the conventional bulk MOSFET due to its superior performance in the sub-10 nm range. In a DG-MOSFET, the presence of more number of gates improves the electrostatic control of the channel by the gate and hence reduces short channel effects. This work investigates the influence of channel thickness on one of the major short channel effects, the DIBL, for fully depleted Si channel DG-MOSFETs with channel length of 12nm. It is found that the DIBL decreases almost linearly from its value of 104mV/V at a channel thickness of 5nm to 8.6mV/V at a channel thickness of 2nm. Thus, a careful engineering of channel thickness can suppress the DIBL to the required minimum level when DG-MOSFETs are downscaled to meet future market requirements.

Index Terms **- DIBL, DG-MOSFET, short channel effect, NEGF.**

I. INTRODUCTION

The scaling of MOSFETs, which are the building blocks of integrated circuit (IC) chips, has successfully continued in the past ever since the introduction of the IC technology in the 1960's. This downscaling, continued in accordance with an empirical rule framed in the early 1970's by G. E. Moore [1], was possible mainly due to the phenomenal progress in process technology [2,3,4]. Thus, the feature size of MOSFET has scaled down from about 10μm in 1972 to 15nm in 2015. However, further downscaling of MOSFETs appears to be difficult due to the difficulty in overcoming the challenges such as the aggravating short channel effects (SCEs) [5,6,7]. To continue with the scaling in future, the industry has to look beyond traditional device geometries, which suffer from severe SCEs [6,8]. Accordingly, the 2012 update of the International Technology Roadmap for Semiconductors (ITRS) suggested the introduction of advanced Silicon On Insulator (SOI) devices such as multi-gate MOSFETs and FINFETS, 1D devices such as nanowire and carbon nanotube FETs and even molecular transistors [9]. Many such novel device geometries have been implemented or presently are being vigorously investigated by the semiconducting industry [10,11,12,13] to meet the requirements of future applications.

Various geometries of multi-gate FETs presently being investigated by the semiconducting industry include double-gate, trigate, and gate-all-around MOSFETs. Among these novel device geometries, the double-gate MOSFET (DG-MOSFET) is a potential candidate to replace the conventional bulk MOSFET [14] due to its superior performance in the sub-10nm technology node as the presence of more number of gates improves the electrostatic control of the channel by the gate and, hence, reduces short channel effects. Though the GAA or trigate structures may provide better electrostatic control of the channel than a double gate structure, they suffer from severe layout-area inefficiency. However, commercialization of DG- MOSFETs require more sophisticated process technology in future [15].

The degrading factors in the scaled dimensions, commonly known as short channel effects (SCEs), include the subthreshold leakage current, gate oxide tunneling, threshold voltage rolloff and Drain Induced Barrier Lowering (DIBL) [16]. For bulk MOSFETs, the drain current decreases exponentially with an ideal subthreshold swing of 60mV/decade as the gate voltage drops below the threshold voltage. However, in scaled devices this ideal subthreshold swing degrades due to the increased subthreshold leakage current, which increases in proportion to W/L (W- channel width, L-channel length) [17]. This subthreshold current is the main contributor to the off-state current, which accounts for the static power that a circuit consumes even when it is in the standby mode. While scaling, gate oxide thickness is to be reduced nearly in proportion to the channel length. This leads to quantum-mechanical tunneling of charge carriers across the oxide layer, giving rise to a gate leakage current that increases exponentially as the oxide thickness is scaled down [18]. In scaled devices, the threshold voltage V_t becomes dependent on channel length and the drain bias. The deviation of V_t from its ideal value with decreasing channel length is known as the threshold voltage rolloff. The deviation of Vt with high drain bias is called the Drain Induced Barrier Lowering (DIBL). DIBL occurs due to the increased influence of the drain voltage on the height of the potential barrier in the channel, and points to a limitation to downscaling. But, it has already been established that a reduction in channel thickness reduces DIBL effects [19]. A careful engineering of channel dimensions can keep DIBL under control. In this article, we investigate the variation of DIBL in fully depleted DG-MOSFETs as the channel length and thickness of the device are reduced, and show that DIBL can be controlled if the channel thickness is suitably downscaled along with channel length.

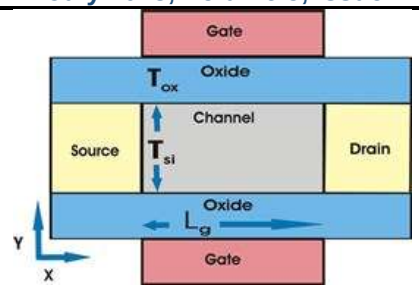

Fig. 1. A Double Gate MOSFET (DG-MOSFET) structure. Fully depleted semiconductor channel is coupled to heavily n-doped Source/Drain semiconductor regions. Top and bottom metal gates are separated from the channel by a thin oxide layer. The transport is assumed to be in the x direction, the confinement direction is y and the width of the device is along the z direction.

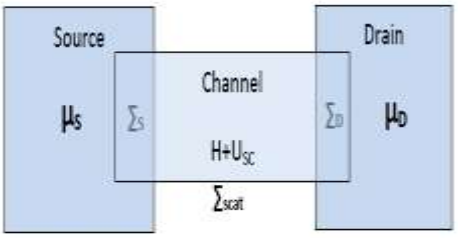

Fig. 2. Schematic of a nanoscale device coupled to Source and Drain contacts. H is the device Hamiltonian, and U_{SC} is the self-consistent channel potential. The effect of coupling the channel to the S/D contacts and scattering of carriers in the channel are accounted for by the self-energy matrices Σ_S, Σ_D and Σ_{SCAT}respectively.

II. Device Structure of DG-MOSFET

The structure of a DG-MOSFET is similar to a conventional MOSFET, except that there are gates on either side of the channel, known as top gate and bottom gate. The presence of two gates promise better control of the channel by ensuring that no part of the channel is far away from a gate electrode. Further, it offers the possibility of two mode of operation , that is, applying bias to both gates simultaneously or applying a bias to one of the gates alone while the other is grounded [11]. The structure of the DG-MOSFET used in this study is shown in fig. 1. It consists of a fully depleted Si channel. The source and drain extension regions on the left and right of the Si channel are heavily n-doped Si regions. The upper and lower metal gates are made up of Al and are separated from the channel by SiO_2 layer. We consider only symmetric operation mode of the device, that is, the same voltage is applied to both gates simultaneously. The width of the device in the *z* direction is assumed to be very large, compared to the other two dimensions. When a positive bias is applied to the Drain contact with respect to the Source, electrons flow from the source to the drain constituting the current. The current is depending on the potential of the channel, which is modulated by the gate bias.

III. Computational Details

All the calculations in this work were done using the free simulation package Nanomos 2.5 available at nanohub of Purdue university [20]. The program, nanoMOS, uses the Non Equilibrium Green's function (NEGF) approach, which provides a rigorous description of quantum transport and interactions that randomize phase [21]. Within the NEGF scheme, the channel is represented by a Hamiltonian (H), which is coupled to two infinite reservoirs (S/D) characterized by their respective Fermi levels μ_S and μ_D (fig. 2). Within NEGF, coupling of the active device to the S/D reservoirs and the dissipative effects of scattering can be accounted for by using appropriate self-energy matrices Σ_S, Σ_D and Σ_{SCAT}respectively [22,23].

Thus, the Green's function has the form

$$G(E) = \left((E + i0^+)I - H - \Sigma_S(E) - \Sigma_D(E) - \Sigma_{SCAT}(E)\right)^{-1} \quad (1)$$

where the single band effective mass Hamiltonian H is

$$H = \frac{-\hbar^2}{2}\left(\frac{1}{m_x^*}\frac{\partial^2}{\partial x^2} + \frac{1}{m_y^*}\frac{\partial^2}{\partial y^2} + \frac{1}{m_z^*}\frac{\partial^2}{\partial z^2}\right) \quad (2)$$

The density matrix ρ(r)is given by

$$\rho = \frac{1}{2\pi}\int_{-\infty}^{+\infty}\left(f_S(E)G\Gamma_S G^+ + f_D(E)G\Gamma_D G^+\right)dE \quad (3)$$

where, $f_S(E)$ and $f_D(E)$ are the electron occupation probability at the source and drain ends respectively. The broadening matrices $\Gamma_{S/D}$ in eqn. 3 are defined as

$$\Gamma_S = i(\Sigma_S - \Sigma_S^+) \quad (4)$$

$$\Gamma_D = i(\Sigma_D - \Sigma_D^+) \quad (5)$$

Starting with some initial guess for the electrostatic potential U_{SC}, the charge density ρ(r) is computed through NEGF equations. Knowing the charge density, Poisson's equation is solved for obtaining the new value of U_{SC}. NEGF equations and Poisson's equation are self-consistently solved till we obtain accurate values of ρ(r) and U_{SC} (fig. 3).

The transport is assumed to be in the x direction, the confinement direction is y and the width of the device is along the z direction. The device is assumed to be wide enough so that electronic eigen functions are plane waves in that direction. The device is biased by applying a positive potential at the drain contact with respect to the source contact. The current can be calculated from the expression

$$I = \frac{2q}{\hbar}\int_{-\infty}^{+\infty}\left[Tr(\Gamma_S G\Gamma_D G^+)\left(f_S(E) - f_D(E)\right)\right]dE \quad (6)$$

The finite difference discretization grid is used for the numerical solution of the NEGF transport equation and Poisson's equation [22,23] (fig. 4). The finite difference grid consists of uniformly spaced nodes with a mesh spacing of *a* along the transport direction x and *b* along the confinement direction y. The simulation domain of the self-consistent loop includes the S/D extension regions, the channel and the top and bottom oxide layers.

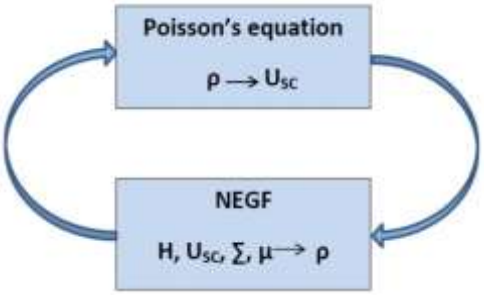

Fig. 3. The self consistent scheme for calculating the charge density and channel potential under non equilibrium conditions of charge transport. Starting with some initial guess for the electrostatic potential U_{SC}, the charge density ρ(r) is computed through NEGF equations. Knowing the charge density, Poisson's equation is solved for a more accurate U_{SC}. These steps are iterated until U_{SC} and ρ(r) converge.

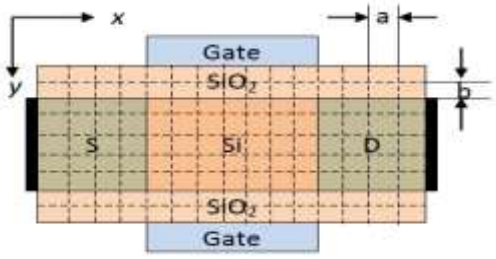

Fig. 4. The finite difference grid for the discretization of the 1D effective mass Hamiltonian and the Poisson's equation in the self-consistent simulation scheme. The grid consists of uniformly spaced nodes with a mesh spacing of *a* along the transport direction x and *b* along the confinement direction y. The simulation domain includes the S/D extension regions, the channel and the top and bottom oxide layers.

The Hamiltonian in eqn. 2, when discretized using the finite difference method yields the Hamiltonian matrix H for the active device region.

$$H = \begin{pmatrix} h(E_1) & 0 & \cdots & 0 \\ 0 & h(E_2) & 0 & 0 \\ \vdots & 0 & \ddots & \vdots \\ 0 & 0 & \cdots & h(E_m) \end{pmatrix} \quad (7)$$

where, $h(E_i)$ is the Hamiltonian for subband *i*.

$$h(E_i) = \begin{pmatrix} 2t - E_i(x_1) & -t & \cdots & 0 \\ -t & 2t - E_i(x_2) & 0 & 0 \\ \vdots & 0 & \ddots & \vdots \\ 0 & 0 & \cdots & 2t - E_i(x_n) \end{pmatrix} \quad (8)$$

$E_i(x_j)$ represents the energy of the subband *i* at the *j*th node of the finite difference grid along the transport direction. The coupling term within each subband is indicated by

$$t = \frac{\hbar^2}{2m_x^* a^2} \quad (9)$$

where m_x^* is the electron effective mass in the x direction, and *a* is the finite difference lattice constant in the x direction.

The Poisson's equation is

$$\nabla \cdot (\varepsilon \nabla U_{SC}) = -q^2(p - n + N_D - N_A) \quad (10)$$

where p is the hole concentration, n is the electron concentration, N_D and N_A are donor and acceptor concentrations, q is the elementary charge, ε is the position dependent dielectric constant. A 2D numerical solution to eqn.10 is composed of potential values at each lattice node of the finite difference grid. To attain these N_X . N_Y potential values (N_X- number of grid points in the x-direction, N_Y- number of grid points in the y- direction), the necessary equations are obtained by applying eqn. 10 at all internal nodes of the simulation grid and applying the boundary conditions at the boundary nodes. At the gate contacts, Dirichlet boundary conditions are used, $U_{SC} = qU_G$, where the gate vacuum potential U_G is determined from the gate bias voltage V_G and work function of the gate contact material. Neumann boundary conditions are imposed at the source/drain contacts and at other boundaries without electrode contacts, $\vec{n} \cdot \vec{\nabla} U_{SC} = 0$, for ensuring charge neutrality at the contact regions. The set of linear equations so obtained are solved directly to obtain U_{SC}.

In our work, characteristics of DG-MOSFETs with channel length of 12nm and channel thickness varying from 2nm to 5nm are investigated. These extremely small channel length is comparable with the mean free path of the electrons, and hence the effect of scattering is not very significant at these dimensions. This fact justifies the use of ballistic transport, that has been assumed in the calculations [26]. We assume a metal gate contact with work function 4.21eV and 2nm thick SiO2 layers as the top and bottom gate dielectric. The source and drain regions included in the finite difference simulation grid are 4nm in extension and have a uniform donor doping of $10^{20}/cm^3$. The channel is made up of undoped Si. Other device parameters such as the oxide thickness, the source and drain extension regions, the metal gate contact work function etc., are kept constant. The finite difference mesh size along the transport direction a = 0.2nm and that along the confinement direction b = 0.1nm. Assuming the transport to be along the (100) direction, we use two different effective masses in the x and y directions: m_x^*=0.98m_0 and m_y^* =0.19m_0, where m_0 is the electron rest mass [27].

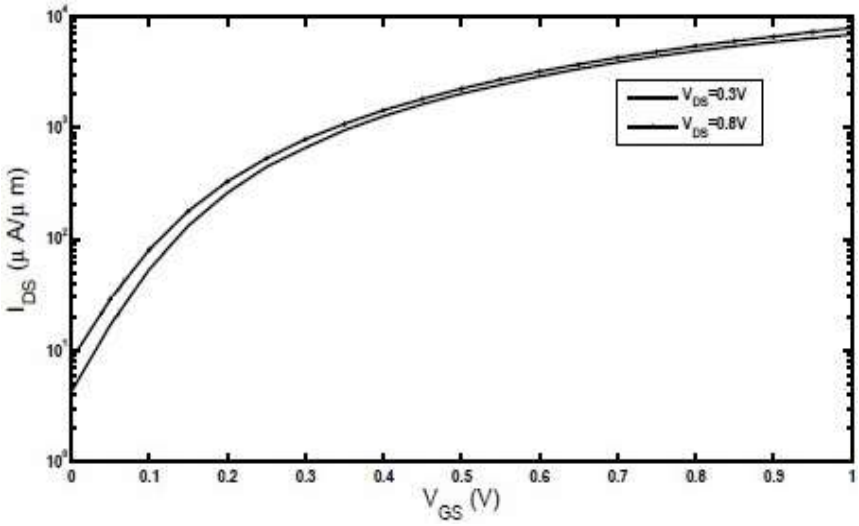

Fig. 5. Gate characteristics of a DG MOSFET for two different drain voltages (V_{D1}=0.3V, V_{D2}=0.8V). Note that the threshold voltage decreases asV_D increases.

Threshold voltage V_t represents the onset of significant drain current flow. In this work, the second derivative logarithmic (SDL) method was used for the determination of V_t. The SDL method defines V_t as the gate voltage corresponding to the minimum of the second derivative of log(I_D)-V_G plot. DIBL is calculated from the equation

$$\text{DIBL} = \frac{\Delta V_t}{\Delta V_D} \qquad (11)$$

where $\Delta V_t = V_t^{DD} - V_t^{Low}$($V_t^{DD}$is the threshold voltage measured at a high drain voltage and $V_t^{Low}$is the threshold voltage measured at a very low drain voltage, typically 0.1V) and $\Delta V_D = V^{DD} - V^{Low}$($V^{DD}$is the high drain voltage and $V^{Low}$is the low drain voltage).

IV. Results and Discussion

The gate characteristics for a device with channel length L_G = 12nm, channel thickness T_{Si} = 3.2nm, and oxide thickness T_{ox} = 2nm, for two different drain voltages (V_{D1}=0.3V , V_{D2}=0.8V) are shown in fig. 5. The subthreshold leakage current (the y-intercept of fig. 5) is significantly small for low drain voltages. The drain current increases exponentially in the subthreshold region and saturates at high gate voltages. The threshold voltage depends on V_D and decreases with increasing V_D.

The DIBL is found from eqn. 11. Figure 6 shows the variation of DIBL for devices of different channel thickness with a channel length equal to 12nm. As the channel thickness is downscaled from 5nm, DIBL shows a marked decrease, reaching a value of 8.6mV/V at 2nm from 104mV/V at 5nm. This effect must be expected, since as the channel thickness is increased, the gate voltage loses its control to the drain voltage on modulating the height of the potential barrier, leading to the degradation of the device performance and a high value for DIBL. The reduction in DIBL with channel thickness is almost linear, and indicates the possibility of controlling DIBL by careful engineering of channel thickness during the fabrication process.

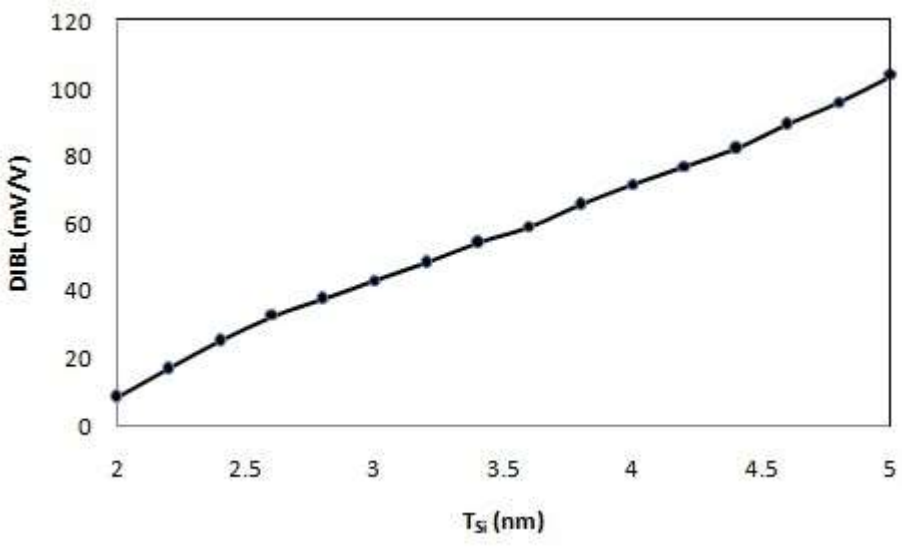

Fig. 6. Variation of DIBL with channel thickness for a DG-MOSFET. The device has channel length L_G = 10 nm, and oxide thickness Tox = 2nm. DIBL decreases steadily as the thickness is reduced.

V. CONCLUSIONS

The presence of two gates in DG-MOSFETs ensures better electrostatic control of the channel by since no part of the channel is far away from a gate electrode and promises better subthreshold performance during downscaling by minimizing short channel effects such as threshold voltage rolloff and DIBL. This work investigated the influence of channel thickness on DIBL for a fully depleted Si channel DG-MOSFETs with channel length of 12nm. It is found that the DIBL decreases almost linearly from its value of 104mV/V at a channel thickness of 5nm to 8.6mV/V at a channel thickness of 2nm. Thus, it is evident that a careful engineering of channel thickness can suppress the DIBL effect to the desired level during the downscaling of DG-MOSFETs.

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