DESIGN OF NOVEL BIOSENSING AMPLIFIER WITH LOW NOISE-POWER FOR WIRELESS BODY SENSOR NODES USING 45NM TECHNOLOGY

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Abstract : ***In this paper, the design of low noise, power efficient Biosensing amplifier and analog to digital converter (ADC) for wireless body sensor nodes and medical implantable gadgets. These design parameters helps to thorough analysis of biomedical recording systems and optimize them. Based on the analysis of biosensing amplifier, the design methodology is applicable for various biomedical applications. The design is done in 45nm Technology. The input signal which is taken for the design is mixed with noise and also the gain of the signal is very poor. In order to decrease the noise and increase the gain of the signal this design is implemented. For that reason, the chip is incorporated with Low clamor Amplifier (LCA), third order Gm-C Low Pass Filter (LPF) and 10-bit Successive Approximation Register (SAR) Analog to Digital Converter. The AFE gain is >100 dB. The AFE and ADC utilize only 133nW and 306nW from on chip regulators, respectively. The measured input referred noise is 0.387pVrms.***

IndexTerms - Analog front end (AFE), low clamor amplifier (LCA), implantable gadgets, wireless body sensor nodes (WBSN), power efficient.

I. INTRODUCTION

Recent advances in the wireless body sensor nodes (WBSNs) and implantable system-on-chips (SoCs) enable a huge example for the treatment of various illnesses such as neural disorders, cardiac diseases, glaucoma, and diabetes and muscle reinnervation [1]-[2]. In order to maximize the results of the problem associated with, the advanced wireless body sensor nodes and system-on-chips are required [3]. First, the scaled down WBSNs must be able to communicate concurrently with nearby base stations in a small wireless area network. The WBSNs are also demands an energy efficient strategy. The multi node data access feature is needed in future for the generalization of body sensor nodes (BSNs), and also for capturing the various biosignals concurrently from the different parts of the human body. Second, in order to have a battery less operation and longer life time for WBSNs [4]. This battery less operation removes the battery recharging or replacement requirements for the nodes. Moreover the toxicity with the batteries is undesirable for BSNs, since they are in direct contact with human body. Third, the continuous monitoring of the signal is required, in order to observe the changes occurring in the human body.

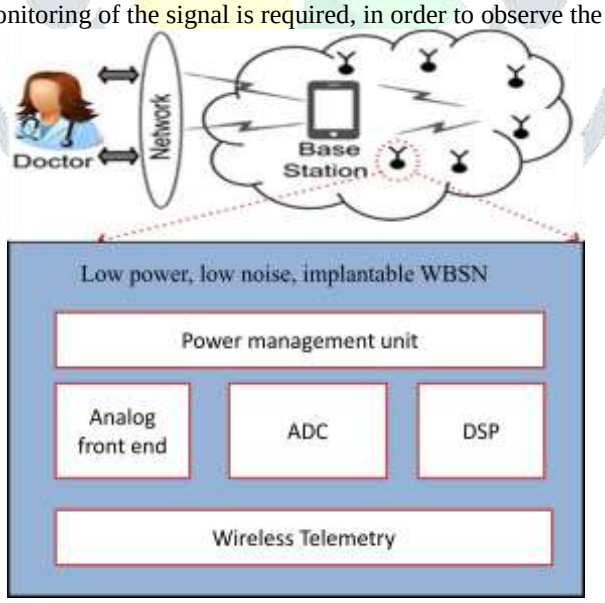

Figure. 1. Wireless Body Sensor Nodes forming a Wireless Body Area Network.

The design tradeoffs in the biosensing AFE are high gain, linearity of the signal, high CMRR, high PSRR, low noise, low power. A thorough analysis and design accumulation of the blocks is necessary to get the detail information about the biopotentials signals. For the process of result analysis and optimization, the main design challenges are follows [3].

a) *Framework outline limitations of the sensor hubs:* This incorporates an ideal number of amplification stages, control utilization of power, filter details, linearity, CMRR, and PSRR. In ongoing examinations, the application of wireless power move in WBSNs requests an extremely low pinnacle control utilization of the whole SoC. Be that as it may, a limited sum of ripple is still show in the supply voltage due to the absence of a bypass s off-chip capacitor. In addition, the post amplification flag handling in the advanced space infuses switching noise into the AFE that shows up as a common mode supply and substrate noise. Consequently, the AFE must have a high PSRR and CMRR, while restricting its control utilization to less than 1 μW.

b) *The idea of biopotential Signals:* These signals are described as a low-recurrence and low-amplitude signals. The amplitude of such signals from several micro volts to a couple of mill volts and their recurrence range ranges from sub-1 Hz to a couple of kilohertz. To guarantee a spotless signal obtaining, the AFE amplifier must have an adequately low input-referred noise (IRN) per unit transfer speed. Since the low frequencies are of interest, the flicker or 1/f noise of MOS transistors is a quick concern. Keeping in mind the end goal to oblige the upper end of the amplitude range (commonly 1– 5 mV), an adequate unique scope of the intensifier is additionally required.

c) *Reconfigurable AFE:* In future, the sensor hubs in a WBAN will catch the different biopotential signals, with various amplitudes and transfer speeds, at the same time from the diverse parts of a human body. Likewise, a solitary AFE with reconfigurable parameters settings, for example, gain, bandwidth, bias current, and sampling rate, is profoundly attractive. The amplifier linearity at low bias current is another imperative plan parameter for the ultralow control AFE.

d) *Sensor Interface Between the AFE and Electrodes:* The electrode tissue interface makes a dc offset voltage (up to 200– 300 mV), which must be filtered out by the AFE so as to maintain the saturation of the first stage amplifier. [3]

So as to address the previously mentioned challenges, we introduce a completely coordinated AFE for the WBSNs and implantable SoCs, which takes after a plan approach also; enhancement to satisfy the necessities postured by a number of design parameters. The remaining paper is discussed about the following sections: Section II represents the execution analysis of the design. Section III represents the design of AFE. Section IV represents the design of SAR ADC. Section V draws the conclusion.

II. EXECUTION ANALYSIS OF THE DESIGN

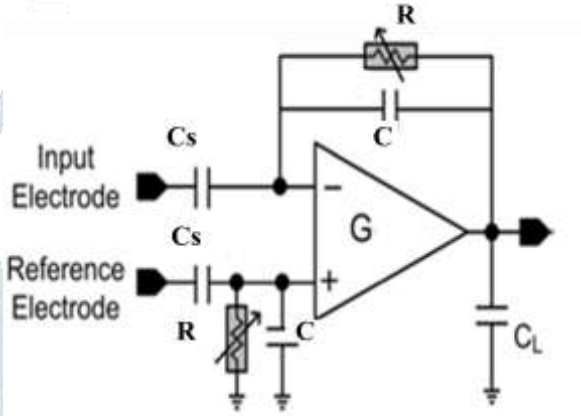

Figure. 2. Frequently used capacitively coupled neural amplifier.

There are so many biosensing amplifiers that are reported in [5]-[22]. In this the single stage configurations implementations are in [5]-[13] and the multi stage implementations are in [14]-[22]. As delineated in Fig. 2, most of these models are capacitively coupled to the account terminals keeping in mind the end goal to reject the dc offset and accommodate the rail-to-rail input common mode range. The intensifier is arranged to give a band pass frequency response, where the high-pass (lower) and low-pass (upper) cutoff frequencies are roughly given by the connection: $f_H = 1/2\pi R\, C$ what's more, $f_L = G/2\pi g_M\, C_L$ (G is the transconductance of the operation transconductance intensifier (OTA), g_M is the intensifier's mid-band gain, and C_L is the load capacitance), individually. The mid-band closed loop gain g_M of the intensifier is set by the proportion of input capacitor C_s to feedback capacitor C ($g_M = C_s/C$) .

With the end goal for one to meet the greater part of the plan requirements, the plan and improvement of the AFE utilizing just a single stage of amplification [5]-[13]. In any case, these works frequently use a vast load capacitor or a band pass channel (BPF) stage to limit the commotion transmission capacity, which is very area inefficient. Additionally, a powerful support stage will be expected to drive the ADC, while using the previously mentioned outlines to manufacture a biosensing AFE.

The objective for the exhibited biosensing front end is to set up a technique that can amplify all the execution tradeoffs. With regards to this objective, the single stage for amplification, filtering necessity for the consequent ADC, programmability, and higher degree of integration are should have been considered for accomplishing a good AFE execution.

III. THE DESIGN OF AFE

The block diagram of the implemented design is shown in the fig. 3. The design consists of low clamor amplifier (LCA), 3^{rd}- order low pass filter (LPF), and analog to digital converter (ADC). The combination of LCA and 3^{rd}- order LPF is defined as AFE.

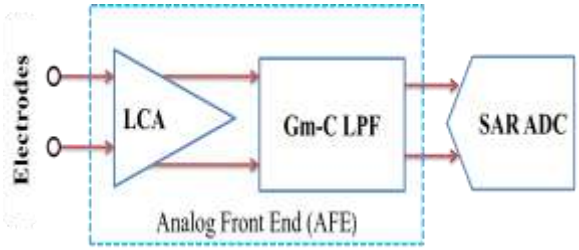

Figure. 3. Block diagram of implemented design.

A. Analog Front-End Design

Maximum noise-power efficiency can only be gained by optimally designing all two major components (LCA, LPF) of the front end. To begin with, in a single stage intensifier, the first organize decides the general clamor execution of the framework as its clamor commitment is fundamentally higher than the other stages. Along these lines, the single stage amplifier, LCA, must be composed for low commotion and high gain at a low bias current. Likewise consider the AFE region alongside the execution parameters appeared in planning and enhancing the framework and the circuit blocks, which were neglected in the past works. Second, a third-arrange LPF is intended to enhance the region of the recording AFE by removing the bulky load capacitors that are utilized as a part of the prior plans to confine the commotion data transmission of the intensifier. Moreover, the programmable LPF likewise acts as an anti aliasing channel organize for different biopotentials, since it is an interface between the single stage biosensing intensifier and the SAR ADC. This dispenses with an extra RC-anti aliasing channel stage to enhance the area of the AFE.

B. Low Noise Amplifier

Figure. 4 show the design of low noise amplifier (LCA). The feedback resistors in the LCA are executed by the nMOS transistors (MT 1– MT 4), giving to a great degree high on-chip incremental resistance (>10^{12}) to incorporate a low-frequency high pass cutoff ($f_{H,LNA}$= 1/2πRC).

Keeping in mind the end goal to confine the noise transfer speed of the pseudo resistors and to lessen the area occupation, an intermediate BPF organize and the huge load capacitors (~tens of picofarad) can be kept away from by judicially picking the arrangement and input capacitors of LCA to meet the criteria recommended. [24]

$$\frac{C_L}{C_S} \ll \frac{2}{3}\frac{f_L}{f_H} \qquad (1)$$

Since the noise contribution from the pseudo resistors is made negligible by fulfilling the disparity (3), the input referred voltage noise of the LNPGA can specifically be composed as an element of the input referred voltage noise of the OTA A1, $v_{in,A1}^2$by the accompanying connection:

$$v_{in,LNA}^2 = v_{in,A1}^2 \frac{(C_S+C+C_{in})^2}{C_s^2} \qquad (2)$$

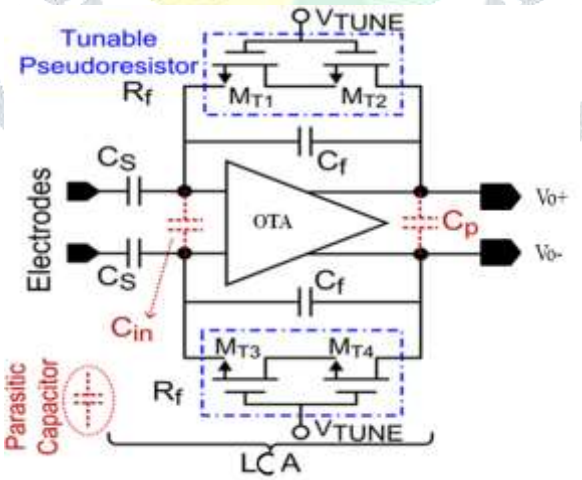

Figure. 4. Design of single stage biosensing amplifier using tunable NMOS pseudo resistors.

The design of LCA (Fig. 4) depends on the enhancement methodology. Due to the extensive range scope of the biopotential signals (several micro volts to mille volts), the principal arrange can stand to have a high yield signal swing. To remember that, a generally high gain of 38 dB (80 V/V) is set for the principal arrange LCA by picking C_s = 9.6 pF and C = 120 fF, individually.

C. Energy Efficient Low clamor OTA

The circuit of operational transconductance intensifier incorporating CMFB is appeared in Fig. 5. The Transconductor center comprises of a degenerated differential pair with auxiliary differential pair strategy [25]. In the proposed circuit the transistor M_{N1} uses an overdrive voltage and the tail current moving through the tail current transistor i.e. M_{N3}. The utilization of folded cascading or some other extra circuit has been avoided. To upgrade the structure for power and noise exhibitions the yield is taken straight forwardly from the channels of M_{N1}. For channels usage the investigation of saturation voltages and threshold voltages for transistors M_{N3} has been completed.

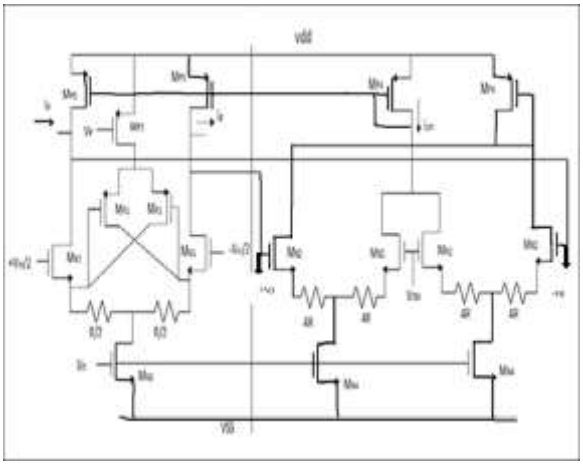

Figure. 5. Complete Transconductor with common mode feed-back amplifier.

To lessen the harmonic distortion components without giving up different parameters, auxiliary differential pair (ADP) strategy has been utilized here. The harmonic distortion can be decreased by other circuit systems however the greater part of those strategies have confinements, for example, significant power utilization, decreased successful transconductance, and restricted frequency response. To outline the idea of auxiliary differential pair strategy, the transconductance bends for settled degeneration resistances and bends for variable degeneration resistance with input voltage can be plotted. By utilizing ADP strategy brings about a leveled transconductance bend and improved linearity. The single finished analog component part of the output current [25] equation becomes as

$$i_d = \frac{G_{MN\_1}}{(1 + G_{MN\_1}R_S)} V_{in} + \frac{G_{MN\_3}}{(1 + G_{MN\_1}R_S)^4} {V_{in}}^3 \quad (3)$$

Where V_{in} is the input voltage supplied to the OTA, R_S is the split resistance,G_{MN_1}, G_{MN_3} are the most significant; is linear transconductance term and undesired third – arrange nonlinear term individually. The linear transconductance term is [25] defined as

$$G_{MN\_1} = \frac{1}{2} \frac{\sqrt{k_p(^{W_N}/_{L_N})I_T}}{1 + \frac{2}{\epsilon_{crit}}\sqrt{\frac{I_T}{W_N L_N K}}} \quad (4)$$

And the undesired third – arrange nonlinear term is expressed as follows

$$G_{MN\_3} = -\frac{G_{MN\_1}}{8\left(\frac{I_T L_N}{K W_N}\right)\left(1 + \frac{2}{\epsilon}\sqrt{\frac{I_T}{W_N L_N K}}\right)^3} \quad (5)$$

Where W_N is width and L_N is length of transistor M_N. I_T Is the tail current, K mechanical parameter and ϵ is basic electrical field [25].

D. 3rd-order Gm-C low pass filter

For the design of the filter the Gm-C approach has been picked due to the simple tuning ability by changing the Gm estimation of the transconductance. The Gm-C channel has a low noise floor however the capacity to deal with vast signal is restricted. In order to chronicle the required an incentive as far as the linearity, the Gm value which relies upon the width, length and the predisposition current of the CMOS transistor must be picked carefully [26]. The operational transconductance amplifier structure is different for various applications. The design of the third order LPF is designed as follows.

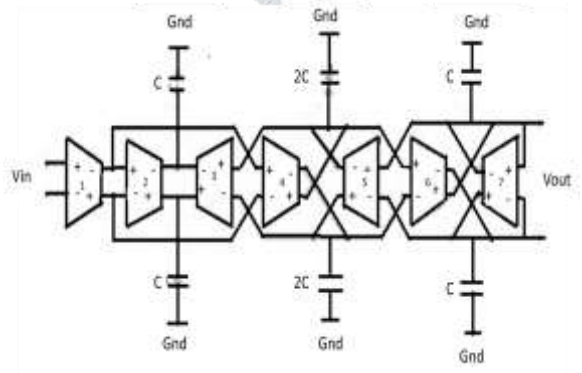

Figure. 6. 3rd Order Gm-C low pass filter circuit.

From the above design it is clear that the low pass filter is designed by using the seven Gm-C OTA's. Here two inputs are given, they are one is positive and the other is negative sine waves. And the output obtained through the LPF is also a linear signal with low frequencies. The main aim for this LPF is not only the frequency but also the gain of the signal. The OTA which has been used in this LPF will also increase the gain of the signal. And it also reduces the power consumption [26].

The design of the OTA is shown in fig. 7. It is chosen because of their various favorable circumstances (counting wide frequency blocks, simple working in blend with OTA transconductance blocks, incorporated circuit usage, and electronic flexibility), OTA channels are

among the best acknowledge of continuous time filters. The transconductance inverter block involves P-type metal-oxide-semiconductor and N-type metal-oxide-semiconductor transistors which prompt diminishment of both the successful chip region possessed by transistors and power utilization.

The transconductance inverter-based OTA channels detailed in examined [27] have two issues: (1) They understand just a single low-pass frequency reaction and (2) they utilize an inverter structure with 112 transistors. Moreover, the filters presented in studies about by likewise have excessively numerous transistors in their inverter-based transconductance blocks.

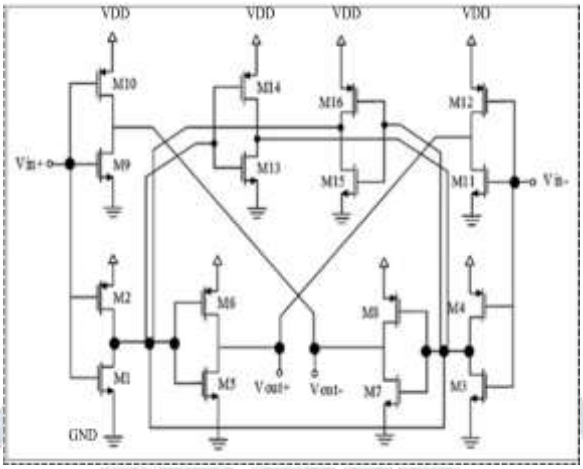

Figure. 7. Design for third-order OTA inverter filter.

The sub threshold inverter transconductance is thus gotten from the accompanying connection in [27] as

$$g_m = \frac{\partial I_D}{\partial V_{gs}} = \left(\frac{1}{\eta V_T}\right) I_{D\,sub-n} + \left(\frac{1}{\eta V_T}\right) I_{D\,sub-p} \qquad (6)$$

Note that there are just eight inverters (16 MOSFETs) in the inverter structure utilized for actualizing the proposed general OTA-C channel. This specific inverter structure was proposed to decrease the space involved (by transistors) in the chip and in addition control utilization in the filter. The design of the OTA-C inverter is done by only eight inverters. This is done because to reduce the area and the power consumption [27]-[33]. By this OTA-C design the gain of the low pass filter is also increased.

IV. DESIGN OF SAR ADC

A successive approximation ADC is a sort of analog to-digital converter that progressions over a reliable basic waveform into a discrete waveform portrayal by means of SAR logic through all possible quantization levels before finally converging upon a digital output for each conversion. The successive approximation analog to digital converter circuit regularly comprises of four sub circuits [34]. They are Successive Approximation Register (SAR), simple voltage comparator, Digital to Analog converter (DAC).

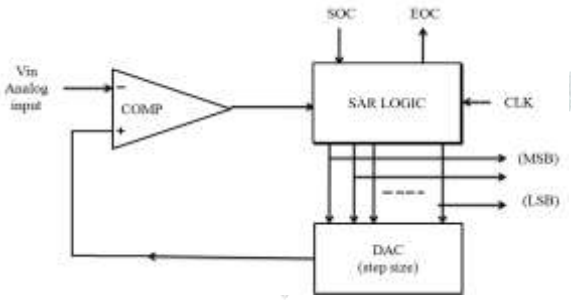

Figure. 8. Block Diagram of SAR ADC.

The most preferred design of comparator is shown in the below figure. In this comparator the most advantage is it removes the dead time issues and offers a high performance. The dynamic power utilization of the circuit is reduced because of the switching transistors and also control transistors are used to charge the output nodes to supply voltage. In the state of reset phase the output nodes are charged to supply nodes. In case of the evaluation phase the result depends on the magnitude of the differential input voltages [35]. During the evaluation phase the transistor which has the higher input voltage will make one of the control transistors high means on and the other control transistor is off.

The advantage of this comparator is enhanced latched transconductance. The response of this comparator, sinusoidal signal is given for one input with variable frequency and same amplitude and the other input is the output obtained from the digital to analog converter. In pre-charge stage both the hubs charge to supply voltage and during assessment phase the output relies upon the differential input voltage [35].

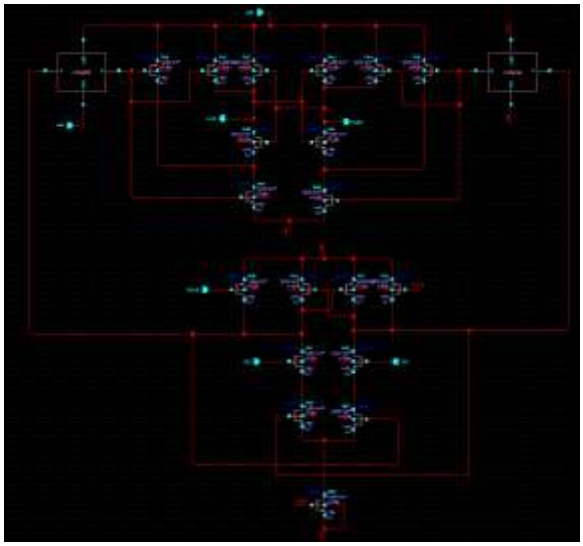

Figure. 9. Comparator.

There one unique structure has been proposed for SAR as shown in Fig. 10. The SAR logic consists of the Sequencer /Code register structure. The structure is made out of a specific number of registers to decide and save the estimation of the bits in an advanced word created by SAR ADC. The structure with the target of lessening their power utilization is considered. These structure work in view of the binary weight algorithm. At the beginning introductory time t_0, which is responsible for deciding the estimation of the Most Significant Bit is set to '1', and puts its value on a bus. After changing over this digital word to equal analog esteem and is compared with sampled input of SAR-ADC. [36]

The yield of the comparator decides if the MSB should be left as '1' or on the off chance that it should be reset to '0' during time t_1. At that point, the second register is additionally set to '1' during time $t_1$and a similar procedure is repeated. Therefore each flip flop is dynamic just for two clock pluses in every conversion [36]. These registers are in a request from the Most Significant Bit to the Least Significant Bit and after the bit value is resolved, this value is saved in its related register. D-flip flop is used in the design of SAR structure.

The schematic of 10 bit sequencer code register SAR is designed. And for the design 20 D flip-flops are utilized. The preset bit is made low for 50nS and high for 500nS to set the main code register flip-flop and reset the remaining flip-flops. The aggregate time of preset is 550nS. The clock of 50nS is utilized. The data input of first flip flop of sequencer register is connected with zero input.

The information contributions of every single flip-flop are connected with comparator output that is zero. The supply voltage is started from the zero level to the voltage of 0.5V.

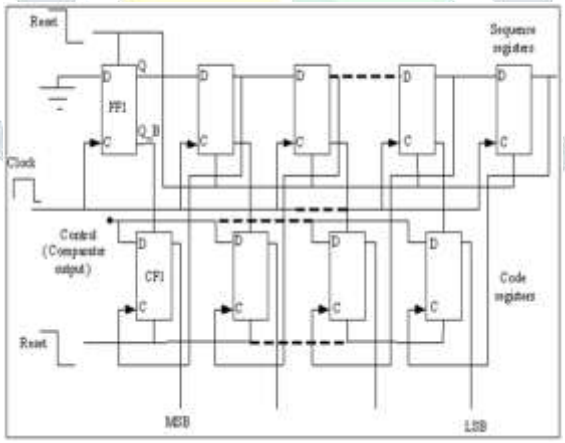

Figure. 10. SAR Logic.

The DAC will create simple likeness this weight. At the point when reset input goes high and clock is activated, output Q of FF1 becomes 0, since D contribution of FF1 sequence register array is grounded and flip flop two (FF2) outs logic High. This low level to abnormal state change of flip flop two (FF2) triggers the code register flip-flop CF1 to store control bus value that is comparator output to its output. At the point when clock signal runs further, the code register flip-flop retains the set value of FF2 output goes to zero. In this circuit positive edge triggered D-flip flop is utilized [36]. This strategy is repeated for every one of the flip-flops until after N-clock cycles a high logic leaves sequencer flip-flop controlling the code register least significant bit flip flop.

The schematic of 10 bit split DAC architecture is appeared in below figure [37]. In this a unit capacitance of 2.5fF is utilized. Attenuation capacitor of 2.5806fF is utilized to isolate LSB capacitor array and MSB capacitor array. On MSB side information bits are D9, D8, D7, D6, D5 and LSB side information bits are D4, D3, D2, D1, and D0. On MSB side every capacitor value is partitioned into two half capacitors associated in parallel and one portion of the capacitance is associated with ground potential and other half capacitance is associated with relating input bit as appeared in Figure. 11.This is done keeping in mind the end goal to decrease the voltage on the best node of the LSB side of the SPLIT DAC. This expanding of node voltage happens when DAC is associated in incorporated SAR ADC [37]. The Figure. 12. Shows the design of 10-bit DAC.

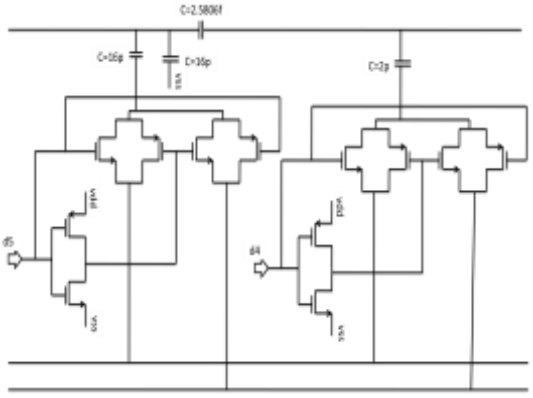

Figure. 11. Design of 2- bit DAC.

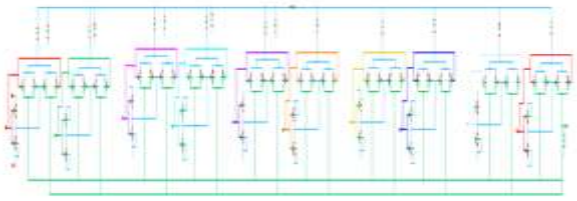

Figure. 12. Design of 10- bit DAC.

Table 1: Parameters of the design in different technologies

CMOS Technology		180nm	45nm
Supply voltage (V)		0.5	0.5
Gain (dB)		52	80
Input referred noise (V_{rms})		124.5n	0.387p
CMRR		84.4	>100
PSRR		45.6	74.6
Power (in watts)	AFE	5.3 μ	133n
	SAR ADC	340.7n	46.04n

V. CONCLUSION

The battery less WBSN and medical implantable gadgets in a WBAN involve a reconfigurable AFE, and it be used in various biosensing applications. In this paper, the design of single stage biosensing amplifier using tunable NMOS pseudo resistors is done for AFE. And the design of each block in AFE and the design of 10-bit SAR ADC are also discussed separately. This is done to maximize the design tradeoff parameters. The proposed design is done in the 45nm technology. The total design is done to reduce the noise and to decrease the power.

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