# SVCL BASED 4T DRAM DESIGN WITH REDUCTION OF LEAKAGE CURRENT

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*Abstract: As we know the leakage power is very important and these is increasing when we going from one technology to another technology generation. CMOS technology improved the level of performance which providing good characteristics such as low cost, low discharge, low power dissipation, high density, low leakage current in the circuits. DRAM used as a cache memory due to the volatile in nature. So that we need to refresh the circuitry and which providing the problem of the leakage current and power consumption. Which can be overcome by proceeding the implementation of DRAM with self-voltage level controllable technique (SVLC). This can be done by using DSCH and Microwind software. This technique help to reduce the leakage current at the lowest point.*

*KEYWORDS - SCVL, DRAM, leakage current, power dissipation.*

## I. INTRODUCTION

The RAM is a sequential memory system which contains SRAM and DRAM both. SRAM is used as a main memory due to the high-speed performance and expensive by cost. But DRAM is used as cache due to its low-cost effectiveness. The random-access memory[1] is one in which the time required for storing (writing) information and for retrieving (reading) information is independent of the physical location (within the memory) in which the information stored. The bulk of memory chip consists of the cells in which the bits are stored in the form of 1 and 0. The cell stores the bit of information as charge on the cell capacitance. Although single capacitor reduces the chip area, the capacitor in a DRAM memory cell leaks meanwhile. The charge in a DRAM cell decays slowly over time via mechanisms [2] like junction leakage, gate-induced drain leakage and power consumption of the circuit. Thus, DRAM needs periodic refresh or it will discharge to zero. For this purpose, careful temporary arrangement of the signal interval and synchronized cyclic refresh is required for proper operation of memory. When cell is storing a '1,'the capacitor is charged to ($V_{dd}$-$V_t$). When cell is storing a '0, the capacitor is discharged to a zero voltage. Due to the leakage effects, the capacitor charge will leak off, and hence the cell must be refreshed periodically. The operation of refreshing of cells is performing in each 5-10ms. So that the dynamic RAM needs continuous flow of power supply.

## II. HISTORY OF WORK

Today's era is to reduce the area and size of the VLSI design. The paper shows a method based on a Capacitance discharge depth is planned [3]. Method to approximation the difference of leakage current due to both intra-die and inter to die gate length development changeability [4]. The research is apprehensive with the investigation of leakage current [5]. The paper introduces a input vector method for leakage current [6].The paper shows a lithography process-aware edge effects improvement method to reduce the leakage current in the shallow trench isolation (STI) [7]. The paper gives the address the rising concern of gate oxide leakage current (gate) at the circuit level [8].The PDP factor needs to be optimized as in CMOS memory cell exhibits two conflicting gauge between power dissipation and circuit delay. In this paper we introduced a super-Diode DRAM cell, which can efficiently reduce power dissipation and a satisfactory PDP value obtained without any hurdle [9]. Memory circuit element includes additional attention to style if discharge current is observed. Varied gate leak reduction methodologies are represented within the literature such as W. K. Luk et. al. offer a unique Dynamic Memory Cell with internal voltage gain[10][11]. H. J. Yooet. al. have developed an occasional voltage high speed self-timed CMOS logic for the multi gigabit synchronous DRAM application[11]. The important fundamentals of recent VLSI devices and principles of CMOS VLSI style [12] have been developed.

In 4T DRAM Cell 4*4 which represents the matrix of rows and columns array. In which Data can be send by using two separate data lines. One is word line and other is bit line. To performing circuit put word line is always one. In figure (a) shows that the 4T DRAM 4*4 circuit diagram.

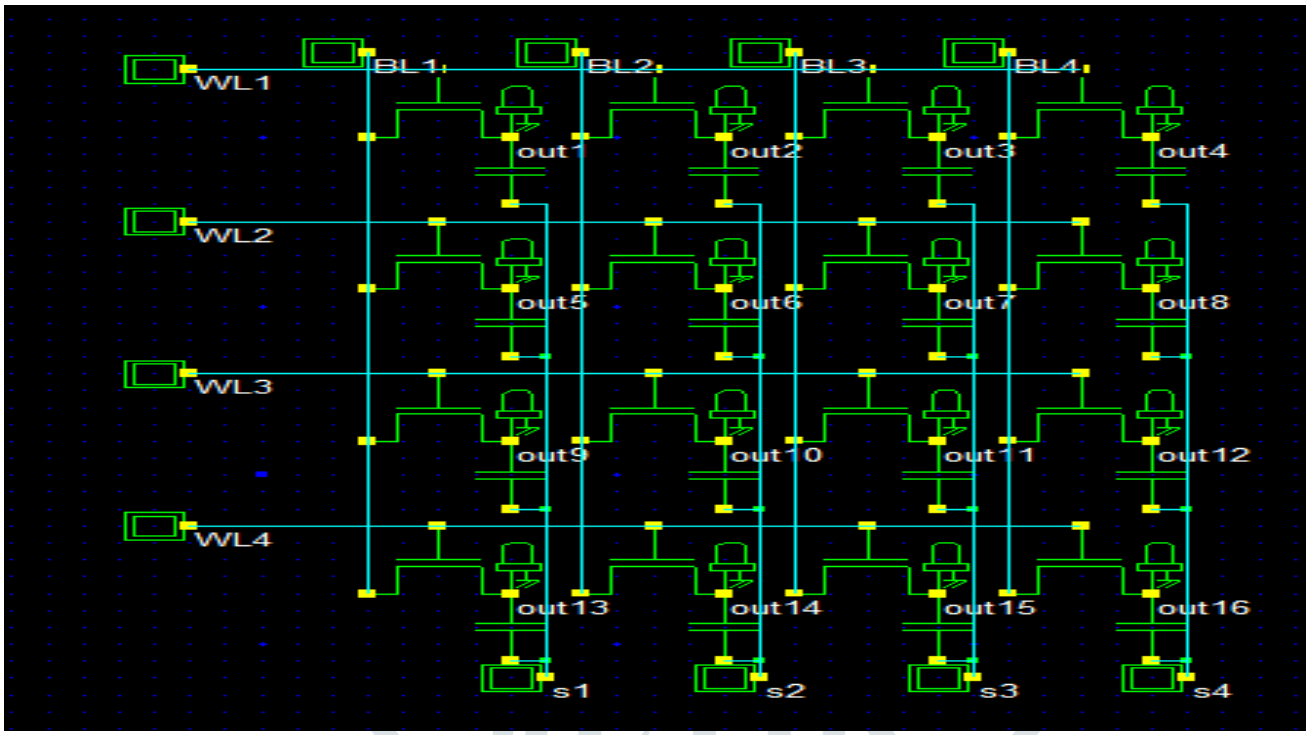


Figure (a) 4T DRAM CELL CIRCUIT

In which WL1, WL2, WL3, WL4 are the word lines and BL1, BL2, BL3, BL4 are the bit lines. To read or write in the circuit is depending upon the performing of operation and for this we have to put the bit lines 1 or 0. In the circuit S1, S2, S3, S4 are the select line which is used as an output. The data to be read or write at which address is directly send or receiving by raised the row and column data line in the circuit. The layout of the 4T DRAM is shown in figure (b).

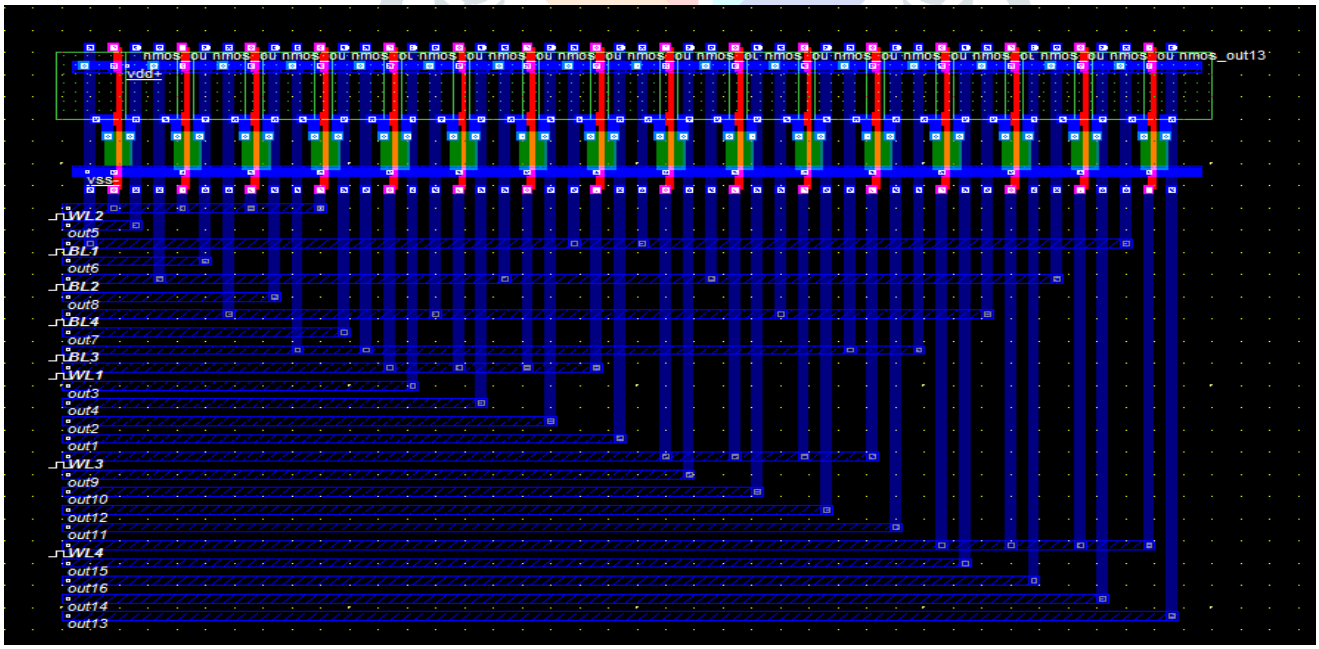


Figure (b) 4T DRAM CELL LAYOUT

## III. PROPOSED WORK

In this paper we are design CMOS 4T dram circuit implementation using self-controllable voltage level technique improving the sub threshold leakage current to the transistor. The circuit is design by using DSCH given as the steady-state voltage $V_{cc}=V_{dd}-V_{th}$. The circuit design array is used a pair of inverters which is connected between the $V_{dd}$ (voltage) and Gnd (ground) terminals. This type of combination is called Self voltage level control technique. In this technique pmos and nmos are connected to bit line and the output select line and which is controlling by using word lines. The SVCL technique the upper level and lower level is used

to control the leakage current in the circuit. The voltage can be swings between in this level due to which the leakages of current is reduced. The Circuit diagram of 4T DRAM using SVCL is showing in figure (c).

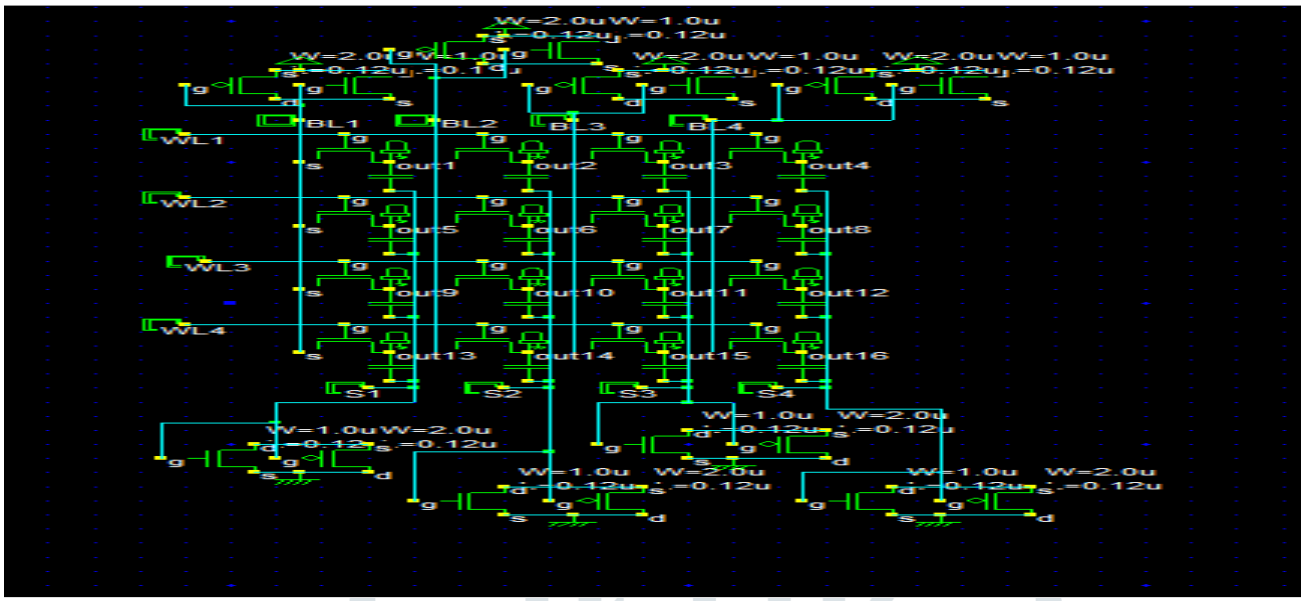


Figure (c) 4T DRAM Circuit using SVCL

The layout design by using Microwind is showing in figure (d). The layout design of four transistors DRAM shows implementation of NMOS using a n+ diffusion layer and gate is implemented by using a poly-silicon and interconnects are implemented by using metal-1 and metal-2[7].In this designing of layout, we are used 0.25um technology in which the 0.002ps scale used. The $V_{dd}$ is the variable Voltage from 3-6v used according to which measurements of the leakage current is shown in the table. By using self-voltage control level technique the delay also reduced which can be calculated easily in it. The power consumption is also lower down in it.

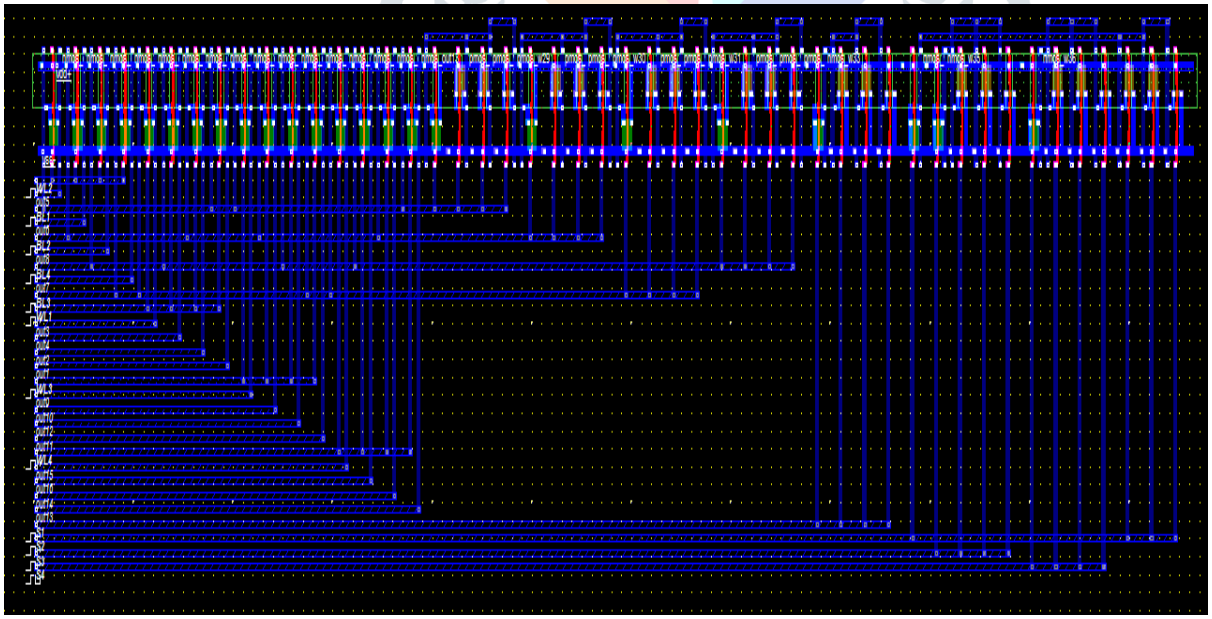

Figure (c) DRAM cell layout with SVCL

## IV. RESULT OF SIMULATION

In this technique the simulation is done by using Microwind. The leakage current in the circuit Using SVCL is decreasing as compared to the 4T DRAM without SVCL. In table shows that result of simulation and experimentally we are using the variable voltage applying in Vdd. The result can be calculated at 20ns timing scale.

**Table (4.1) Leakage Current with variable voltage at 0.25µm scale**

| Input voltage (V) | Without SVCL(20ns) | With SVCL (20ns) |
|---|---|---|
| 3 | 0.568mA | 0.263mA |
| 4 | 0.569mA | 0.263mA |
| 5 | 0.569mA | 0.264mA |
| 6 | 0.570mA | 0.265mA |

As we go the technology then we observed that the changes in the technology scale invented after one by one. If the VLSI technology increases then the size of the chip is decreases. The power consumption and the voltage power supply are decreases. Here we can use 90 nm technology scale. At this scale 1V voltage power supply is used. The low power supply affected the leakage current and power consumption in the circuit. This scale of 90nm is applied into the 4T DRAM SVCL then we will get the low leakage current and power consumption as compare to the 0.25µm technology.

**Table (4.2) Leakage Current with variable voltage at 90nm scale**

| Input voltage (V) | Without SVCL(20ns) | With SVCL (20ns) | Power consumption with SVCL(µW) |
|---|---|---|---|
| 1V | 0.098mA | 0.058mA | 0.664 µW |

## V. CONCLUSION

The performance is the important parameter which is affected the speed and area. In this paper we are used 4T DRAM self-voltage control level technique. This technique is speed up the circuit and reduce the leakage current up to 53%. The simulation is done by using DSCH2 and Microwind2. The variable voltage $V_{dd}$ is used at 0.25µm technology scale. We also measured this results data with 90nm technology scale then we get the low leakage current and power consumption. It means that the as we reduce the chip size, area, voltage and the threshold voltage in the circuit then the leakage current and power consumption is also reduced. This scale is work at low threshold voltage and the performance of the circuit also increased further by changing the W/L ratio in the circuit.

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