

Design and Analysis of Full Adder Circuit in Quantum Dot Cellular Automata Approach

¹Pranali Nile, ²Sayli Mohite, ³Sankit Kassa

¹Student, ²Student, ³Associate Professor

¹Usha Mittal Institute of Technology,

¹S.N.D.T. Women's University, Mumbai, India

Abstract: This paper presents the design of a 1-bit full adder using reduced number of Quantum dot Cellular Automata (QCA) gates. QCA is a newly formed nanotechnology for electronic circuits. QCA consist of a basic component namely a cell which further consists of two electrons and four logically interacting quantum dots. The advantages of QCA are faster speed, smaller size, low power consumption. The proposed QCA full adder circuit saves upto 50% Cell counts and 67% Area composed to the previous designs. QCA Designer 2.0.3 tool has been used for verifying the output of the circuit.

IndexTerms - QCA, Inverter, Majority Gate, Full Adder, QCA Designer.

I. INTRODUCTION

QCA is a combination of Quantum Dot and Cellular Automata. QCA is beyond Complementary Metal Oxide Semiconductor (CMOS). CMOS basically provides micro-scale computing with high density and has low power Very Large Scale Integrated (VLSI) circuit. The CMOS technology has several drawbacks such as high leakage current, power dissipation and limitation of speed in GHz range. Hence CMOS technology is overtaken by QCA.

A cellular automata is a discrete dynamical system consisting of a finite or infinite grid of cells. Each of the cell can be in only one of a finite number of states at a discrete time. Further, the state of each cell in the grid is determined by a transformation rule that factors in its previous state and the states of the immediately adjacent cells. Cellular automata are implemented as a software program. This paper considers how to use QCA in a practical manner.

The paper is organised as follows: QCA basic, Proposed Design of Full Adder, Simulation result and Discussion, Conclusion.

II. QCA BASIC

2.1 Basic four dots QCA

The basic QCA cell consists of four quantum dots in the square array coupled with tunnel phase logic. Among the four quantum dots, two dots consist of electrons. The two quantum dots which consist of electrons are present diagonally. The electron must start from the first dot. The electrons cannot leave the cell, else they are able to tunnel between the dots.

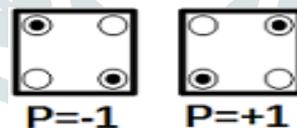


Fig.1. Basic Four dots QCA Cell.

If more than two electrons are placed in the cell, Coulomb repulsion will take place and the two electrons will repel in opposite direction. So, there are two energetically equivalent ground state polarisation namely logic 0 when $P=-1$ and logic 1 when $P=+1$.

2.2 Line of QCA cell

The line of cells is the simplest QCA array. Since the cells are coupled to their neighbours, the same polarisation is present at the ground state of each cell of the line. Hence in these state the electrons are widely separated. The input is applied at the left end of the QCA line and has the same polarisation throughout the line.

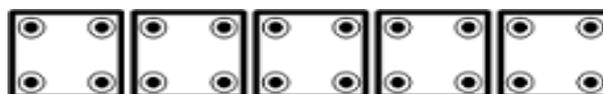


Fig.2. Line or Wire of QCA Cell.

In the line of QCA cell upto 10 cells are manageable to give the same logic and after 10 cells logic may differ either 0 or 1. Since the cell communicate with their neighbouring cell, so there is no need of long interconnects lines. The input is applied to the cell at the edge of left end of QCA cell and the output appears at cell at the edge of QCA array.

2.3 Basic Gates of QCA

In the basic gates of QCA the computation becomes a task of applying the inputs that further put the system in to an excited state and then relaxing it in a new ground state. The mapping of a combinational logic problem onto a QCA system is accomplished by finding arrangements of QCA cells that implement the logic functions as AND,OR,NOT.

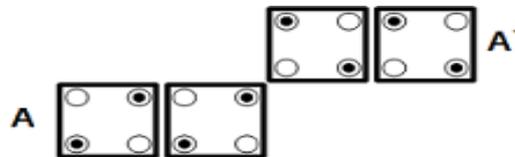


Fig.3. QCA Inverter.

In an inverter design as shown in Fig.3, the input is first split into two lines of cells and then they are brought back together at a cell that is displaced by 45 degrees. In the first line of QCA cell, which is the input line of QCA cell it consist of 3 cells which have logic 1 and then the QCA inverter takes place which then comprises of logic 0. Hence the output logic comes out to be logic 0 after the second line of QCA cell which also presents 3 cells in it.

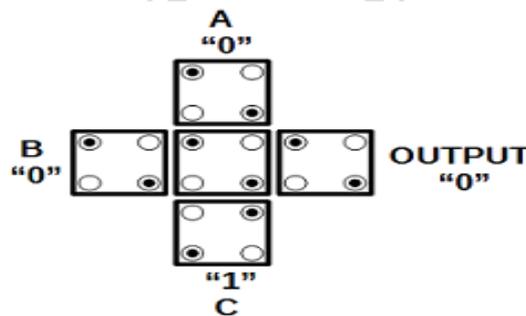


Fig.4. 3 Input QCA Majority Gate.

In 3 input majority gate design as shown in Fig.4, the 3 inputs are given such that the majority polarisation wins and then propagated to become the output. Among these inputs one of the input can be used as a programming input to select the AND or OR function. The programming input for logic 0 is AND gate and the programming input for logic 1 is OR gate. Thus, it is possible to implement all combinational logic functions with the combination of majority gates and inverters.

2.4 QCA Components

- Inverter- Inverter is a cell arranged in diagonal manner. If the input is given as 0 then the output comes out to be 1 and vice-versa.
- 3 input majority gate- This gate is composed of five QCA cells with a cross shaped structure. In this 3 input are given and one output gate is present. Among the 3 inputs the most preferred input is given as the majority gate. The gate with one input fixed to 0 or 1 acts as an AND or OR gate.
- Wire- A cell of a wire is a line of a QCA cell. If input is 0 then output comes out to be 0 and if the input is 1 then output is also 1.
- Crossover- The collection of two intersecting QCA wires is known as crossover. This architecture uses two line or wire of QCA cell with a cross shaped structure.

The below Table 1 shows the QCA components symbol listed in abstract symbol and the actual symbol.

Table 1. QCA Component Symbols.

QCA Primary Component	Abstract Symbol	Actual
Inverter		
3 Input Majority Gate		
Wire		
Crossover		

2.5 Clocks in QCA

Cells can either be in one of the two states and the change of state in the cell is recognised by the state of its adjacent neighbours. The direction in which the state transition occurs in QCA cells is a method to control data flow. So the clock in QCA provides powering the automata and controlling the data flow direction.

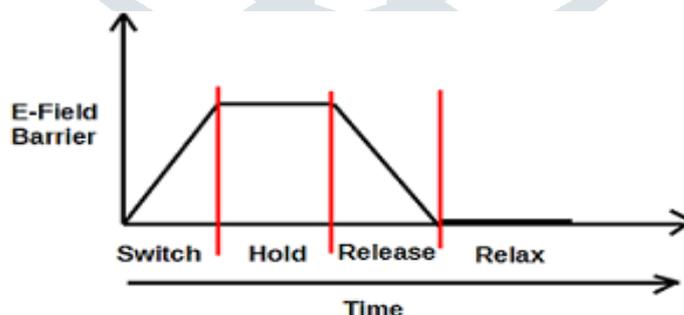


Fig.5. QCA Clock phase.

A QCA clock consists of 4 stages in the tunneling barriers of the cell. In the first stage, the tunneling barrier switches ON and starts to rise. In the second stage, the tunneling barrier helps to prevent electrons from tunneling. In the third stage, the tunneling barrier starts to fall down and hence reduces the high barrier to lower down. In the fourth and final stage, the tunneling barrier allows electrons to freely tunnel again.

In short, when the clock signal is high electrons are free to tunnel.

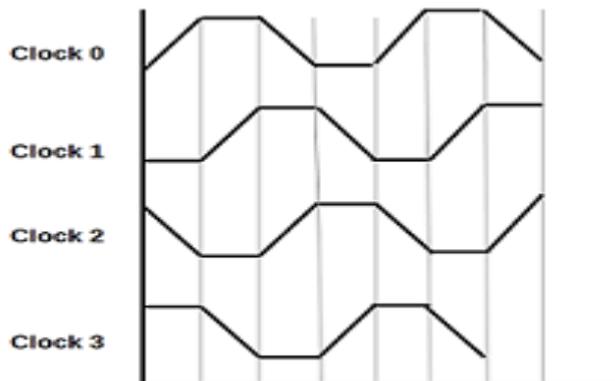


Fig.6. QCA Clocks.

In below figure, the clock-zones of vertical and horizontal wires are marked with 1 and 3 respectively. The central cell can be marked as either clock 1 or 3.

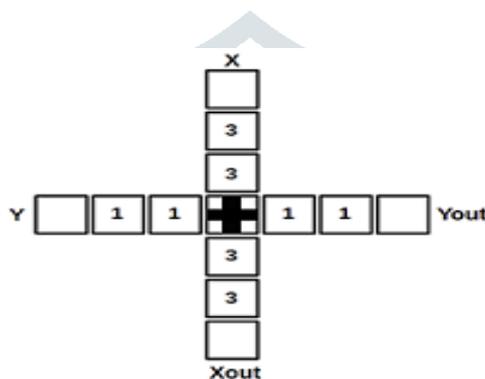


Fig.7. Clock-zone based on crossover gate.

III. PROPOSED DESIGN OF FULL ADDER

The Full Adder performs the addition of three boolean variables and produces two outputs as sum and carry. Let A, B, Cin be the three variables.

The truth table of Full Adder is given in Table 2.

Table 2. Truth Table of Full Adder

A	B	Cin	Sum	Carry (Cout)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The sum and carry is given as:

$$\text{Sum} = A'B'Cin + A'BCin' + AB'Cin' + ABCin \tag{3.1}$$

$$\text{Carry (Cout)} = AB + BCin + CinA \tag{3.2}$$

The circuit diagram of Full Adder using Boolean logic gates is given as:

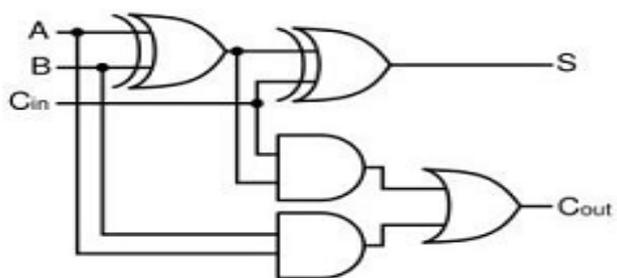


Fig.8. Block Diagram of a Full Adder using Boolean Logic Gates.

IV. SIMULATION RESULT AND DISCUSSION

Inputs A, B, Cin are used to initialise the cellular automata cell to a particular value. Sum and Carry (Cout) are two outputs for simulation of full adder.

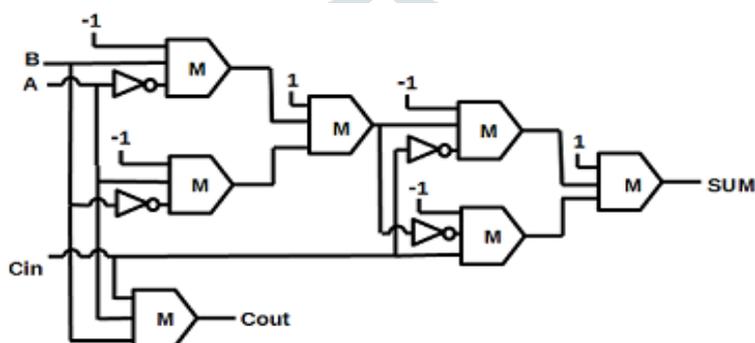


Fig.9. Block Diagram of a Full Adder using QCA Gates.

In this implementation the cells are arranged in the required clock phase as per the majority gate. For each AND values the majority gate is provided by the same clock as Clock 1. For each OR values the majority gate is provided by the same clock as Clock 3. The input A and Cin are placed inside the cells so to overcome this and bring the two input outside the cells and make a majority gate to simulate the outcome of carry, the crossover gate technique is used. The crossover gate is used two times by the clock zone 1 and 3 placed in horizontal and vertical manner respectively for each gate. For simulating the sum and carry, the same clock is given as Clock 3.

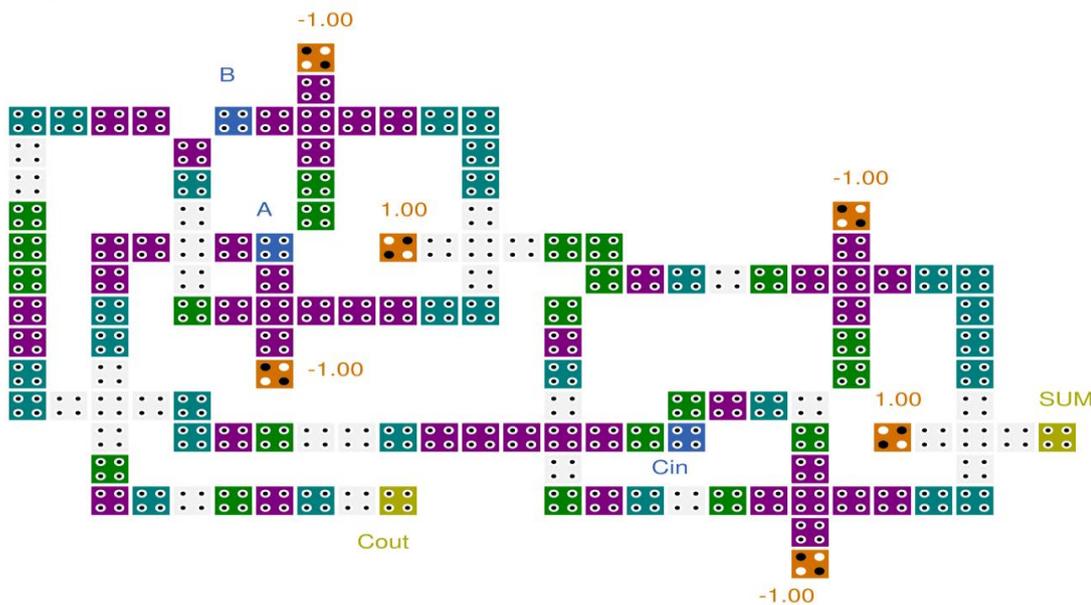


Fig.10. Implementation of Full Adder using QCA Designer 2.0.3

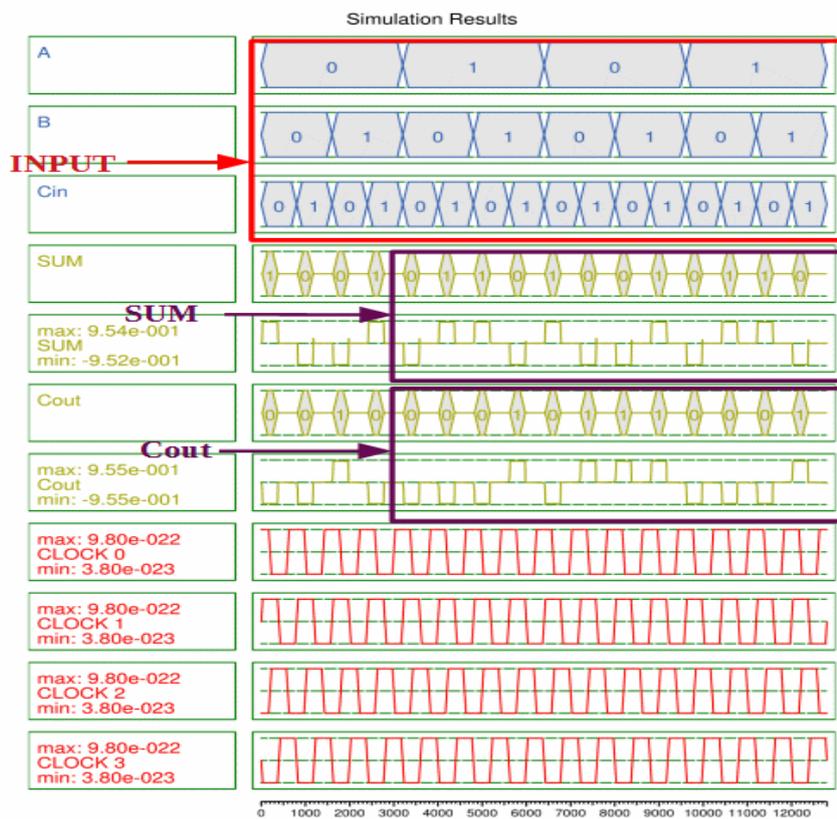


Fig.11. Simulation of Full Adder using QCA Designer 2.0.3

The Table 3 contains the comparison of QCA full adders for some previously designed QCA bit adders. The cell count and area for given references 2, 3, 9, 13 are 292, 220, 180, 150 and 0.62, 0.36, 0.22, 2.25 respectively. The 'Proposed' design consists of 135 cell count and 0.21 as the area, which is compared less than the other full adder design.

Table 3. Comparison of QCA Full Adders

QCA References	Cell Count	Area (μm^2)	Layer Type
2	292	0.62	Coplanar
3	220	0.36	Coplanar
9	180	0.22	Coplanar
13	150	2.25	Coplanar
Proposed	135	0.21	Coplanar

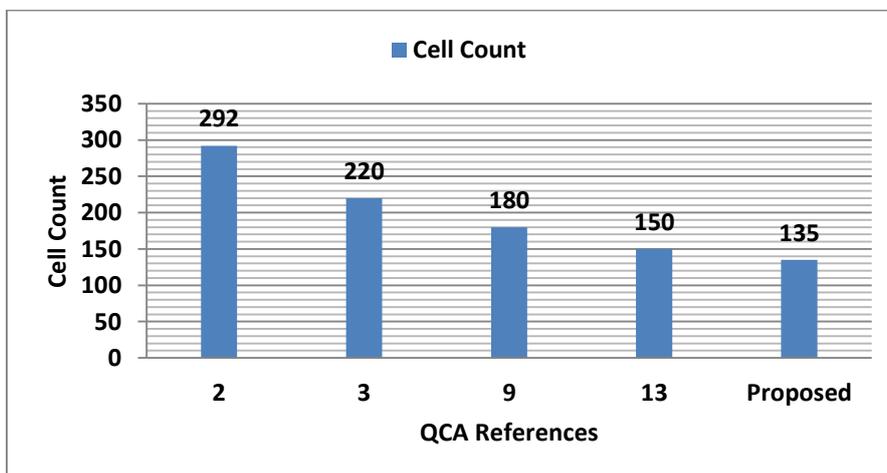


Fig.12. Number of cells of Proposed Full Adder and previous design

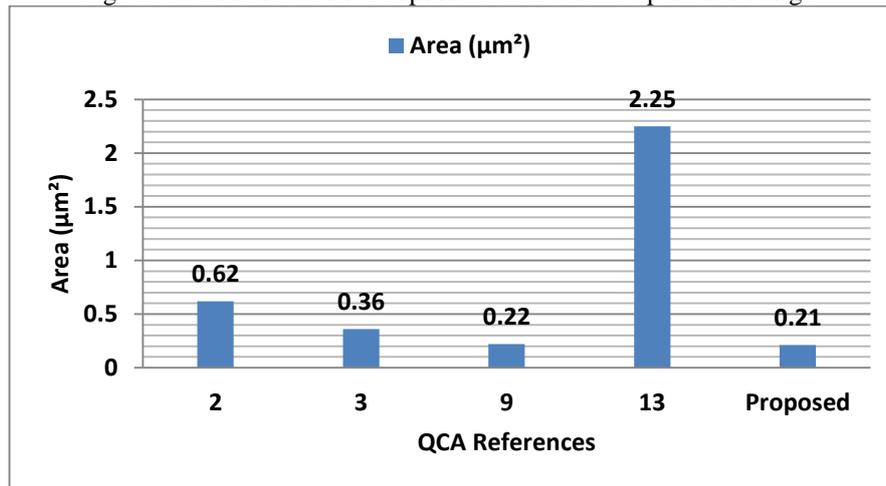


Fig.13. Area usage of Proposed Full Adder and previous design.

V. CONCLUSION

In this paper basic QCA cell, QCA wires, logic gates and clocking has been discussed. The paper is based upon a single layer 3 input design full adder. The proposed full adder circuit utilized only 135 numbers of total QCA cells and $0.21\mu\text{m}^2$ area in its design. This saves 50% total cell counts and 67% total area compared to previous circuits. So, the QCA circuits must have faster speed, smaller size and low power consumption. If the algebra equation produced during output will be simpler then the circuit will be efficient in cell count. By using proper clocks, one can reduce the delay time for fast circuits.

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