Design Analysis of 1-bit Comparator using different Logic Techniques

[1]Ashima Singh, [2]Akanksha Mishra, [3]Rajesh Mehra, [4]Srishtee Chaudhary
[1]Student, [2]Student, [3]Professor, [4]Lecturer
[1]Department of Electronics & Communication Engineering,
[1]NITTTR, Chandigarh, India

Abstract : The research work illustrates various designing techniques used in designing a productive 1-bit Magnitude Comparator Logic circuit. The comparator has been designed using Conventional CMOS Logic and further compared with two different logic design techniques, viz. Gate Diffusion Input Logic and Pass-Transistor Logic. The GDI-Logic based Comparator employs 4 P-channel MOSFETs and 4 N-channel MOSFETs. The total area to be utilized by the comparator based on GDI Logic is significantly less as compared to the conventional design. The software tools used in schematic designing and simulation of 1-bit comparator are DSCH-3.1 and Microwind-3.1. Circuit is designed using DSCH-3.1 and further simulated using Microwind-3.1 utilizing 45 nm fabrication technology. The software tools cater the parametric investigation of design. The design methodology employed in designing the comparator is Auto-Generated. Analysis of different Logic techniques have been done on the basis of basic performance parameters, viz. power consumed, power dissipated, delay, area covered and number of transistors used. The paper presents three Logic Design approaches for 1- bit Comparator design and analytical scrutiny based on various above said parameters. The results reflected that GDI Logic provides a superior quality of design approach in comparison to the conventional CMOS and PTL. The GDI logic design provides an efficient design which consumes less power of approximately 85.9% and delay of about 42.1% which is lesser than that of conventional MOS design. GDI-Logic has proved to be even better than PTL as it consumes less power of around 43.4% and delay of 89% lesser than that of PTL.

Index Terms **- CMOS, Delay, GDI Technique, Magnitude Comparator, Pass Transistor Logic, Power Dissipation, Shannon Theorem, VLSI design.**

I. INTRODUCTION

Comparator is an electronic device that compares any two n-bit binary numbers and generates result on the basis of their compared values. The three possible outputs generated by Comparator are $I_1=I_0$, $I_1>I_0$, $I_1<I_0$ which suggests the comparison in magnitude of two numbers i.e. I_0 and I_1. The basic block representation of n-bit magnitude comparator is illustrated in **Fig.1** [1]. Applications of comparator circuit are primal in the measurement and instrumentation circuits. Some basic application of comparator is Analog to Digital convertor, Function generator, Signal Detection and Neural Network etc.

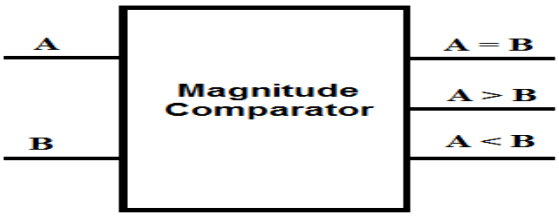

Fig.1: Representation of n-bit Comparator

II. LOGIC DESIGN APPROACH

With the advancements in technology, scaling of electronic devices has become a prior need and chip miniaturization has become a key subject in research area. In the realm of VLSI technology, main retarders stood in circuit designing are power consumption, power dissipation, area occupancy etc. So, these parameters are crucial design issues which play prime role in Very Large Scale Integration. Nowadays, it has become mandatory to fabricate large number of components on a small chip in order to scale down electronic devices. Important parameters that determine popularity and commercial demand in the market are chip size, number of transistors utilized, power dissipation, power consumption and speed. There are various ways by which CMOS comparators can be designed. This paper deals with three different design techniques, viz. Conventional, PTL and GDI Logic which serves an efficient solution in achieving the required functional specification. Evaluation of performance parameters is done by employing the above said design techniques. Each approach shows advancement in area utilization, speed of operation, power consumption, power dissipation and transistor count. The parameters may improve with different design approaches. So, appropriate selection of logic technique is very crucial in order to achieve desired results. The main aim of experimenting all

design techniques is to obtain a compact design structure with minimal transistor count to carry out desired logic functions. This consumes less power, acquires less space, produces low delay and attains an increased speed [2].

Comparator designed using combinational logic gates have very high operating speed but the area occupancy is large due to large transistors count which ultimately results in high cost incurrence. Power consumption is measured in terms of Dynamic Power and Static power. Dynamic power is a result of switching power and short circuit power whereas static power results due to the leakage current produced by parasitic transistor. Dynamic power and Static power adds up to contribute in the total power consumption. The drawback involved is that dynamic power becomes impossible to eliminate as it results due to computing operations [3].

The average dynamic power dissipated (P_d), is defined as the energy required in charging and discharging circuit capacitance given by $C_L V^2_{dd}$ per unit switching time (t_p) as shown in the equation(1) [4].

$$P_d = C_L V^2_{DD} / t_p \quad \ldots (1)$$

The total power dissipated given by 'P_T' is defined as the sum total of static, dynamic and short circuit power dissipations.

$$P_T = P_{st} + P_{dy} + P_{scd} \quad \ldots (2)$$

Symbol τ_p denotes the average propagation of input signal to reach its output through CMOS circuit

$$\tau_p = (\tau_{Phl} + \tau_{Plh})/2 \quad \ldots (3)$$

Where,

τ_{Phl} = Propagation delay from input to output of a signal as it transits from high to low.

τ_{Plh} = Propagation delay from input to output of a signal as it transits from low to high.

From above equations, Power Delay Product can be defined as,

$$P_{dp} = 2P_{avg} * \tau_p \quad \ldots (4)$$

Where,

P_{dp} = Power Delay Product

III. CMOS COMPARATOR

Conventional CMOS design technique makes use of a large number of transistors. In this technique transistors transmit logic 'high' or logic 'low' from input to output. Due to more transistor count, area occupancy is relatively higher along with high power consumption and power dissipation. As a result of this, speed of the circuit reduces to a great extent.

The Boolean expression for the comparator outputs can be realized through Truth table provided in **Table 1**.

Table 1: 1-bit Comparator Truth table

I_1	I_0	$P(I_1>I_0)$	$Q(I_1= I_0)$	$R(I_1< I_0)$
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

From the Truth table, Boolean expression for different outputs can be expressed as:

$P= I_1 I_0'$ ……. (5)

$Q= I_1 I_0 + I_1' I_0'$ ……. (6)

$R= I_1' I_0$ ……. (7)

The circuit implementation of logic functions given in Table (2) using combinational logic gates is shown in **Fig.2**.

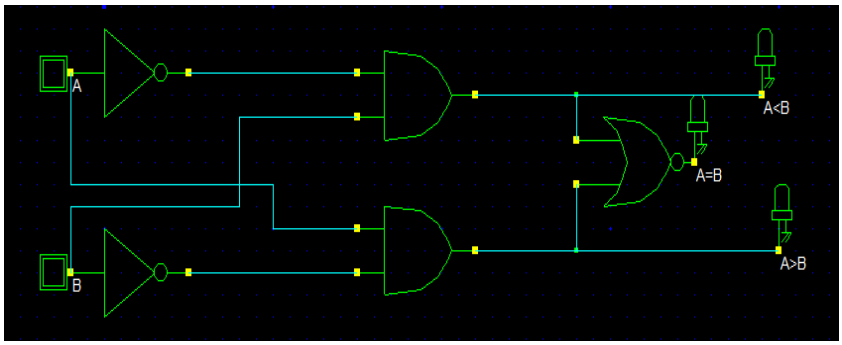

Fig. 2 Logic Circuit Diagram of 1-bit Comparator

CMOS is composed of two transistors, viz. NMOS and PMOS which are connected in pull-up and pull down configuration. PMOS transistor passes a strong logic '1', so it's source terminal is connected to voltage 'V_{DD}' and source terminal of NMOS is connected to the ground as it passes strong logic '0'. The connections of PMOS and NMOS in pull-up and pull-down configuration is shown in the **Fig.3** [5].

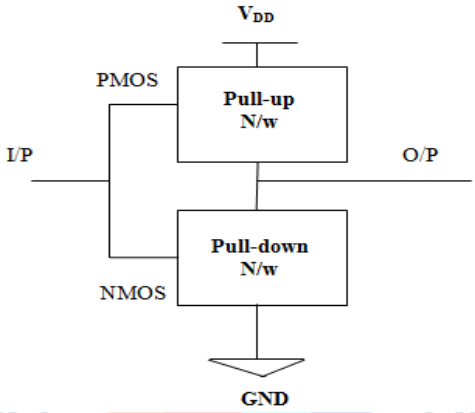

Fig. 3 CMOS inverter in pull-up and pull-down configuration

IV. LOGIC DESIGN TECHNIQUES

The paper incorporates two design techniques which are as follows:

1) *Gate Diffusion Input (GDI) Logic*
2) *Pass-Transistor Logic (PTL)*

GDI logic

It is a special design technique that uses less number of transistors to design digital combinational circuit which consumes very low power. With the reduction in transistor count, there is great reduction in power consumption, propagation delay and area required for circuit design while maintaining low complexity. As a result of this, speed of the circuit enhances [6].

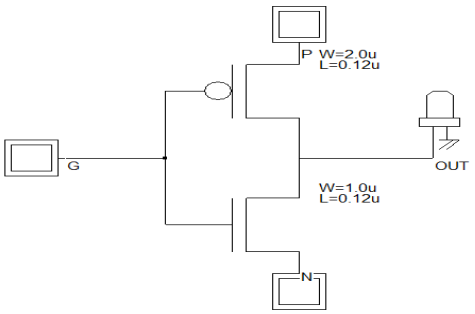

Fig. 4 The basic GDI cell

"Figure 4" presents the basic design of GATE DIFFUSION INPUT LOGIC cell which comprises three inputs, namely G, P and N. Input 'G' is the Gate common to N-MOSFET and P-MOSFET; 'P'is the input to source of P-MOSFET and 'N' is the input to source of N-MOSFET. The GDI-Logic cell is composed of two MOS transistors connected in pull-up and pull-down configuration, such that a large number of complex logic functions can be realized and hence implemented using only two

transistors [2]. Different functions that can be implemented utilizing the GDI-Logic are provided in **Table 2**. Since, number of transistors gets reduced; the circuit complexity is also reduced. Hence, GDI Logic is considered the fastest in performance while consuming low power.

Table 2: Function implementation using GDI-Logic

G	P	N	OUTPUT	FUNCTION
A	B	0	A'B	X
A	1	B	A'+B	Y
A	B	1	A+B	OR
A	0	B	AB	AND
X	B	A	A'B+AC	MUX
A	1	0	A'	NOT

PTL logic

Pass-transistor logic is also known as transmission-gate logic. This technique uses MOSFET as a switch. The fundamental difference between pass-transistor logic and the CMOS logic is that the source and drain terminals of CMOS is connected to input variables rather than the logic (i.e. logic 'high' or logic 'low') as shown in **Fig.5**. In PTL, any logic to be implemented is first minimized using Shannon's Theorem and then utilized in designing. Hence, a large logic circuitry can be reduced such a design technique as it employs lesser number of transistors and is sufficient to perform any logic function. As a result, the circuit acquires lesser area on chip thereby enhancing operational speed [7].

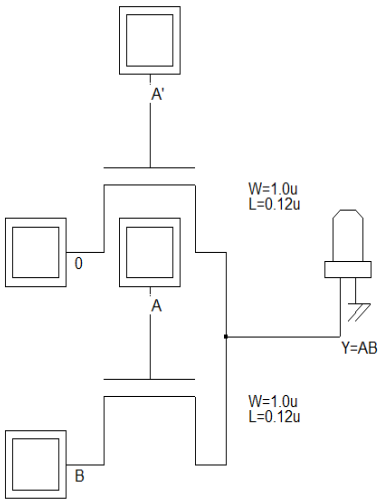

Fig. 5 Symbol for AND Gate using PTL

V. COMPARATOR SCHEMATICS

Comparator using conventional CMOS logic is designed on DSCH-3.1 as shown in **Fig 6** in which In1 and In2 are used as inputs and Out1, Out2, Out3 are used as outputs. In the complete circuit, 8 CMOS transistors (4 PMOS & 4 NMOS) are used to implement XNOR GATE. In order to implement AND gates, 8 CMOS (4 CMOS for each AND gate) and 4 inverters employing 2 CMOS each are used. The total number of transistors used are 24 (12 PMOS & 12 NMOS) [8].

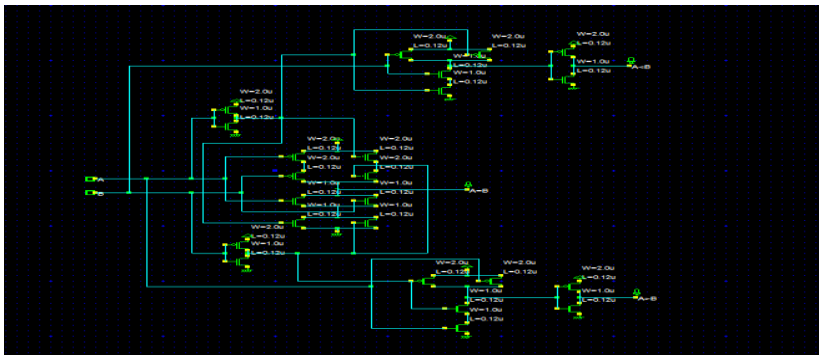

Fig. 6 Circuit implementation of 1-bit comparator using Conventional CMOS Logic

In this paper two distinct Logic Techniques are introduced, viz. GDI-LOGIC & PASS-TRANSISTOR LOGIC which utilizes less number of transistors to perform a particular function. The schematic of GDI-based comparator design using DSCH-3.1 is as displayed in **Fig. 7**. The transistors used in designing XNOR logic is 4 (2 PMOS & 2 NMOS). Total number of transistors employed in designing 1-bit comparator is 8.

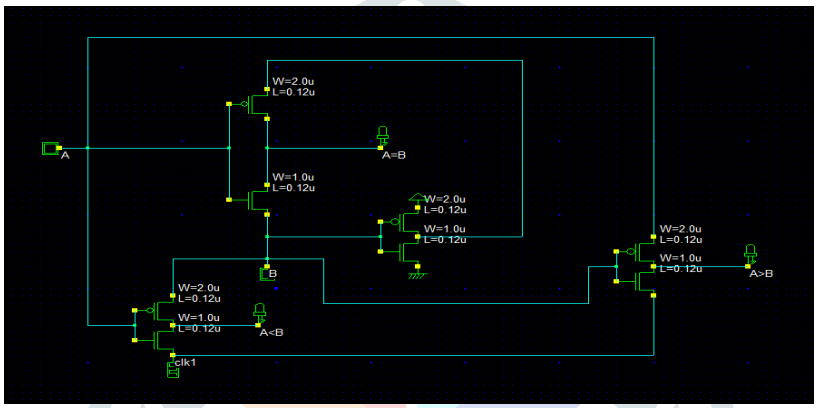

Fig. 7 Circuit implementation of 1-bit comparator using GDI Logic

Pass-Transistor Logic is another proposed technique that is efficient in reducing the area of chip. The schematic diagram of PTL-based comparator using DSCH-3.1 is shown in **Fig. 8**.The transistors used in implementing XNOR gate is 6 (3 PMOS & 3 NMOS). Total number of transistors employed in designing 1-bit comparator is 8.

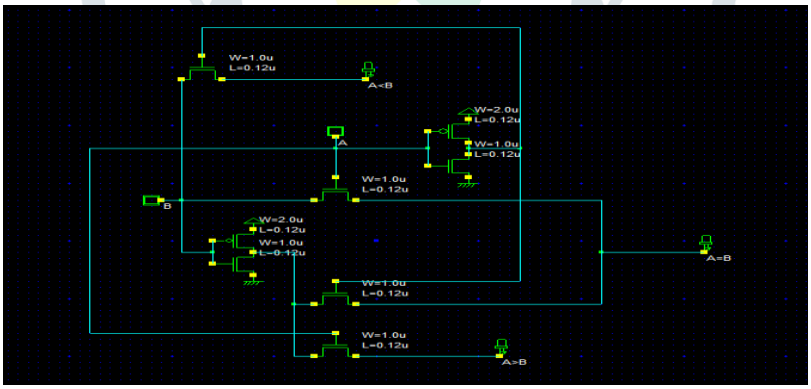

Fig. 8 Schematic of 1-bit comparator using PTL-based Logic

VI. SIMULATION RESULT

Layout Design & simulation waveform of conventionally designed1-bit comparator is presented in **Fig. 9a** and **Fig. 9b** respectively.

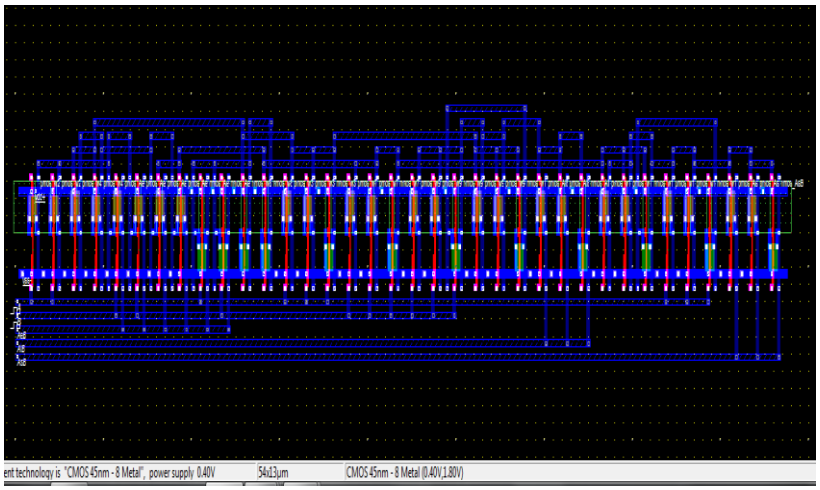

Fig 9a

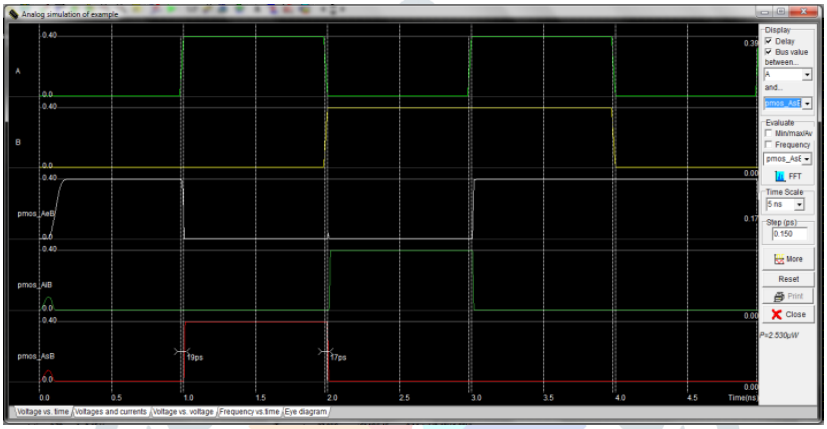

Fig. 9b

Power dissipation and area covered in this design technique is comparatively larger as shown in the **Fig. 9c** & **Fig. 9d** respectively.

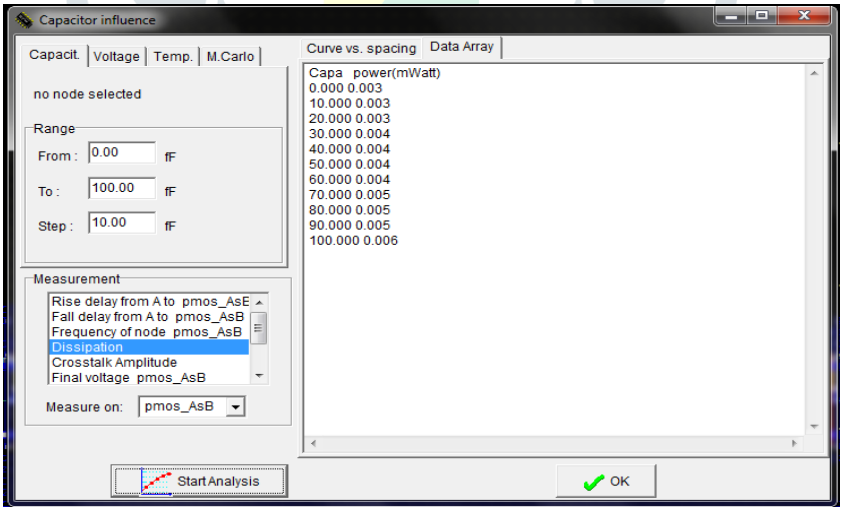

Fig. 9c

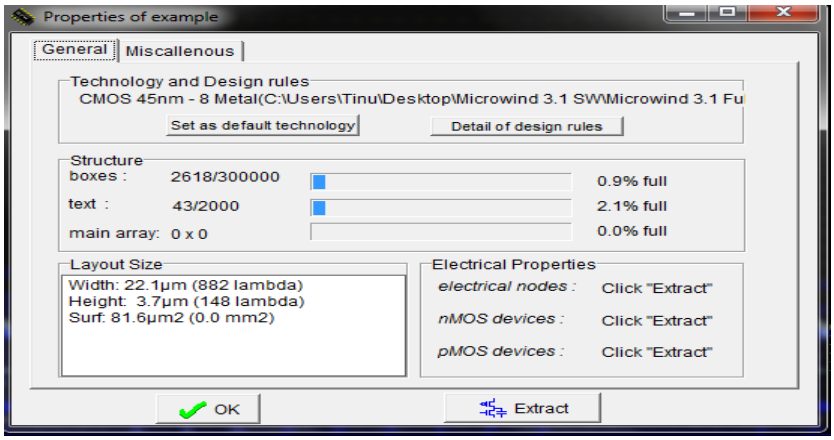

Fig. 9d

Layout Design & Simulation waveform of GDI-based designed 1-bit is shown in **Fig. 10a** and **Fig. 10b** respectively.

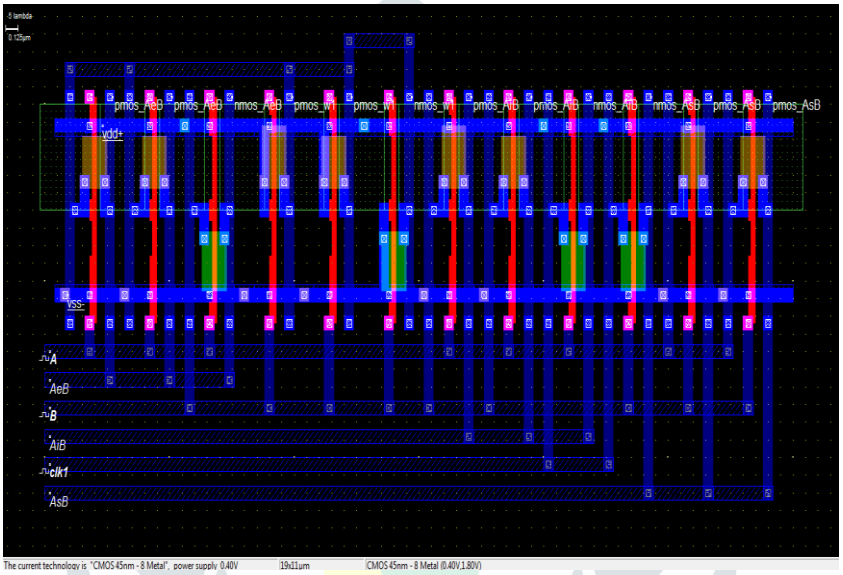

Fig. 10a

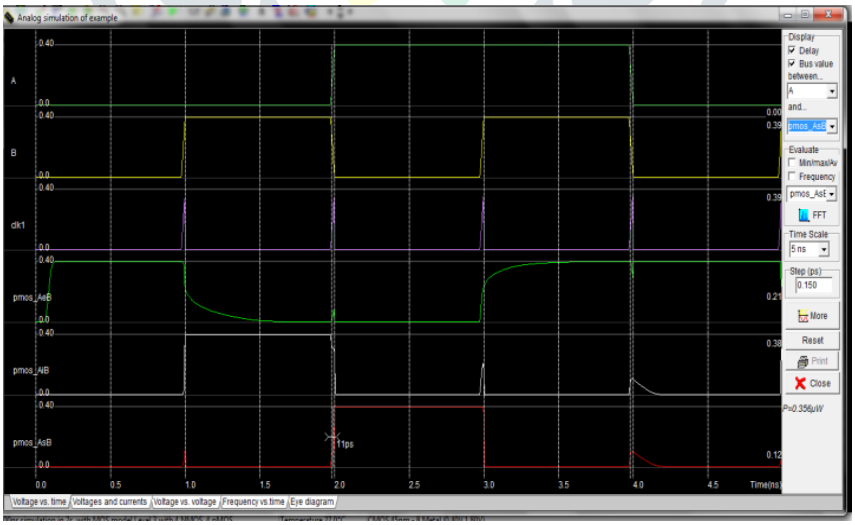

Fig. 10b

Power dissipation and area covered in GDI-based design is comparatively lower than Conventional design and PTL logic design as shown in **Fig. 10c** & **Fig. 10d** respectively.

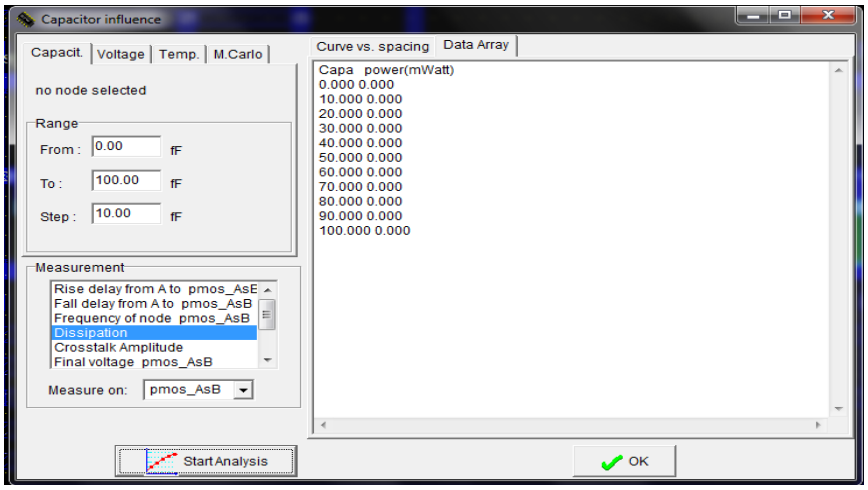

Fig. 10c

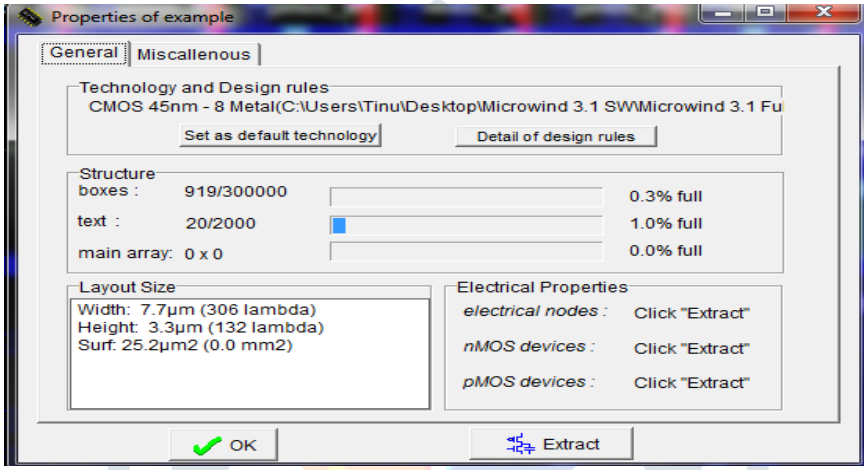

Fig. 10d

Layout Design & Simulation waveform of PTL-based designed 1-bit comparator is presented in **Fig. 11a** and **Fig. 11b** respectively.

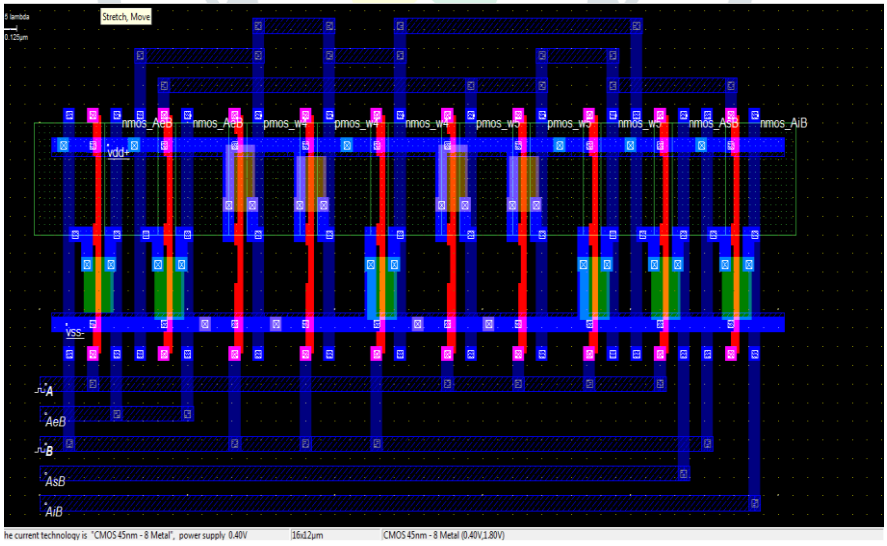

Fig. 11a

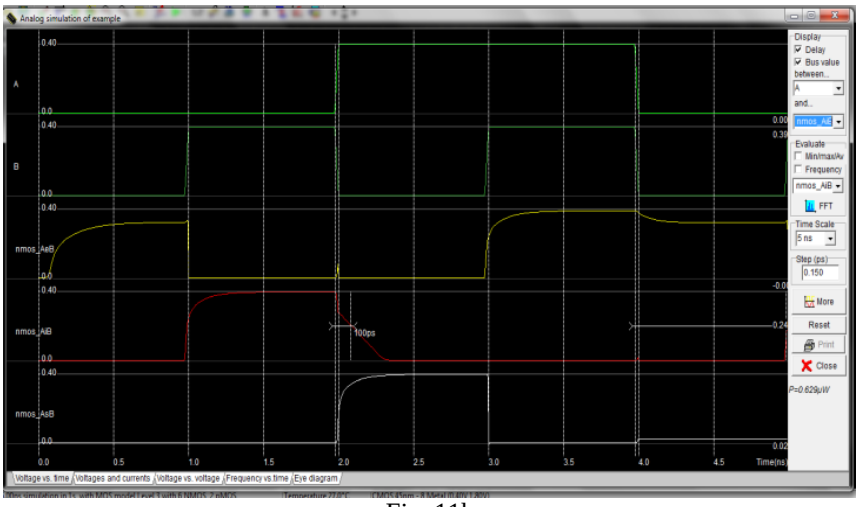

Fig. 11b

Power dissipation and area covered by MOS transistors using PTL design technique is shown in the **Fig. 11c** & **Fig. 11d** respectively.

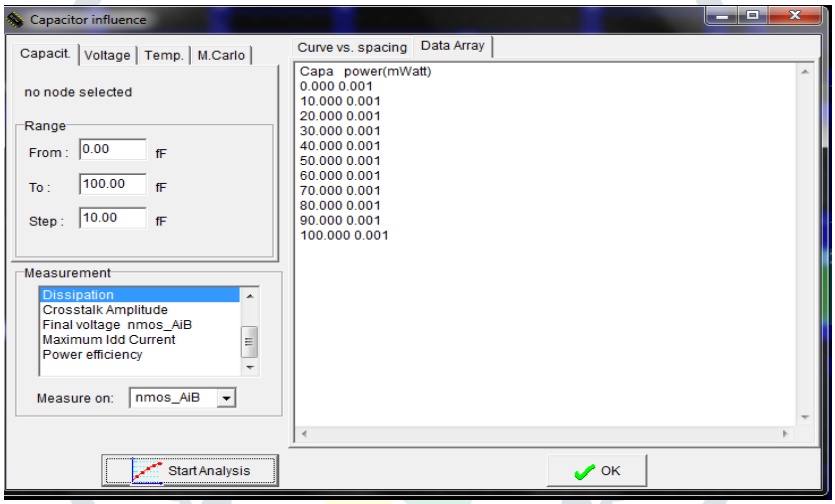

Fig. 11c

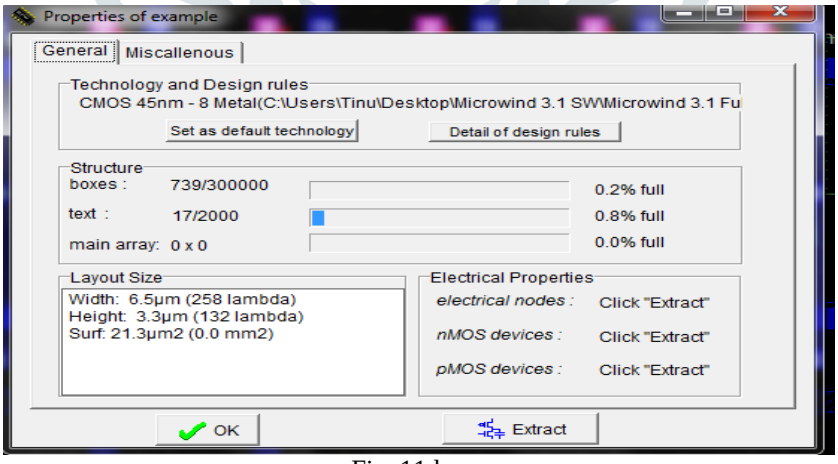

Fig. 11d

On simulating the designs of 1-bit comparator using different logic techniques, various parameters have been observed and plotted in the Comparison **Table 3** for Comparative Analysis. The comparison is done on the basis of Area covered, Power consumption, Power dissipation, Delay and number of transistors used. The technology used to simulate the designs is Auto-generated.

Table: 3 Analysis and Comparison between different Logic design techniques

Design Style	Features				
	Area	***Power Consumption***	***Power Dissipation***	***Delay***	***Transistor count***
Convenctional	81.6 μm^2	2.530µW	0.006 µW	19psec	24
GDI	25.2μm^2	0.356 µW	0.000 µW	11psec	08
PTL	21.3 μm^2	0.629 µW	0.001 µW	100 psec	08

It is fairly pronounced from the Analysis and Comparison **Table (3)** that the Power Consumed by GDI-based design is as around 85.9% less as compared to the Conventional design. On comparing with PTL-based design, it is approximately 43.4% less in GDI- based design. Delay parameter is the least in case of GDI which means it develops the fastest comparator. Number of Transistors used in PTL DESIGN & GDI DESIGN are same and also very few as compared to the Conventional Design which reduces the area. The efficient reduction in area provides a compact device with low power consumption those results in low power dissipation. By considering all the above parameters, it is clear that GDI-based design is far more efficient than Conventional logic and Pass-transistor logic.

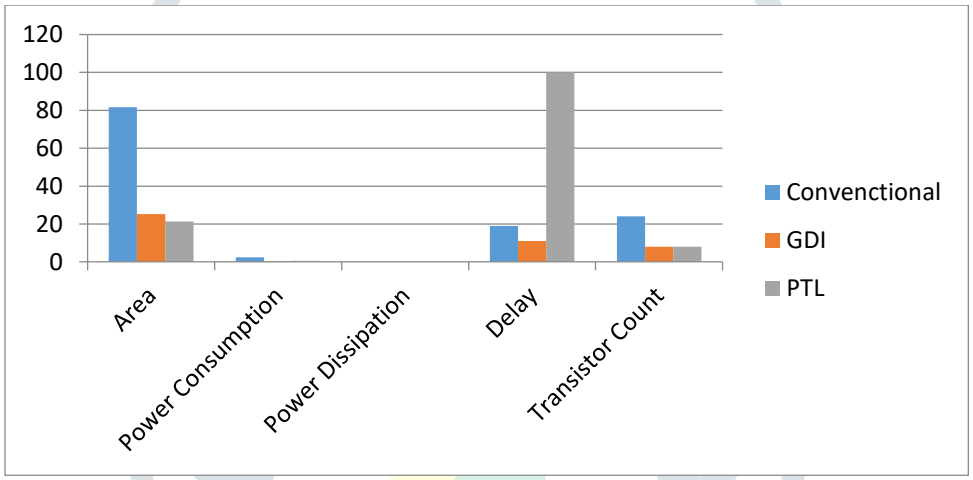

Fig.12 Comparison of Area, Power, No. of MOS transistors, Delay for different Logic Design Techniques

VII. CONCLUSION

After carrying out simulation of 1-bit comparator using three distinct Logic Techniques at 45nm fabrication technology, it is found that the power consumption, delay, power dissipation and number of MOS transistors have reduced to a great extent in case of GDI-based Logic. The reduction in above referred parametric values results in the improvement of performance of comparator circuit. Hence, GDI Logic has proved to be better designing technique as compared to the Conventional MOS Logic and PTL.

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