

# Comparative Study on Performance of various Adders used in Vedic Multiplier

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**Abstract:** Floating point multiplier plays a very important role in all DSP application can perform computations. In IEEE 754 standard describe the floating point number in single precision method and double precision method. The single precision floating number has the 3 parts, sign parts, exponent part and mantissa part. This mantissa part to perform the 24 bit multiplication, it can done by Vedic algorithm. In this Vedic algorithm adders are essential. With the advances in the VLSI technology, researchers have working on reducing the delay, area and power consumption. In this paper, the design 9bit, 18bit and 36bit of various adders like Carry Look Ahead adder (CLA), Carry Save Adder(CSA), Ripple Carry Adder(RCA), and Kogge Stone Adder (KSA). Further, the performance analysis was done in terms of area and delay. All adders are coded by using Verilog HDL and simulated with Xilinx ISE tool.

**KEYWORDS:** Ripple Carry Adder(RCA), Carry Save Adder(CSA), Carry Look-ahead Adder(CLA), Kogge Stone Adder(KSA).

## I. INTRODUCTION:

In all arithmetic function, addition plays a vital role. Adders are used in various application in modern VLSI system like DSP algorithms like IIR, FIR filter design [1]. Adders are critical hardware unit for efficient implementation of arithmetic unit. Addition operation also used in complements operations, encoding, decoding etc. Addition operations involved two numbers which are added and carry is produced. Hence addition operation results in sum value and carry value [2]. The carry which is generated during addition operation

from each adder is given to the next adder and so on. Therefore the carry is propagated in series computation. Hence delay is more as the number of bits increases [3].

In this paper various adders like Ripple Carry Adder, Carry Save Adder, Carry Look-ahead Adder and Kogge Stone Adder are designed using Verilog Code. The parameters like delay, LUT and slices are compared.

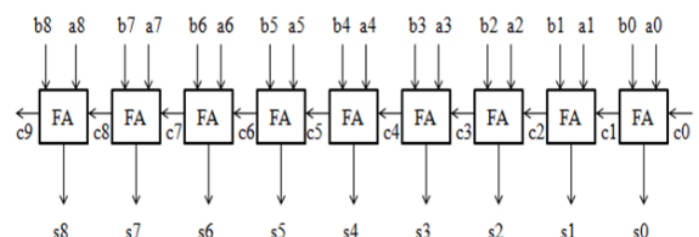
## II. ADDERS ARCHITECTURE

### 1. Ripple Carry Adder(RCA)

Multiple full adder circuits can be cascaded in parallel to add an N-bit number. A RCA is a logic circuit in which the carry-out of each full adder is the carry in of the succeeding next most significant full adder. It is called a RCA because each carry bit gets rippled into the next stage. In a ripple carry adder the sum and carry out bits of any half adder stage is not valid until the carry in of that stage occurs. Propagation delays inside the logic circuitry are the reason behind this.

Propagation delay is time elapsed between the application of an input and occurrence of the corresponding output. Each full adder inputs a  $C_{in}$ , which is the  $C_{out}$  of the previous adder.

The layout of ripple carry adder is simple, which allows for fast design time; however, the ripple carry adder is relatively slow, since each full adder must wait for the carry bit to be calculated from the previous full adder.



**Figure 1 Ripple Carry Adder**

## 2. CARRY SAVE ADDER(CSA)

Carry Save Adder(CSA) commonly are employed in high speed multipliers, where they generally are able to function more rapidly than “carry propagate” or “ripple carry” adders because a carry save adder doesnot completely perform the relatively time consuming carriers with sum bits between successive addition in the multiplication process but instead defers this task until the final cycle of the multiplying operation.

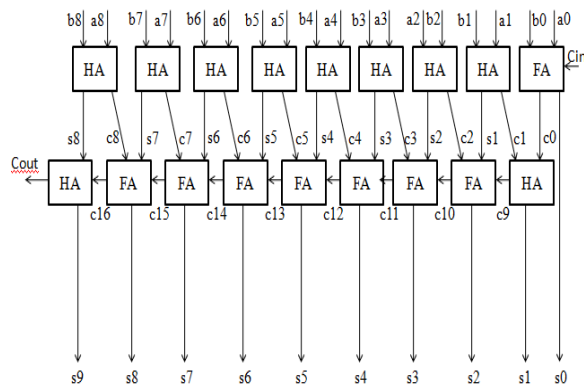
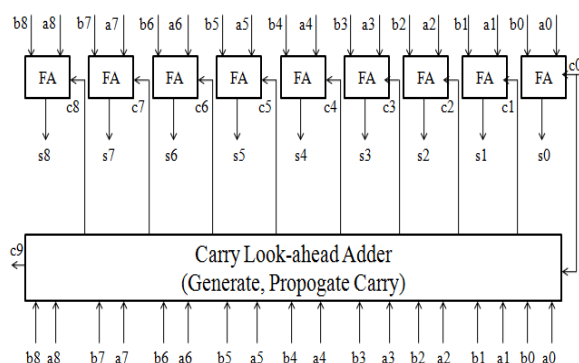


Figure 2 Carry Save Adder

## 3. CARRY LOOKAHEAD ADDER

A Carry Look-Ahead Adder (CLA) or fast adder is a type of adder used in digital logic. A carry look-ahead adder improves speed by reducing the amount of time required to determine carry bits. It can be contrasted with the simpler, but usually slower, ripple carry adder (RCA), for which the carry bit is calculated alongside the sum bit, and each stage must wait until the previous carry bit has been calculated to begin calculating its own sum bit and carry bit. The carry look-ahead adder calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger-value bits of the



adder.

Figure 3 Carry Look-ahead Adder

## 4. KOGGE STONE ADDER(KSA)

Kogge Stone adder(KSA) is the parallel prefix Adder and broadly considered as one of the fastest addition method. Carry generation is much faster because of parallel computation. The KSA comprises of three stages like Pre-processing Stage, Carry generation Stage and Post-Processing Stage. In the pre-processing stage propagation and generation signals are generated. Carry Generation Stage includes several cells which used to generate carry for the next stages and finally Post-processing Stage is used to generate Sum and carry out bit. From the pre-processing stage we get  $P(a,b)$  and  $G(a,b)$  signals.

$$\square \quad G = a_i \& b_i ; P = a_i \wedge b_i$$

$$\bigcirc \quad (P_i \& G_{i-1}) ; P = P_i \& P_{i-1}$$



Sum and Carry out bit is generated in the Post-Processing Stage.

$$\nabla \quad S_i = P_i \wedge C_{i-1}$$

Koggestone adder is one well known faster addition technique and also has a lower fan-out at the output which increases its performance but on the other hand, it occupies much area and creates wiring congestion problem.

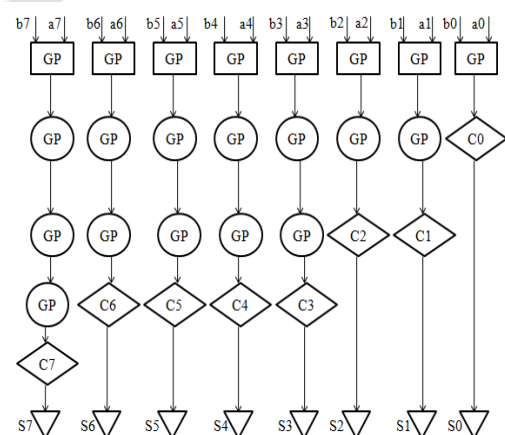


Figure 4Kogge Stone Adder

### III. COMPARISION OF RESULTS:

#### 1. OVERALL ANALYSIS OF ADDERS

The above mentioned adders are implemented in Verilog HDL. From the simulation results above, the adders with 9-bit, 18-bit and 36-bit are analysed based on the parameters given in the tables below.

**Table 1 Various bit adders delay in ns**

Delay in Ns	9 bit	18 bit	36 bit
KSA	8.427	12.837	15.18
RCA	9.335	14.092	22.712
CSA	9.939	16.183	37.322
CLA	8.861	13.224	23.924

**Table 2 Various bit adders LUT's in Nos**

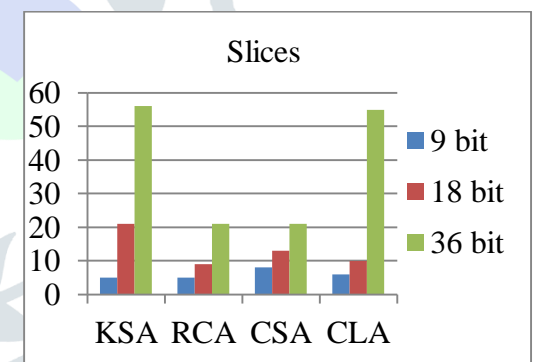
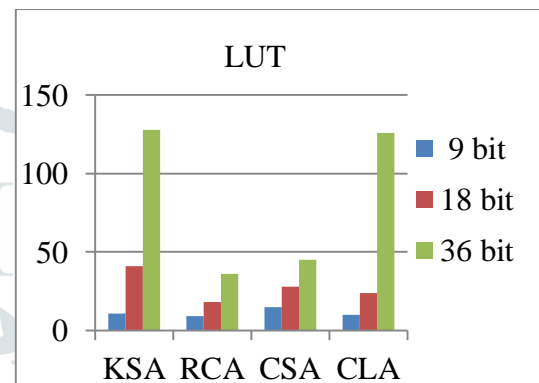
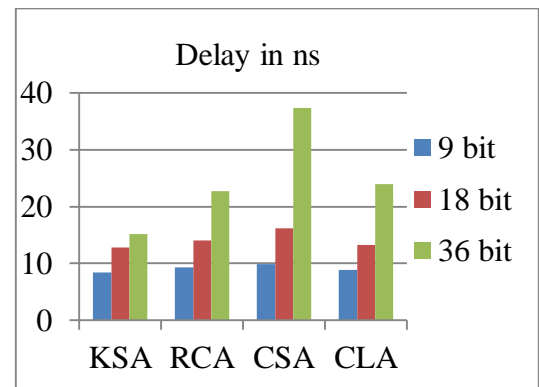
LUT	9 bit	18 bit	36 bit
KSA	11	41	128
RCA	9	18	36
CSA	15	28	45
CLA	10	24	126

**Table 3 Various bit adders number of occupied Slices in Nos**

SLICES	9 bit	18 bit	36 bit
KSA	5	21	56
RCA	5	9	21
CSA	8	13	21
CLA	6	10	55

#### IV. CONCLUSIONS

In this paper, we have compared various adders such as Ripple Carry Adder(RCA), Carry Save Adder(CSA), Carry Look-ahead Adder(CLA and Kogge Stone Adder(KSA). The Kogge Stone Adder results in reduced delay when compared with the other adders.



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