Power Efficient and Performance Comparisons of Diverse CMOS Structure of 2:1 MUX using DG FINFET Technique

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Abstract: In this paper, we suggest 2:1 MUX architecture with low power high speed with the following logics: Static CMOS logic, Pseudo NMOS logic, CMOS Domino logic, and also Dual Rail Domino logic using DG FINFET (Double Gate Fin Shaped Field Effect Transistor) Technique. The portability was upgraded in gadgets with taller balances because of increment tensile stress. The urgent barriers to scaling of mass CMOS gate lengths comprise short channel impacts, ideal current, entryway dielectric spillage, and devices for the different devices. However, the DG FINFET outline provides improved power over short channel impacts, low spillages & improved yields. Results demonstrate that CMOS Domino Logic 2:1 MUX with the DG FINFET is the most efficient architecture in comparison with other family logic circuits since average power consumption is less than that of Power Delay Product (PDP) and other logic families. However, trade-offs b/w static CMOS logic & domino logic are concluded that can be ignored when taking into consideration total performance. Because DG FINFET Domino logic is above another logic family, this study shows that DG Domino logic allows any of higher MUX including low-power delay with PDP levels. The designed circuits are realized in a standard 90nm process technology and use 0.7V supply voltage. Our optimization circuitry using the proposed method reduces power consumption and leakage current by a significant amount of multiplexer circuit.

Key Words: **MUX, Pseudo NMOS logic, Static CMOS logic, CMOS Dual-Rail Domino logic, and CMOS Domino logic Low Power, Cadence, Leakage Current, Delay.**

1. INTRODUCTION

In various industrial applications that include the introduction of low-powered & area-efficient devices [1, 2], batteries & portable devices are of great demand. In 1965, Gordon Moore noticed Moore's law. He was INTEL Corporation's co-founder. He set speed for the new digital uprising also used to increase power and reduce costs in the computing world. He estimated that every two years there will quadruple the number of transistors on the integrated circuit. This prediction is referred to as the law of Moore. Many industrial applications are now planned for the range of nanometers. The scale of the transistors is limited to phenomena such as short-channel effects, including hot carrier effects & tunneling using oxide thickness. CPU is an integral part of the arithmetical logic unit (ALU). The adder cell is a major ALU unit. A significant number of digital circuit adders have been used to add numbers [3, 4]. Adders are used for computing addresses [5], table indices, and related operations in each of the processors in other parts of the processor. The need for mobile devices like mobile phones, tablets, laptops [6, 7] has increased and the need for VLSI circuits which are area effective and strong has emerged. In lower power applications, low power adder cells are used. There are n select lines in a 2n input multiplexer to determine the input line to give to o/p [8]. 2:1 "switch logic" [9] is a basic block. There are 2 input lines (A) & (B), 1 line "S" & other output "Y" as seen in fig. 1 [10]. The truth table of 2:1 MUX has represented in the Table and the logic function is

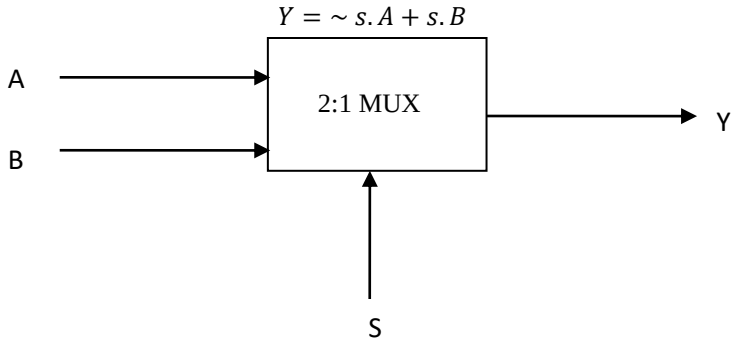

Fig. 1. Symbol Diagram of a 2:1 MUX

Table I. 2:1 MUX truth table

Select Line	I/P		O/P
~s/s	A	B	Y
1/0	X	0	0
1/0	X	1	1
0/1	0	X	0
0/1	1	X	1

2. PROPOSED 2:1 MUX

In this paper, 2:1 multiplexer has been considered via various logics like Static CMOS, Pseudo NMOS, CMOS Domino & CMOS Dual Rail Domino logic has been simulated at 90nm technology shown in below figures. Sizing of a transistor for 2:1 MUX designed and estimated results and comparison are shown is below Tables.

A. Static CMOS logic

Static CMOS logic is designed consists of select pins S, SBAR, two inputs A and B, and output pin VOUT. A PUN composed of four pMOS and PDN containing four nMOS has been created for the static CMOS based on 2:1 MUX. The PUN is designed with two series-connected parallel pMOS circuits. The PDN is designed with a parallel communication of 2 series nMOS circuits. To achieve the correct output, Static CMOS logic output is connected to the inverter. Vdc at 0.7V would be attached to the power supply pull-up circuit and the ground is attached to the pull-down circuit. Vpulse is used to provide input to the circuit that is set to the 2:1 MUX truth table. CMOS schematic has illustrated in Figure 3 also its transient response has illustrated in Figure 4.

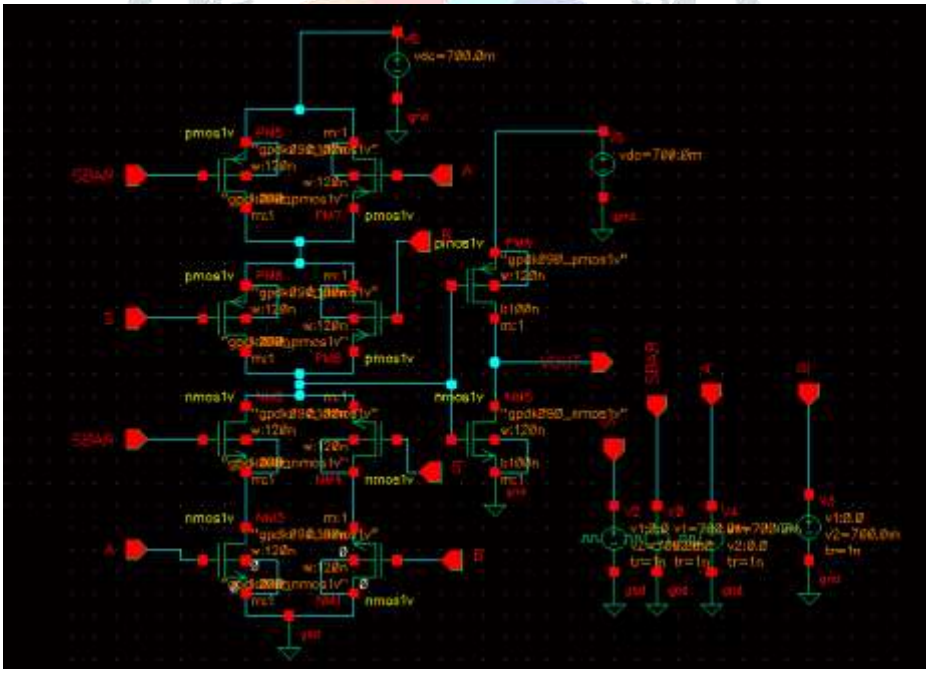

Fig. 2.Schematic of Static CMOS logic

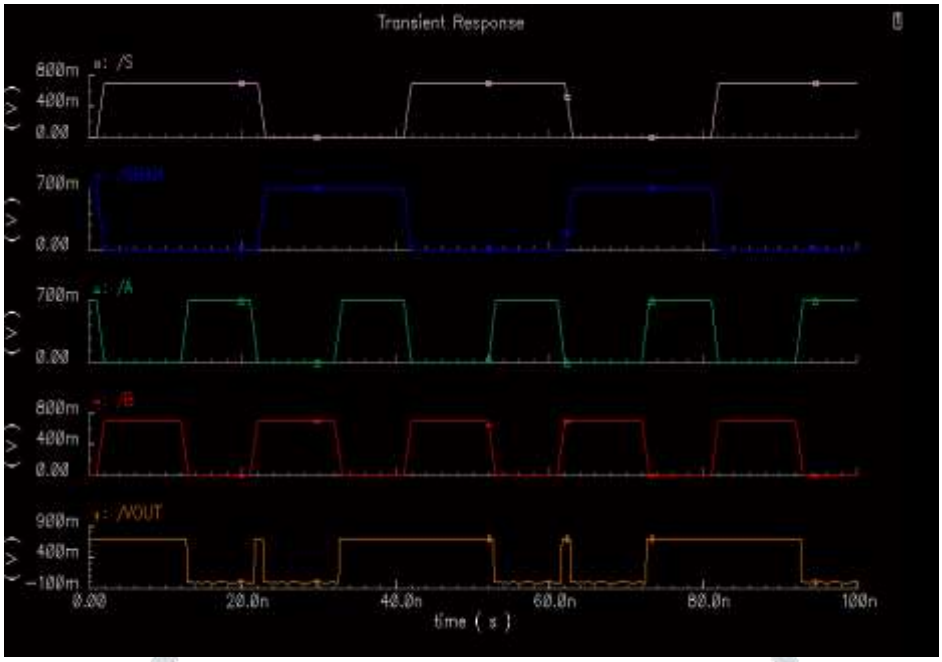

Fig. 3.Transient Response of Static CMOS logic

B. Static CMOS logic using DG FINFET

Double Gate devices are used in numerous inventive forms in circuit designs of analog & digital. Two transistors and their source and drain terminals are connected to form a Parallel transistor pair. 2nd gate is compared to the standard gate in Double-Gate (DG) FINFETS, predictable both for superior control effects on short channels and for controlling the leakage current. Here, DG FINFET self-determined front and back control can be used effectively to develop performance & minimize power consumption. Fig.5 indicated the scheme of static CMOS logic using DG FINFET, and Fig.6 indicated the output waveform, with its leakage current waveform indicated in Fig.7.

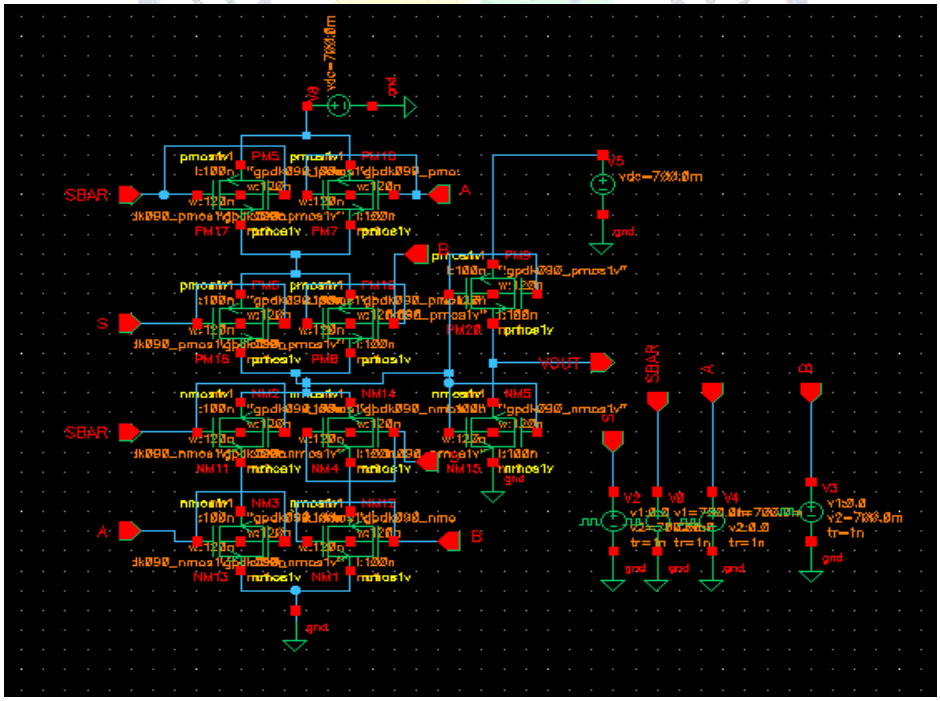

Fig. 4.Schmetic of Static CMOS logic using DG FINFET

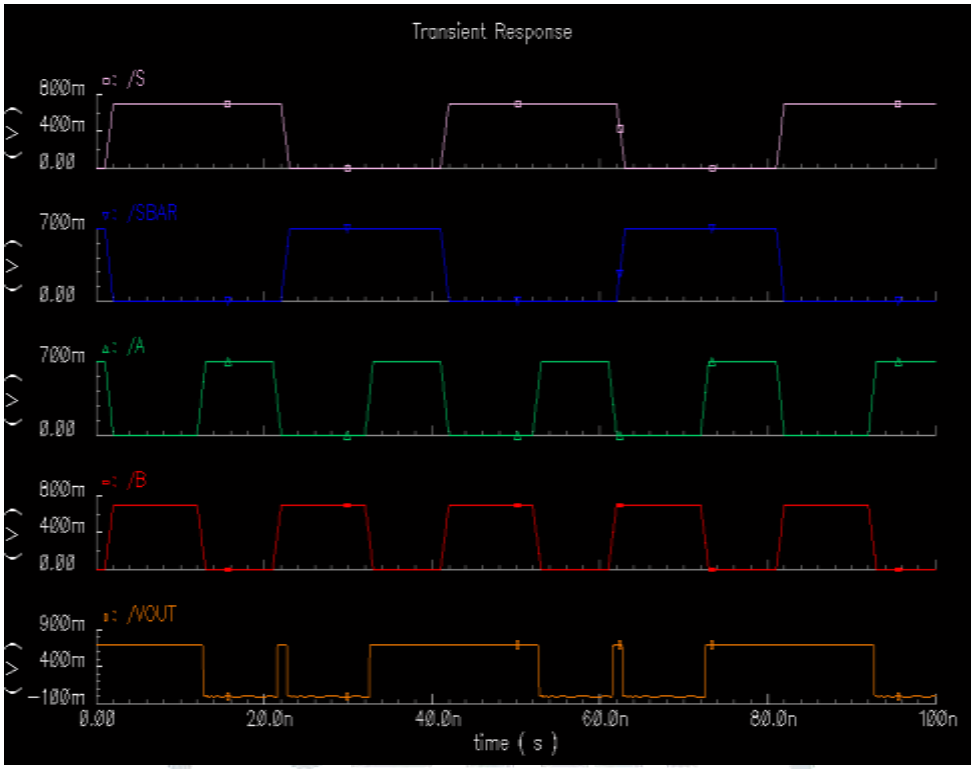

Fig. 5. Output Waveform of Static CMOS logic using DG FINFET

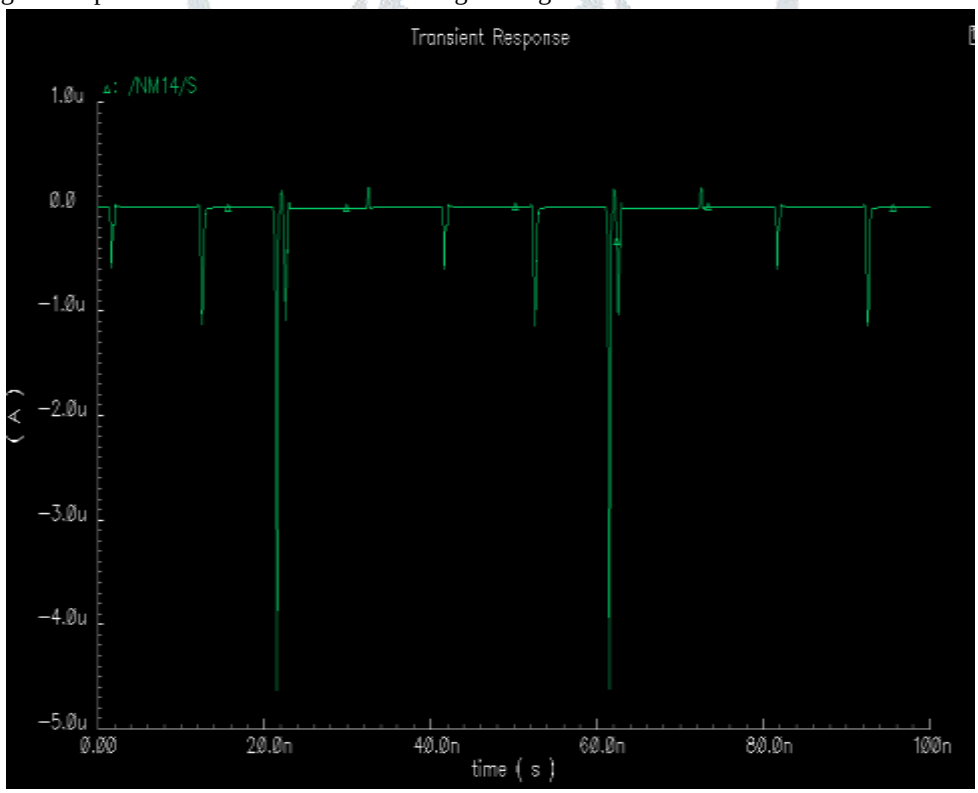

Fig. 6. Leakage Current Waveform of Static CMOS logic using DG FINFET

C. Pseudo NMOS Logic

PDN is like a standard static gate in pseudo NMOS logic, but the PUN still has a pMOS transistor on it. To compromise between the spectrum of noise and the speed, the pMOS transistor diameter is chosen to be around 1/4 strength of NMOS PDN; the optimum size is procedural [11]. This reduces the area necessary for implementing logics that increases the speed in return.

Pseudo-NMOS logic consists of S, SBAR, two A and B inputs, and the output pin VOUT. 2:1 MUX architecture with Pseudo NMOS logic is very close to that of Static CMOS, except a single pMOS transistor for complete PUN & is enduringly grounds to

minimize transistors counts. In Fig. 8 transient response and Fig. shown the Pseudo NMOS output is attached to the inverter to get the proper Pseudo NMOS Logic schematics output. Power supply via Vdc is provided at 0.7 V and the circuit inputs are supplied with Vpulse as provided in the 2:1 MUX truth table. The simulated Result Summary is shown in Table2.

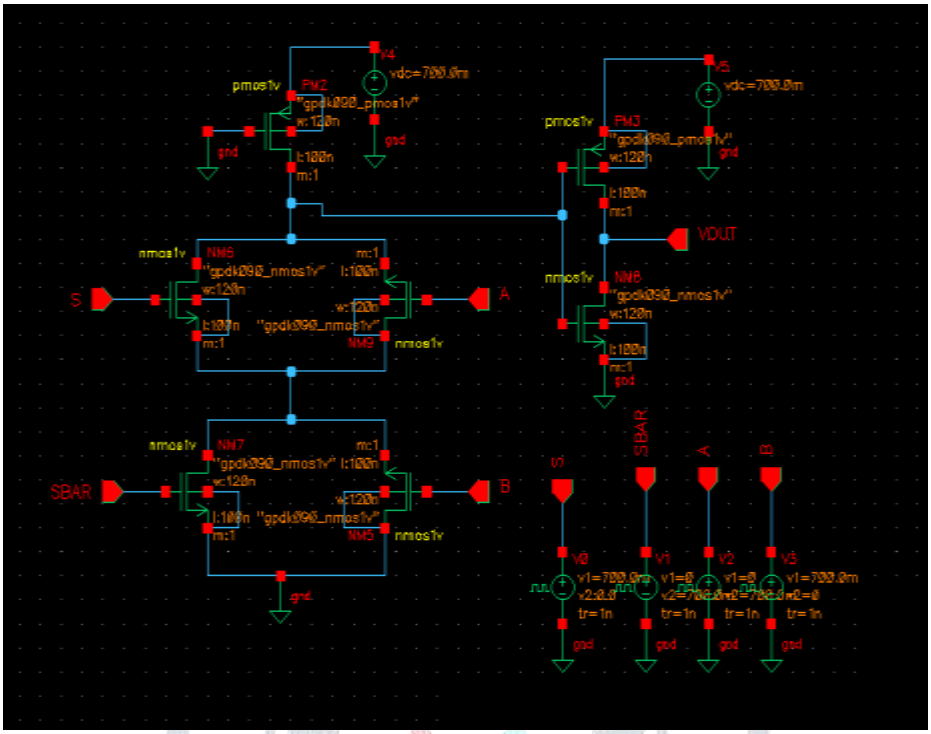

Fig. 7. Schematic of Pseudo NMOS Logic

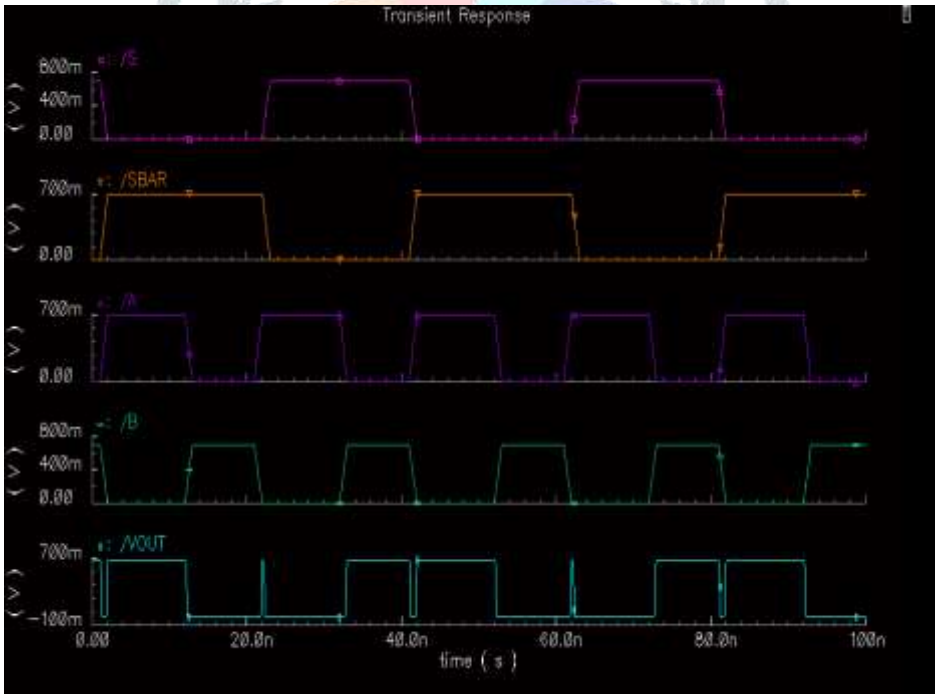

Fig. 8.Transient Response of Pseudo NMOS Logic

D. Pseudo NMOS Logic using DG FINFET

2 transistors also their source & drain terminals are connected to form a Parallel transistor pair. The second gate is included in contrast with the conventional gate DG FINFETS, predictable to control short channel effects to superior control and to control the current leakage. Here, DG FINFET self-determined front and back control can be used effectively to develop efficiency and reduce power consumption. The schematic for pseudo-NMOS logic using DG FINFET is indicated in figure 5 and the Output waveform is indicated in Figure 11 and its Leakage Current Waveform indicated in Figure 12.

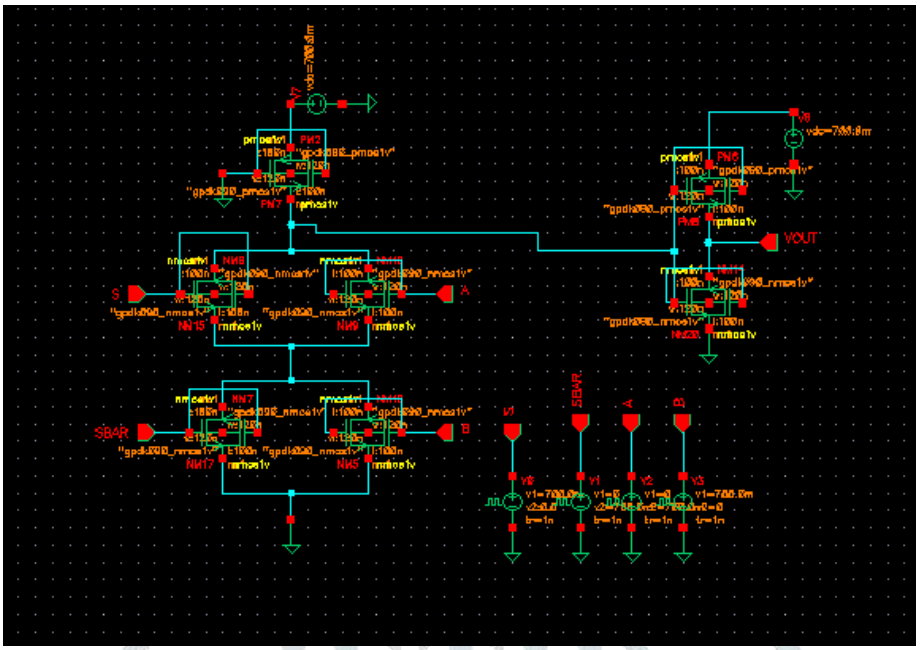

Fig. 9. Schematic of Pseudo NMOS Logic using DG FINFET

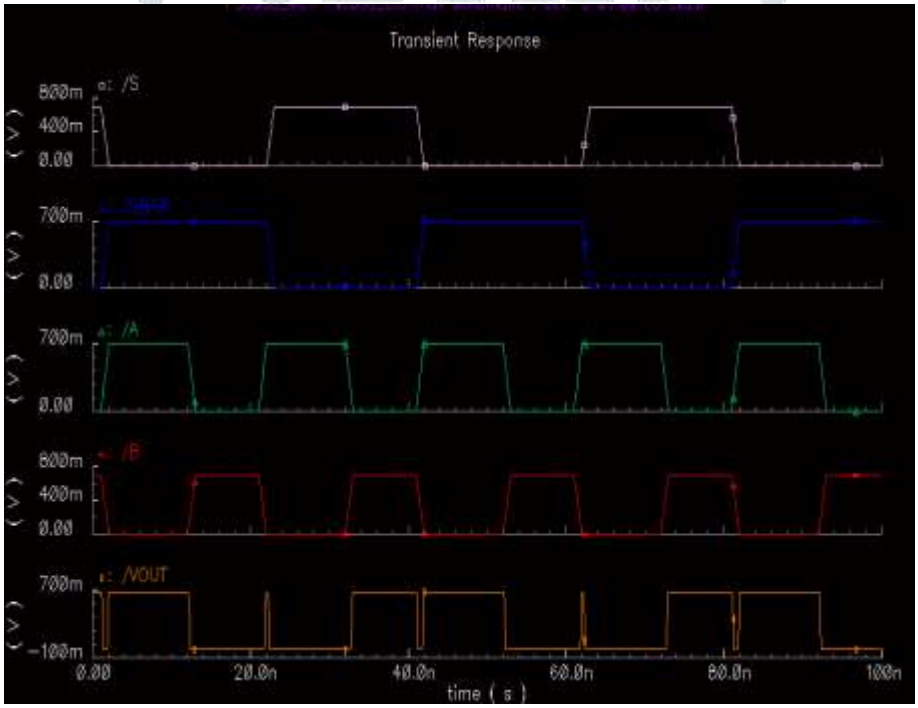

Fig. 10. Output Waveform of Pseudo NMOS Logic using DG FINFET

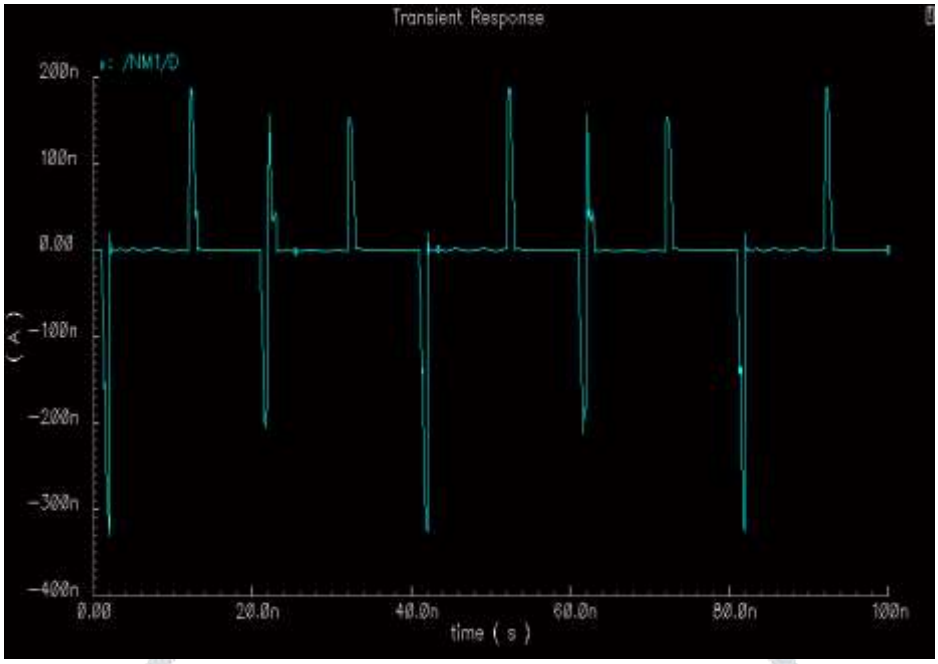

Fig. 11. Leakage Current Waveform of Pseudo NMOS Logic using DG FINFET

E. CMOS Dual-Rail Domino

A complete logic family of CMOS Dual-Rail Dominos can only use inverting logic to measure any inverting or non-inverting function which is a restriction of this form of domino logic. However, more area, wire, and power are required.

Figure 13 shows that the 2:1 MUX is configured the complementary domino logic to bind with existing domino logic. Many other working principles continue to be the same as Domino logic. Dual-Rail Domino logic's transient response is indicated in Figure 14.

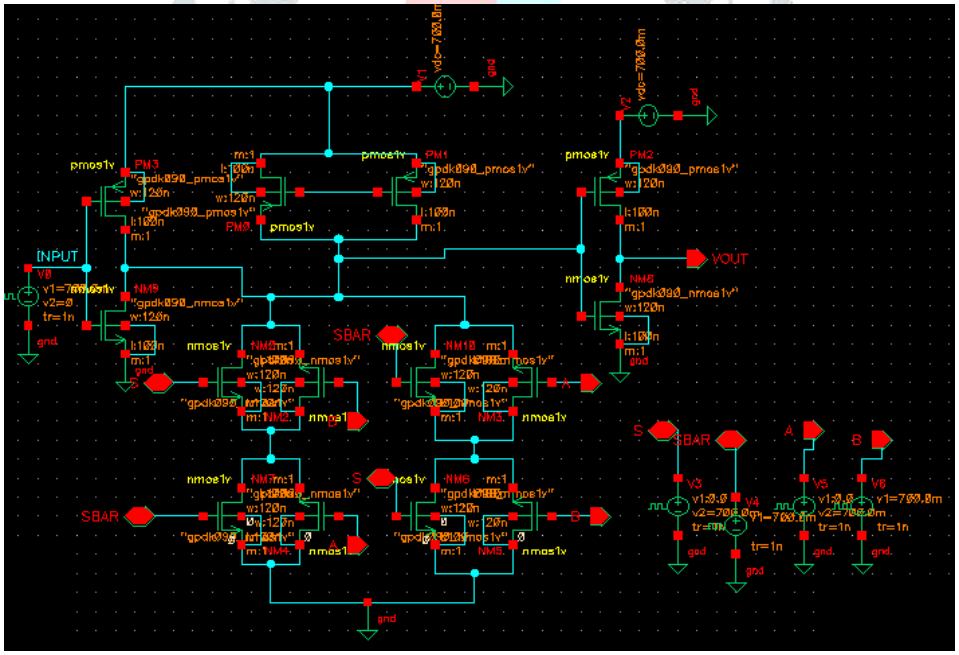

Fig. 12. Schematic of CMOS Dual-Rail Domino

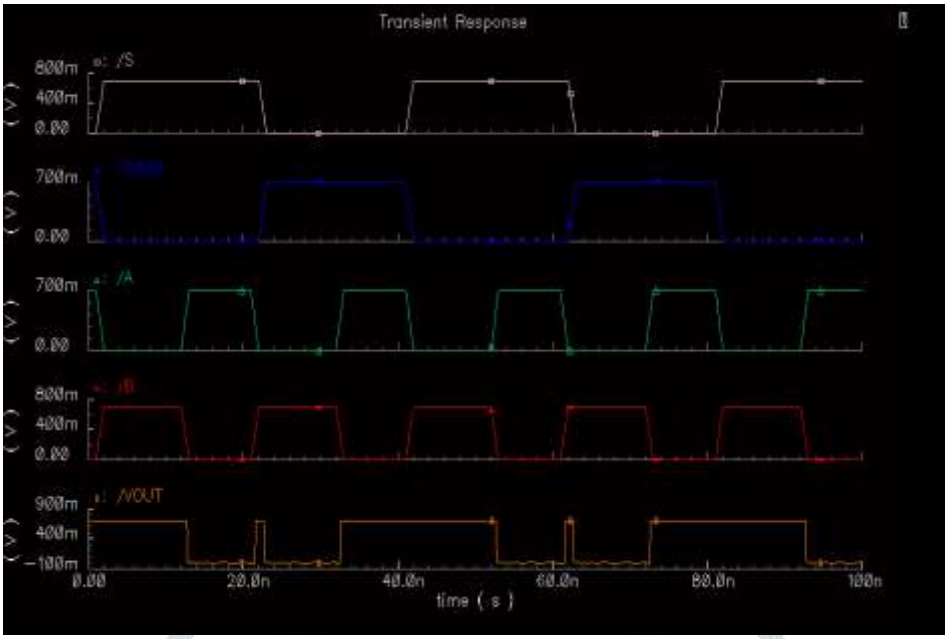

Fig. 13.Transient Response of CMOS Dual-Rail Domino

F. CMOS Dual-Rail Domino using DG FINFET

Two transistors and their source & drain terminals are connected to form a Parallel transistor pair. The second gate is introduced in comparison with the traditional DG FINFETS gate, predictable to manage short channel effects to superior control and to control leakage current. DG FINFET can be efficiently utilized with the self-determination of front & back gate control to develop performance and minimize power consumption. The schematic of CMOS Dual-Rail Domino using DG FINFET is demonstrated in Figure 15 and the Output waveform is demonstrated in Figure 16 also it's Leakage Current Waveform shown in Figure 17.

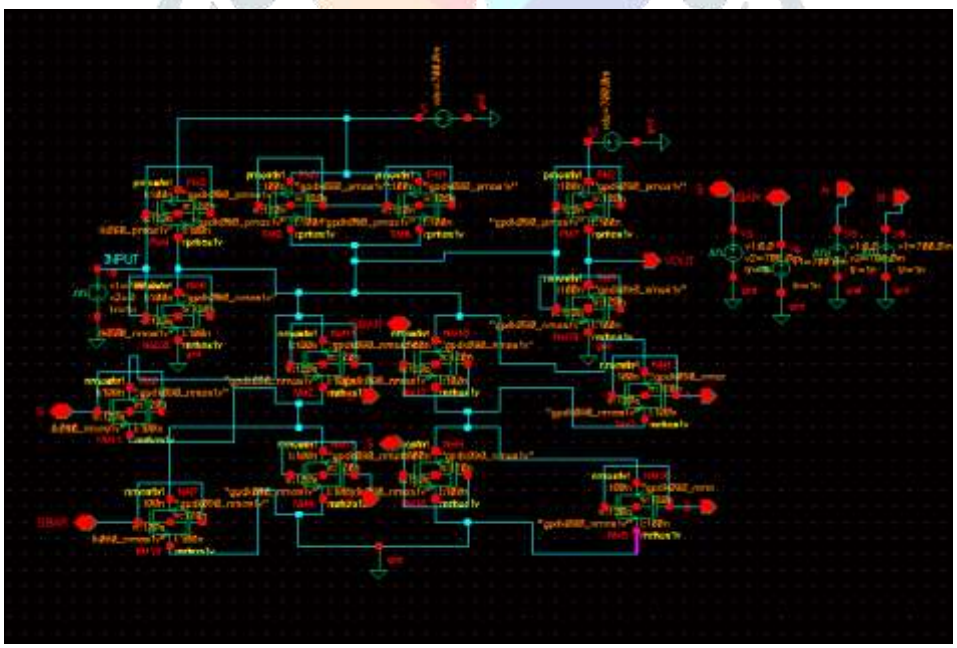

Fig. 14. Schematic of CMOS Dual-Rail Domino using DG FINFET

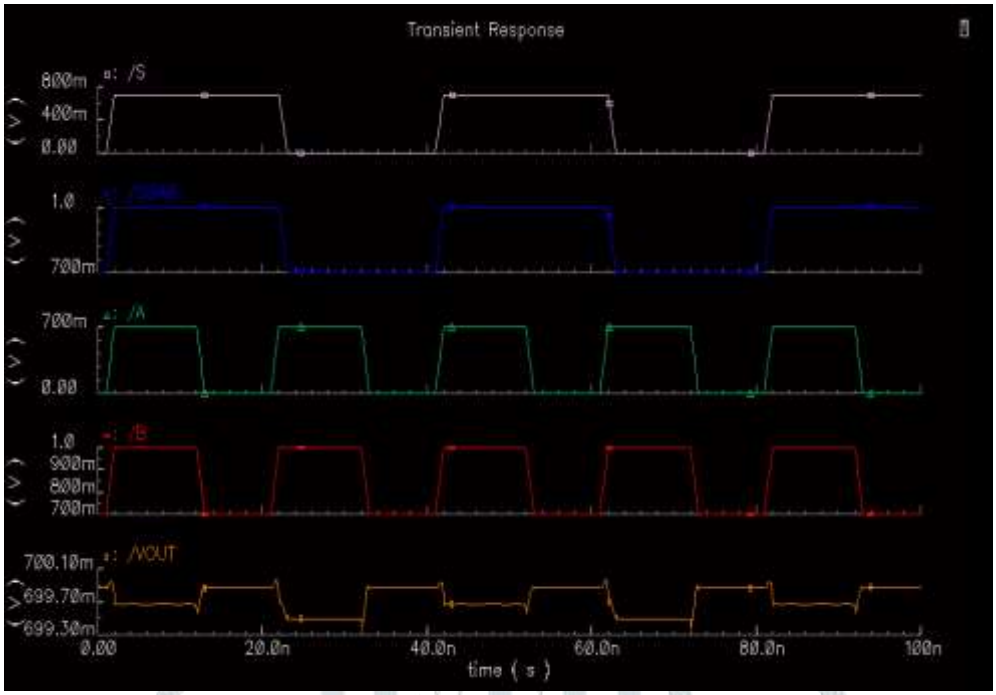

Fig.15. Output Waveform of CMOS Dual-Rail Domino using DG FINFET

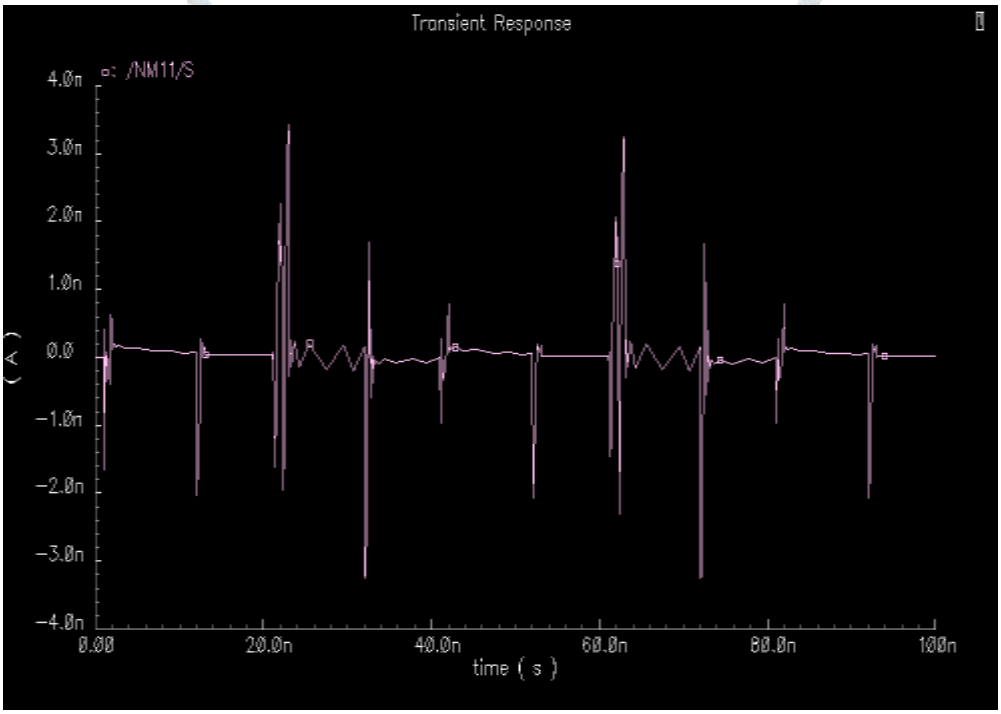

Fig.16. Leakage Current Waveform of CMOS Dual-Rail Domino using DG FINFET

G. CMOS Domino Logic

To address the Dynamic Logic Circuits monotonicity problem, Domino Logic was added. As shown in Fig18, a static CMOS inverter between dynamic gates is necessary for the resolving of the monotonicity problem.

The 2:1 MUX construction is similar to Pseudo NMOS Logic using Domino logic. The only distinction is that grounded PUN has the high clock skew that Vpulse gives. To resolve the problem of monotonicity and increase circuit efficiency, this output is connected to a CMOS inverter as shown in fig.18. VDD is used for supplying energy to the connected circuit with the power supply and the other inputs supplied by Vpulse; Transient response of Domino logic is demonstrated in Figure 19

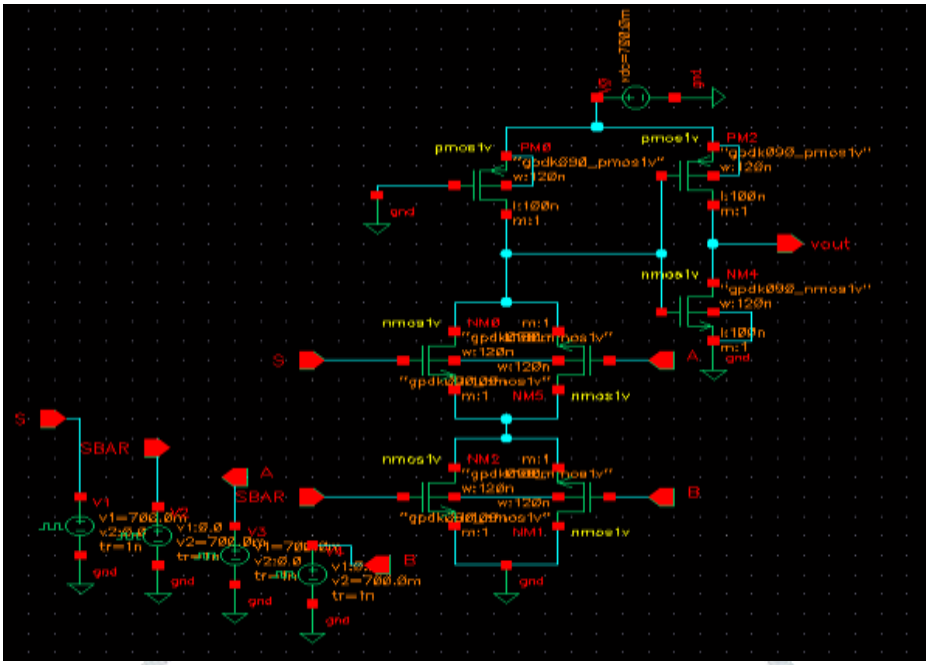

Fig. 17. Schematic of CMOS Domino Logic

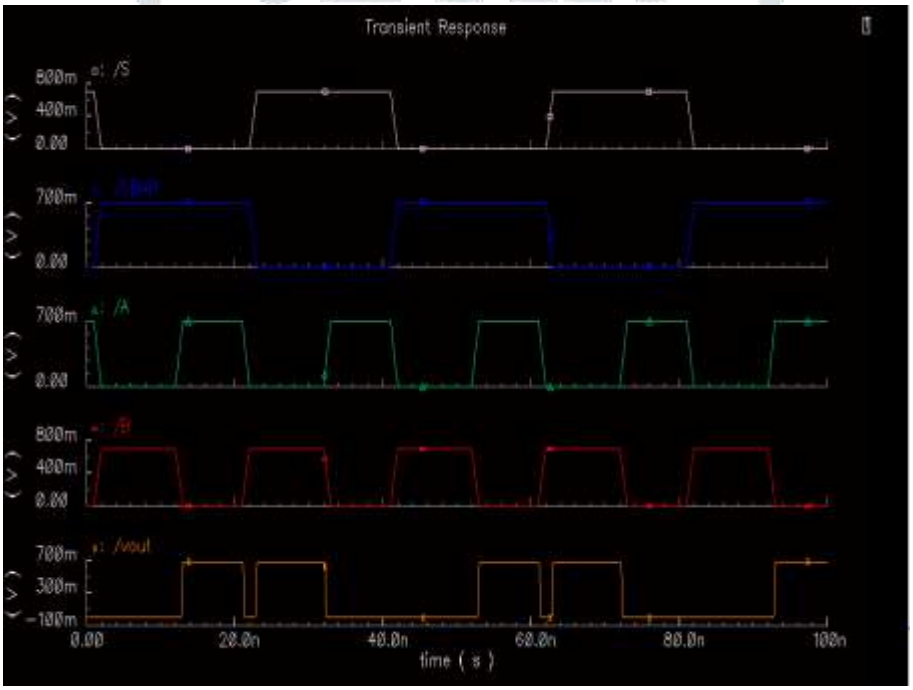

Figure 18.Transient Response of CMOS Domino Logic

H. CMOS Domino Logic using DG FINFET

2 transistors also their source & drain terminals are connected to form a Parallel transistor pair. The second gate is introduced in contrast with the conventional gate in DG FINFETS, predictable to control short channel effects to superior control and to control the current leakage. DG FINFET can here be used for efficient self-determination of the front and back gate to achieve performance and reduce power consumption. The schematic of CMOS Domino Logic using DG FINFET is demonstrated in Figure 20 & Output waveform is demonstrated in Figure 21 and its Leakage Current Waveform demonstrated in Figure 22.

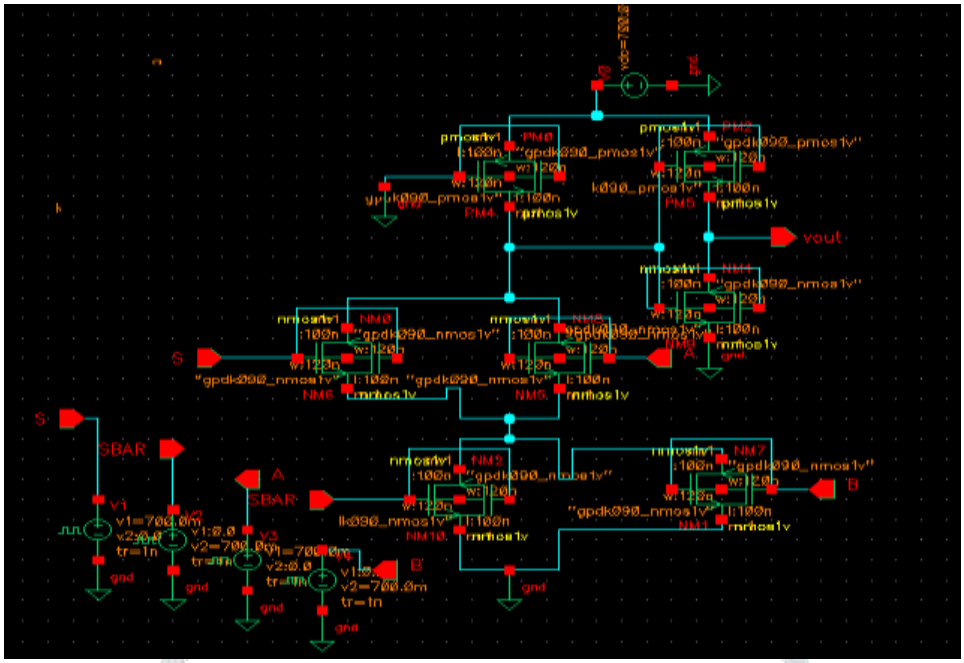

Fig. 19. Schematic of CMOS Domino Logic using DG FINFET

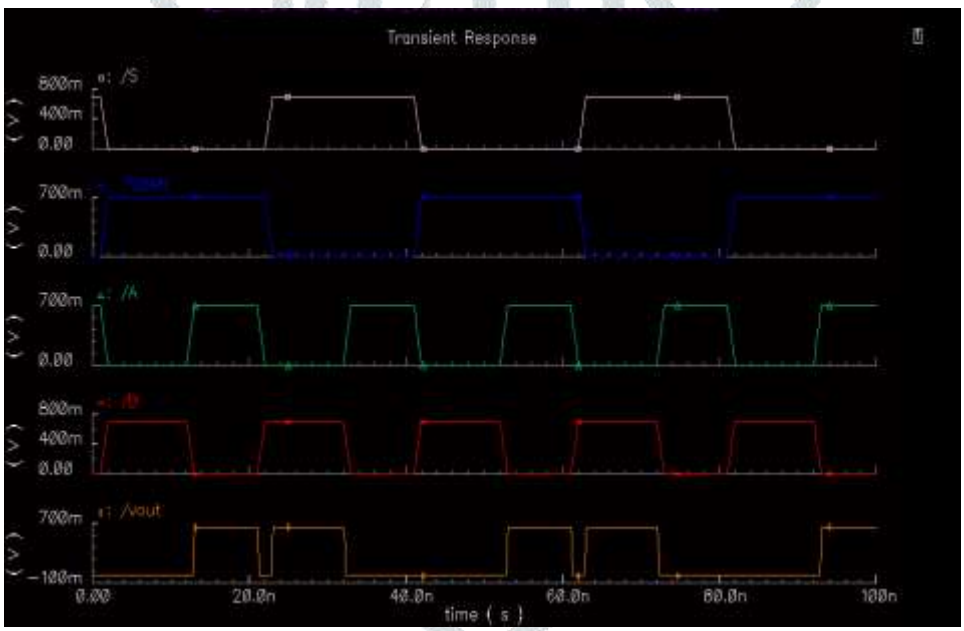

Fig. 20. Output Waveform of CMOS Domino Logic using DG FINFET

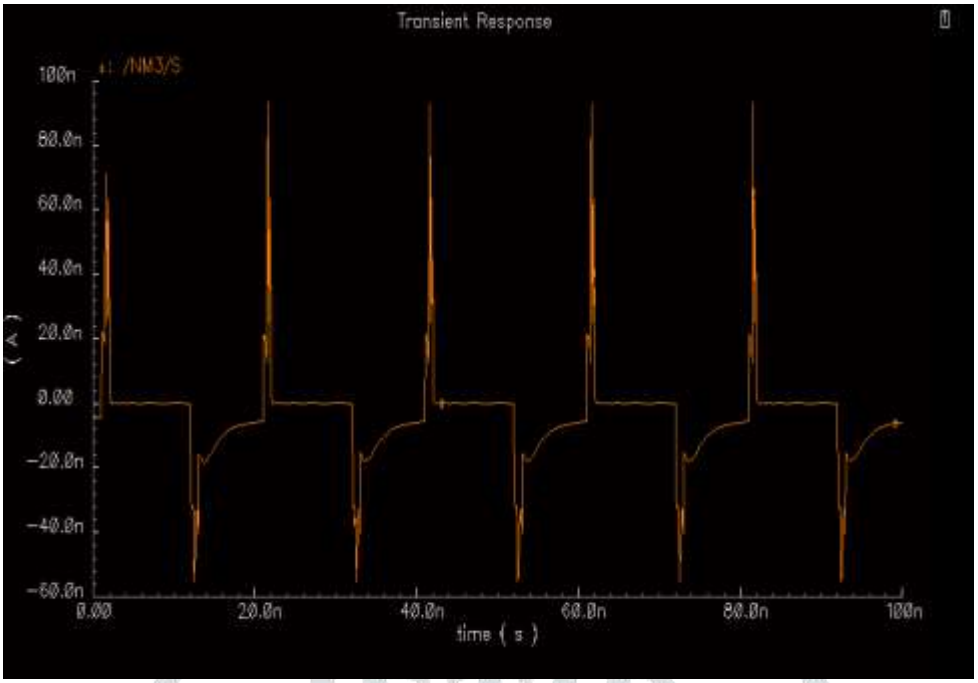

Fig. 21. Leakage Current Waveform of CMOS Domino Logic using DG FINFET

3. SIMULATION RESULT

A low power high speed 2:1 MUX design by the use of various logics like Pseudo NMOS, Static CMOS, CMOS Dual Rail Domino, and CMOS Domino logic using DG FINFET Simulation has been completed on cadence tool using 90nm technology with nominal supply voltage Vdd = 0.7 V. Gate leakage being only main method at room temperature 27°C, several logics have utilized for diminution of power consumption & maintaining the performance of 2:1 MUX, it comparative analysis parameter like Average Current, leakage power, Propagation Delay, Power product delay (PDP).

Comparison between Static CMOS, Pseudo NMOS, CMOS Domino & CMOS Dual Rail Domino logic, and applied technique is shown below table II and table III.

Table II. Comparison of Result Summary

Performance Parameter	Pseudo NMOS Logic	Static CMOS Logic	CMOS Domino logic	CMOS Dual-Rail Domino logic
Leakage Power	9.08nW	12.30nW	9.01nW	16.11Nw
Leakage Current	11.2nA	16.45nA	10.1nA	18.02nA
Average Power	22.02 µW	28.22µW	24.23 µW	45.12 µW
Propagation Delay	2.12ns	2.23ns	2.02ns	2.43ns
Power Delay Product (PDP)J	0.46		0.48	
Number of Transistor	7		7	

Table III. Comparison of Result Summary

Performance Parameter	Static CMOS Logic using DG FINFET	Pseudo NMOS Logic using DG FINFET	CMOS Dual-Rail Domino logic using DG FINFET	CMOS Domino logic using DG FINFET
Leakage Power	10.03nW	8.1nW	12.10nW	7.9nW
Leakage Current	12.04nA	9.02nA	14.21nA	8.02nA
Average Power	24.26µW	20.22 µW	38.23 µW	21.01 µW
Propagation Delay	2.02ns	1.12ns	1.34ns	1.09ns
Power Delay Product (PDP)J	0.48	0.20	0.49	0.22
Number of Transistor	12	7	14	7

4. CONCLUSION

This paper proposes low power high speed 2:1 MUX design by the use of various logics like Pseudo NMOS, Static CMOS, CMOS Dual-Rail Domino, and CMOS Domino logic; using DG FINFET (Double Gate Fin Shaped Field Effect Transistor) Technique. The findings show that 2:1 MUX CMOS Domino logic using DG FINFET has the most efficient concept, as average energy consumption is lower than other logic families and the delay is lower than that of other logic families. Since DG FINFET Domino Logic outperforms other logic families, this study shows, DG FINFET Domino Logic allows for higher MUXs with a low power delay and PDP levels. The designed circuits are realized in a standard 90nm process technology and use 0.7V supply voltage. Our optimization circuitry using the proposed method reduces power consumption and leakage current by a significant amount of multiplexer circuit. The importance of a Multiplexer is that it is possible to reduce large parallel buses into serial signals for telecommunication, data communication, satellite, and military applications by using serial converters (the most relevant MUX-application).

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