INVESTIGATIONS ON CASCADED MULTI LEVEL INVERTER SYSTEM

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Abstract: This paper deals with modeling, simulation and implementation of five level cascaded inverter system. A five level inverter fed induction motor drive system is modeled and the results are presented. The prototype of the system is also presented to compare the simulation results with experimental results. There is close agreement between simulation results and experimental results.

Keywords: Induction motor, Multi level inverter, Cascaded inverter, Total harmonic distortion, Matlab Simulink.

I. GENERAL

Multilevel inverter [MLI] topology is a most promising inverter topology for medium voltage and high power applications. This inverter synthesizes several different levels of DC voltages to produce a stepped AC output that approaches the pure sine waveform [9]. It has the advantages like high power quality waveform, lower voltage ratings devices, lower harmonic distortion, lower switching frequency losses, higher efficiency, reduced dv/dt stresses etc.

II. CASCADED MULTILEVEL INVERTER

Cascaded multilevel inverter is based on the series connection of inverter with separate DC sources. Cascaded multilevel inverters eliminates the excessively large number of bulky transformers required by conventional multilevel inverters, the clamping diodes required by diode clamped multilevel inverters and the bulky capacitors required by flying capacitor multilevel inverters. Therefore cascaded multilevel inverters (CMLI) appear to be superior to other multilevel structures. The cascaded multilevel structure uses two H-bridge inverters: A main bridge and an auxiliary bridge. The load is connected in such a way that the sum of the outputs of these bridges will appear across it. The ratio of power supply between auxiliary bridge and main bridge of 1:1, 1:2 and 1:3 are used to produce, five level, seven level and nine level voltage across the output terminals.

III. OPERATION OF CASCADED FIVE LEVEL INVERTER

Five level inverter fed induction motor drive system uses a Symmetrical Cascaded Multilevel Inverter (SCMLI) consisting of two cascaded H-bridge inverters: a main bridge inverter and an auxiliary bridge inverter. The load is connected in such a way that the sum of the outputs of these inverter bridges will appear across the load. The ratio of power supplies between the auxiliary bridge and main bridge is 1:1.

The main bridge $H_1$ as well as auxiliary bridge $H_2$ consists of DC source of $V_{dc}$ each as shown in Figure 5.2. By proper opening and closing of switches, each H-bridge can generate three different voltage outputs $+V_{dc}$, $0$ and $-V_{dc}$. $H_1$ can generate these voltages by proper combination of four switches $S_1$, $S_2$, $S_3$ and $S_4$. When $S_1$ and $S_4$ are simultaneously on, the output of $H_1$ is $+V_{dc}$, when $S_2$ and $S_3$ are simultaneously on, the output of $H_1$ is $-V_{dc}$. Similarly the output of $H_2$ can be made equal $+V_{dc}$, $0$ and $-V_{dc}$ using $S_5$, $S_6$, $S_7$ and $S_8$. Simultaneous turning of switches $S_1$, $S_2$ or $S_3$, $S_4$ or $S_5$, $S_6$ or $S_7$, $S_8$ results in zero output voltage. The output voltage of $H_1$ is taken as $V_1$ and the output voltage of $H_2$ is taken as $V_2$. The output voltage of the inverter is synthesized by the sum of output voltages of main bridge and auxiliary bridge. i.e. the output voltage of $H_1$ and $H_2$ and is given as $V = V_1 + V_2$. Thus the five level inverter output voltage of $+2V_{dc}$, $+1V_{dc}$, $0$, $-V_{dc}$, $-2V_{dc}$ can be obtained. Table 5.1 shows the switching states of transistors, output voltage of...
H-bridges and output voltage of five level inverter. ‘0’, status means switch is in OFF state and ‘1’, status means switch is in ON state.

Table 1: Switching states of transistors of five level inverter.

<table>
<thead>
<tr>
<th>Voltage level</th>
<th>S1</th>
<th>S2</th>
<th>S3</th>
<th>S4</th>
<th>V1</th>
<th>S5</th>
<th>S6</th>
<th>S7</th>
<th>S8</th>
<th>V2</th>
<th>V =V1+V2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>-1Vdc</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>-1Vdc</td>
<td>-2Vdc</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>-1Vdc</td>
<td>-1Vdc</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
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<td>1</td>
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<td>0</td>
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</tr>
<tr>
<td>4</td>
<td>0</td>
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<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>+1Vdc</td>
<td>+1Vdc</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>+1Vdc</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>+1Vdc</td>
<td>+2Vdc</td>
</tr>
</tbody>
</table>

IV. SIMULATION RESULTS OF FIVE LEVEL INVERTER

The simulation is done using Matlab simulink and the results are presented. The DC input voltage of each bridge of a cascaded structure is shown in Figure 1. The output voltage is shown in Figure 2. It can be seen that the output has 5 levels. The output current is shown in Figure 3. Three phase structure of five level inverter is shown in Figure 4. The output voltage of the inverter is shown in Figure 5. Output current of the inverter is shown in Figure 6. The speed response of five level inverter fed induction motor drive is shown in Figure 7. The speed increases and settles at 1305 rpm. FFT analysis is done for the output current as well as output voltage and the corresponding spectrums are shown in Figure 8 and 9 respectively. The current THD is 7.09 percent and voltage THD is 8.40 percent.

Figure 1. DC Input voltage of five level inverter with induction motor load
Figure 2. Output voltage of five level inverter with induction motor load

Figure 3. Output current of five level inverter with induction motor load.

Figure 4. Three phase structure of cascaded five level inverter
Figure 5. Output voltage waveforms of 3-phase five level inverter

Figure 6. Output current waveforms of 3-phase five level inverter

Figure 7. Rotor speed of five level inverter fed drive system
Laboratory module for the hardware of five level inverter is fabricated, tested and the corresponding results are presented here. The hardware consists of micro controller module, pulse amplifier module and IGBT module. The switching pulses for MOSFETs M₁ and M₅ are shown in Figure 10. Output voltage of five level inverter fed induction motor drive is shown in Figure 11. The experimental value of current THD of five level inverter is 6.64 percent and voltage THD is 7.81 percent.

Figure 10. Switching pulses for M₁ & M₅ of five level inverter
VI. CONCLUSION

Five level cascaded inverter fed induction motor drive system with equal DC sources is modeled, simulated and implemented successfully. Simulation and experimental results for stator voltage, stator current, rotor speed and FFT spectrums of five level inverter system are presented. The hardware results of three phase five level inverter system are also presented. The experimental value of current THD is 6.64 percent. There is close agreement between simulation and experimental results. The efficiency of five level inverter fed induction motor drive system is 74.43 percent. The THD values of five level inverter system are less than that of three level inverter system and the efficiency as well as rotor speed of 5 level inverter fed induction motor drive system are more than that of 3 level inverter system. Therefore five level inverter is better than three level inverter system.

REFERENCES