Novel Circuit Designing of 2 to 4 Decoder using Quantum dot Cellular Automata

Ruchita Patil, Shweta Agrawal

[1]Research Scholar, Electronics and Communication Engineering Dept, SRCEM, Gwalior India,
[2]Professor, Electronics and Communication Engineering Dept, SRCEM, Gwalior India.

ABSTRACT

The Quantum effects instigate to dominate device recital when transistor geometries are abridged. Sometimes, transistors refrain to have the properties that mark them beneficial for computational designs. With the intention of keeping pace with Moore's Law, diverse assessing elements must be developed. An alternative prototype to transistor-based logic is Quantum dot cellular automata. This technology has an enormous capability to provide ultra-high density and extremely low power dissipation. These features allow us to develop high-speed, small and high performance circuits for computation and memory circuits. QCA have recently become the focus of interest in the field of low power nano-computing and nanotechnology.

The decoder in the QCA is very important circuit to address the QCA based random access memory array, RF-based Home Automation System, Automatic Wireless Health Monitoring System in Hospitals for Patients and Secret Code Enabled Secure Communication using RF Technology

In this paper, we realize the n to 2n decoder circuit with fundamental and functional realization of decoder algorithm. The design optimizes considerable reducing the number of q-cell count with removing crossover that minimizes the power consumption of the circuit. The proposed 2 to 4 decoder is more robust and enjoy single layer without wire crossing, via clock phasing, which require only one type of cells. The result shows that the proposed decoder circuit performs better than the exiting decoder circuits in all aspects. QCA Designer tool is used to validate the layout of the proposed designs.

Keywords: - Quantum Dot Cellular Automata, 2-to-4 Decoder, QCA, CMOS, VLSI, Nano-technology.

INTRODUCTION

A motivation towards nanotechnology is due to the limitations of scaling down of MOS structure in CMOS technology, because the scaling down of MOS leads to an increase in operating powers and latency. The microelectronic industry is experiencing new challenges for continuing the Moore's law [1]. Therefore, new alternatives are introduced to overcome the physical problems of CMOS [2]. Also, at the same time there are numbers of problems like short channel effects, tunneling effects etc. have been discovered, which have encouraged the need to find an alternative of CMOS technology. A quantum-dot cellular automaton (QCA) is one of the alternative nanotechnologies that are proposed to overcome such problems and take over the CMOS circuit designs. It has attained considerable worldwide attentions due to its attractive characteristics such as ultra-high speed (THz), high device density, and low power consumption of digital circuits in comparison to current CMOS technologies based circuit designs. Decoders are important digital circuit, which is generally used for addressing random access memory arrays. They can also be design in Quantum-dot cellular automata (QCA) technology at Nano-scale. Previously, a number of decoder designs have been proposed, but no one are actually efficient. QCA is a new digital system for next generation [3–4]. Majority gate [4] and Inverter cell [4] are two main primitive logic gates for circuit designs in QCA nanotechnology. Till now various QCA based logic Circuits have been implemented [4–15]. Majority gate and Inverter cell has desirable features to implement logic for QCA. However, still the logic is not competent and research is continuous due to the current trends of complexity, power and area constraints. Majority gate & Inverter cannot reduce the circuit complexity and maximizes the device density in QCA circuits alone. These gates are not functionally complete to design all logic circuits. The main focus of all new techniques is to reduce circuit parameters and excels these major issues.

Decoder is the most frequent combinational component used in digital logic systems. The Decoder is a very useful electronic circuit that has uses in many different applications such as signal routing, data communications and data bus control applications. Based on this various arrangements of the QCA cells widespread range of QCA Decoder designs are realizable [5–15]. A number of QCA decoders have been designed and implemented with the help of three majority gates. For Example in Figure they have implemented a decoder without enable input based on 3 input majority gates, during the design of Look up Table, a part of combinational logic block (CLB) of field programmable logic array (FPGA). Aim of this paper reducing the complexity of design structure by three input majority gate. This approach results in large unused area used which can be seen from comparison table.

This paper presents the simple and effective layout design of decoder digital circuit without using the property of crossover in the layout that used higher power compare to single layer circuit that not use the 90°crossover in the circuit that have enhanced the performance of several conventional designs in terms of power, area, clock delays and circuit complexity. The detailed comparison is of the proposed and conventional designs with regards to various characteristics are presented in the discussion. The organization of this paper is as follows, in section 2, QCA preliminary have discussed. In section 3, Proposed QCA decoder is presented. Section 4 represents QCA implementation of proposed decoder and its simulated output .Section 5, represents comparative study analysis of proposed decoders with existing one in all aspects. The last section 6 represents the conclusion.

QCA PRELIMNARIES

Quantum-Dot Cellular Automata (QCA) is another nano technology worldview which encodes twofold data by charge setup inside a phone rather than the regular current switches. There is no present stream inside the cells since the columbic cooperation between the electrons is adequate for calculation. This worldview gives one of numerous conceivable answers for transistor-less calculation at the nanoscale. The standard QCA cells have four quantum dots and two electrons [16]. There are different dots of QCA cells proposed which incorporate a six-dot QCA cell and an eight-dot QCA cell. In a QCA Cell, two electrons possess askew inverse spots in the cell because of shared shock of like charges. A case of a basic unpolarized QCA cell comprising of four quantum dots masterminded in a square is as appeared in Fig.1 dots are basically puts where a charge can be limited. There are two additional electrons in the cell those are allowed to move between the four dots. Burrowing in or out of a cell is smothered. The numbering of the dots in the cell goes clockwise starting from the dot on the top right.

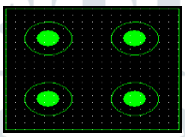


Figure 1 Simple 4-dot Unpolarized QCA cell.

A polarization P in a cell, that measures the extent to which the electronic charge is distributed among the four dots, is therefore defined as:

$$P = \frac{(\rho_1 + \rho_3) - (\rho_2 + \rho_4)}{\rho_1 + \rho_2 + \rho_3 + \rho_4}$$

Where **ρi** is the electronic charge in each dot of a four dot QCA cell. Once polarized, a QCA cell can be in any one of the two possible states depending on the polarization of charges in the cell. Because of columbic repulsion, the two most likely polarization states of QCA can be denoted as P = +1 and P = -1 as shown in Fig.2. The two states depicted here are called most likely and not the only two polarization states because of the small (almost negligible) likelihood of existence of an erroneous state.

Figure 2 P = +1 Binary Logic1 P =- 1 Binary Logic 0

LOGICAL DEVICES IN QCA

As found in the past areas, the data in QCA cells is exchanged due to columbic cooperation's between the neighbouring QCA cells; the condition of one cell impacts the condition of the other. The essential rationale gadgets in QCA are:

- Binary Wires.
- Inverter.
- Majority Gate Voter

Binary Wire

A paired wire can be seen as an even arrangement of cells to transmit data starting with one cell then onto the next. A case of a QCA wire is as appeared in Fig. 3. A parallel wire is regularly separated into different clock zones, to guarantee that the flag doesn't fall apart as signs for the most part have a tendency to debase with a long chain of cells in a similar timing zone.

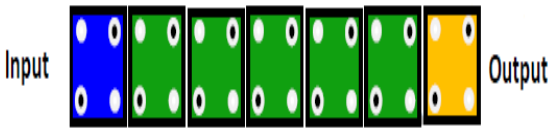


Figure 3 a QCA binary wire Realization

Inverter

Two diagonally aligned cells will have the opposite polarization. Henceforth, inverters can be implemented with lines of diagonally aligned cells. An example of a QCA Inverter is as shown in Figure

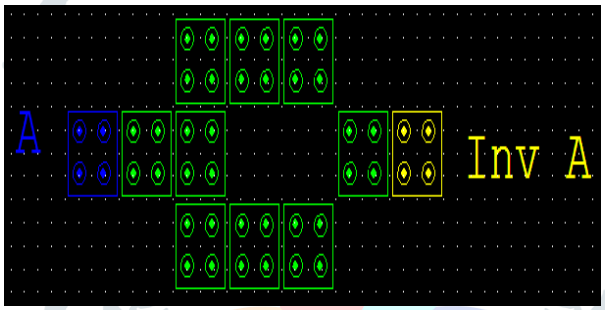


Figure 4 QCA designed inverter circuits

Majority Gate

Majority Gate (MV) is the fundamental logic block in any QCA design. A majority gate can be built with the help of five cells. The top, left and bottom cells are inputs. The device cell in the centre interacts with the three inputs and its result (the majority of the input bits) will be propagated to the cell on the right. An example of an MV representation in QCA is as shown in Fig. 5. The logic function implemented by the MV is

Consider the Coulombic cooperation between cells 1 and 4, cells 2 and 4, and cells 3 and 4. Coulombic connection between electrons in cells 1 and 4 would typically bring about cell 4 changing its polarization in light of electron aversion (accepting cell 1 is an info cell). Notwithstanding, cells 2 and 3 additionally impact the polarization of cell 4 and have polarization P=+1. Therefore, on the grounds that most of the cells impacting the gadget cell have polarization P=+1, it too will likewise accept this polarization on the grounds that the powers of Columbic collaboration are more grounded for it than for P=-1.

$$f(A,B,C) = A.B + B.C + C.A$$

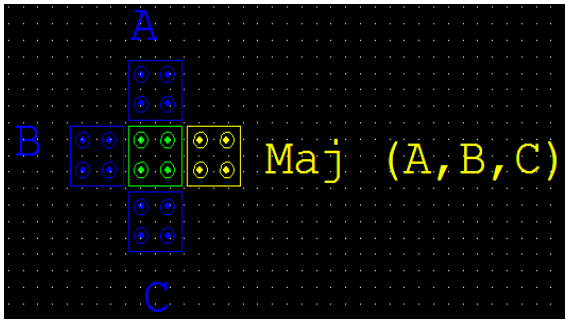


Figure 5 A three input majority gate

THE QCA CLOCK

This section will clarify and talk about how the QCA clockworks. Not at all like the standard CMOS clock, has the QCA clock had more than a high and a low stage. The periods of the QCA clock and illustrations are talked about underneath.

The check in QCA is multi-staged. Individual QCA cells are not planned independently. The wiring required to clock every phone exclusively could without much of a stretch overpower the disentanglement won by the natural neighbourhood interconnectivity of the QCA design [8]. Four phase switching realized in each clocking phase for different clock zones. Information flows in a pipelined fashion from inputs towards outputs during four clock zones.

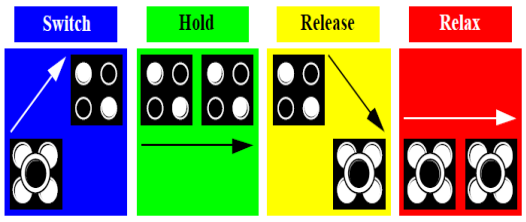


Figure 6 the four phases of the QCA clock

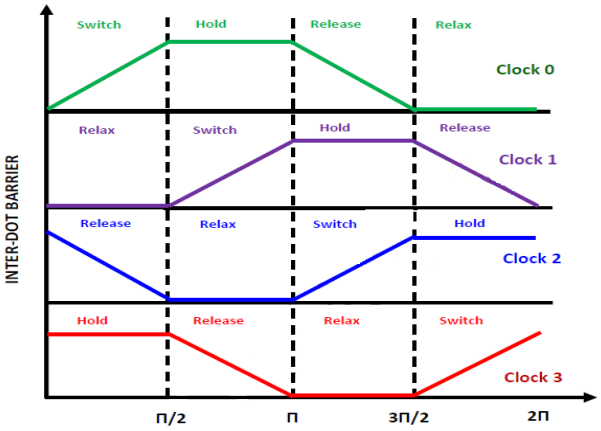


Figure 7 Clocking phases in different clock Zones

Now and time it merits specifying that there is some characteristic pipelining incorporated with the QCA innovation. After each 4 time steps, it is conceivable to put another esteem onto a QCA wire.

CROSSOVER

In QCA structures fabrication of interconnection between components needs to be handled efficiently for a better stability. Till now, there are two different types of crossover are available. These are coplanar and multilayer. In multilayer crossover, multiple layers are used as in CMOS circuit design for interconnection between components as depicted in Fig. In coplanar crossover strategy, wire crossing is done by two different cells. These cells are orthogonal to each other, so they operate without affecting neighboring cells. The first wire consists of cells of 90° orientations and second wire has only 45° orientations as shown in Fig. The main drawback of this scheme is that any misalignment of cells during fabrication may cause a cross coupling between the two wires. Works have been done to mitigate such effects, and also to increase the robustness of the circuits, but all these end up with large area overhead [14, 17]. Another type of coplanar wire crossing is addressed in S. H. Shin [13]. In this method wire crossing is based on interference of clocking phases as depicted in Figure.

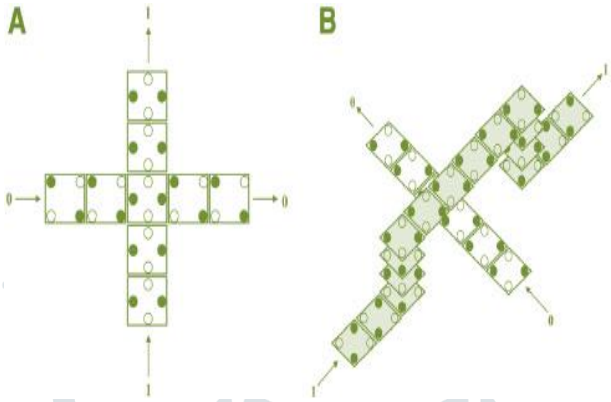


Figure 8 Different Type of Crossover

LITERATURE REVIEW

In this section, we discuss, a very useful digital logic circuits to access the memory array i.e. decoder circuits (2- to-4 decoder) in QCA. It is implemented with the help of three inputs majority gates, which is efficient in all aspects in comparison to previous 2-to-4 decoder designs in QCA. In Beginning, previous designs of 2-to-4 decoder, which is already successfully implemented in QCA, are presented and then our design is proposed.

Modular design methodology is first proposed in [31] to construct the 4-to-16 decoder. The latency of this decoder is only five clock cycles. The symmetrical fan out offers a solution to the problem where there is no wire crossing. There are five 2-to-4 decoders in a tree structure configuration to build a 4-to-16 decoder. This design uses AND, and delay (modular) blocks. Each decoder uses eight 2-input AND gates. Four of eight AND gates are used to enable or disable the output

In [32], a new modular-based design methodology is presented for QCA. The basic block of QCA cells for logic computation is referred to as a tile. In general, a tile can have many different topologies in the QCA layout. For generating stable and synthesis-amenable logic functions, a tile must have the following features: (1) Logic functions must have flexible tile at high polarization level. It is necessary to have strong tile to limit interactions from unwanted external cells. (2) Signals should be routed easily between and among tiles (such as with a Manhattan strategy). (3) A tile should have stable signals, in which an output should not suffer from weakened value due to lack of polarization or the presence of a glitch. 3 × 3 QCA grid is an example of a tile. The tiles based on the 3 × 3 QCA grid provide universal logic functions and are flexible for logic design. The non-fully populated tile is defined as a tile in which one or more QCA cells are undeposited. The 2-to-4 decoder using the 3 × 3 grid as part of the tile achieves a reduction in an area and in the number of clocking zones.

This design has 588 cells.

A 4-to-16 decoder in [6] has five-layered structure. The inputs are placed in the middle layer (layer 3) and they move up and down. A recently designed 7 input majority gate is used as 4-input AND gate in the decoder design. For each different input, the decoder gives 16 different outputs (0–15), which address the memory cells. There is the same clock vertically in all layers due to layer clocking. The decoder of one clock cycle has less latency in comparison with other decoders. Higher input majority gates in multiple layers reduce the cell count and latency compared to other designs.

In [2], the circuit of the 2-to-4 decoder is designed using the 3-input majority gate in QCA. This circuit includes eight majority gates. A 5-input majority gate is needed for performing a logical 2-to-4 decoder [13] in QCA. Eight majority gates are required for increasing the delay and complexity in the circuit using traditional methods. The implemented decoder has four 5-input majority

gates arrayed as AND. This circuit reaches the output in 7 clock phases (1.75 clock cycles) and includes two inputs and an enabled input. When the EN
input is inactive (EN = 0), all output will be passive. When the EN is active (EN = 1), the outputs will appear with respect to inputs A and B. The decoder provides high consistency in the output and EN input makes it a controllable module. This 2-to-4 decoder consists of 268 cells covering an area of 0.3 lm2.
Finally, In [1] It requires four 5- majority gates and two inverters as shown in Fig.8. According to Fig. 8, the proposed decoder is composed of two separate blocks. The first block includes inputs and inverter gate, and the other block includes a five-input majority generates the output signal. Total of these blocks is implemented in a single layer design. This QCA-based design uses 193 quantum cells.

PROPOSEED DESIGNS

In, previously we have discussed about various type of logical structure design of 2-to-4 decoder, which has presented earlier. They have implemented their designs with general methods. They implemented the structural design, with eight three input majority gates and with four five input majority gates. However neither of designs is checked carefully and hence these circuits' takes large area, crossover and latency. This motivated us to optimize these designs which should be efficient in all aspects. There has many articles on design memory and implementation of CLB of FPGA in QCA [3-5], in which 2-to-4 decoder is requires for addressing the memory array. For example, in to build an four bit Look up Table (LUT), While, 2-to-4 decoder presented in this paper, needs only four three-input majority gate to implement this, which function as three-input AND gate. The output of this decoder is visualizes with same clocks phases and it has two wire lines, of inputs A & B The schematic representation of the decoder circuit shown in Figure 10. It has two data inputs **A** and **B**, and four output lines **D0**, **D1**, **D2** and **D3**. The block diagram is shown in Figure 9. The truth table is shown in table 1:

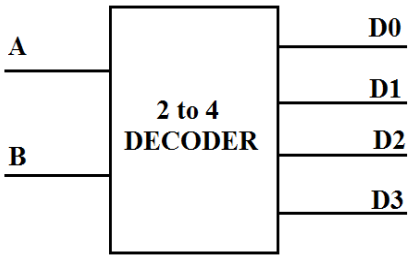


Figure 9 basic block diagram of Decoder

A	B	D0	D1	D2	D3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Table: Truth Table of 2 to 4 Decoder

The layout and simulation results of the proposed decoder design are shown in Figure 11 and 12 respectively. As is obvious, the output generate meticulous highly polarized signals (shown inside the rectangles) leading to provide a high drivability for the circuit. The proposed design consists of an area 51884 nm^2, circuit complexity of 12 cells and latency of 0.5 clock delays.
Use recommends a viable answer for intelligent wiring with a lessened number of external fixed input cells giving settled sources of info. In a run of the nano QCA circuit, both 0 and 1 fixed input are expected to execute a capacity. The proposed strategy introduces settled esteem generator equipment which can lessen the quantity of required fixed inputs.

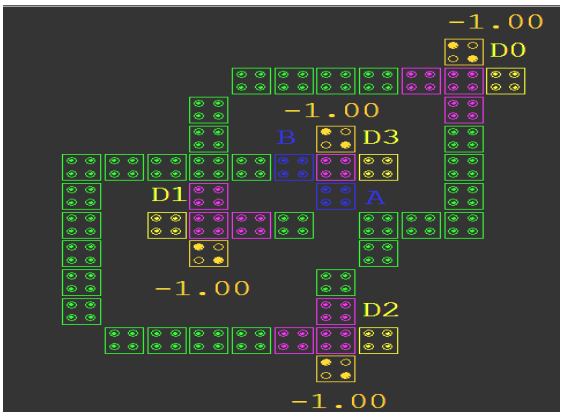
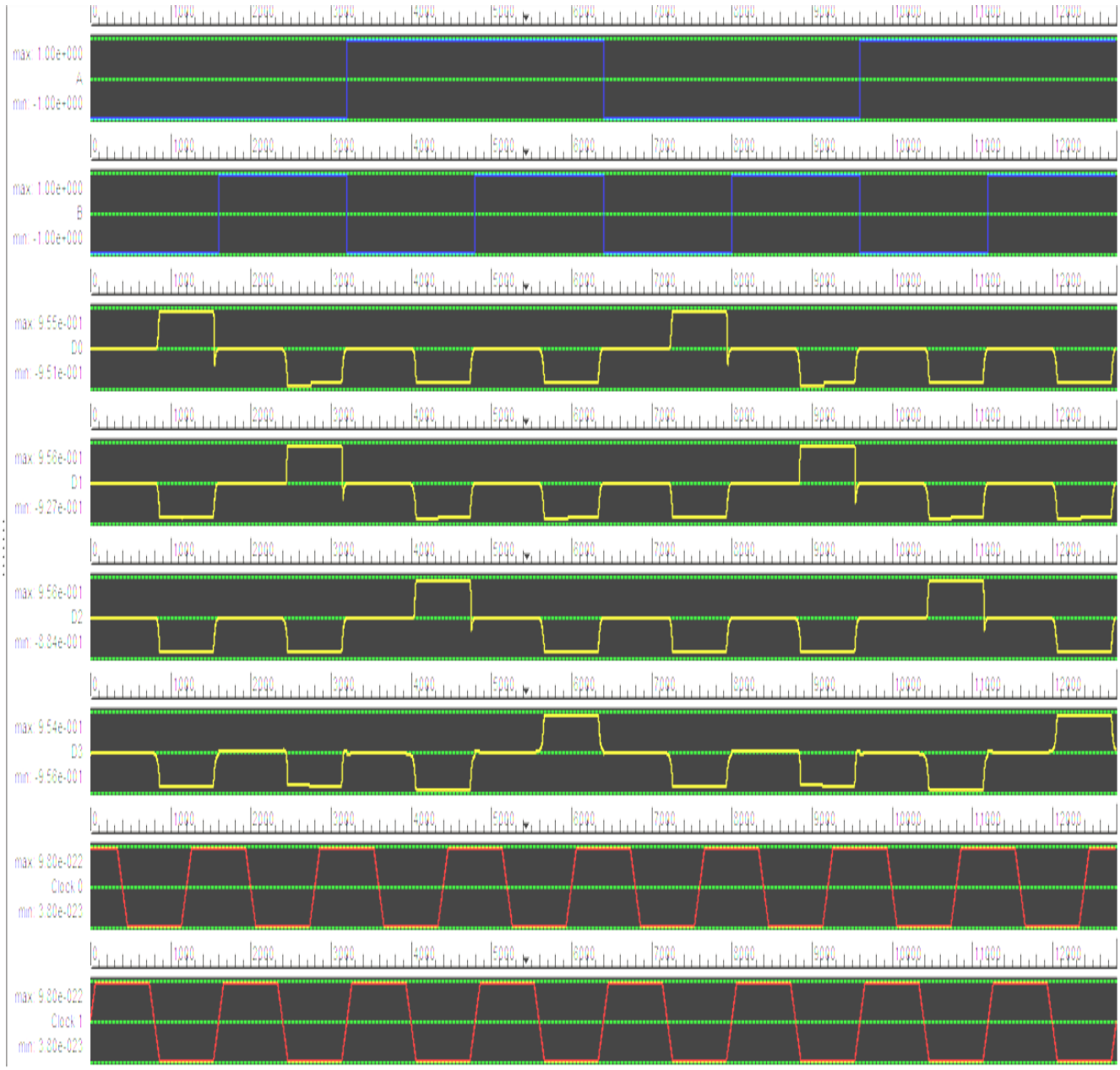


Figure 10 Layout of Propose Decoder Design

SIMULATION RESULT AND ANALYSIS

All the designs which are presented in this paper have been justified using the simulation tools QCA Designer- 2.0.3 with default parameters have been used for verified the functionality of the proposed QCA-circuits. The default parameters are listed as: QCA cell size=18 nm, diameter of quantum dots = 5 nm, number of samples = 12, 8000, convergence tolerance = 0.001, radius of effect = 65 nm relative permittivity = 12.9, clock low = 3.8e−23 J, clock high = 9.8e-22 J, clock amplitude factor = 2.000, layer separation = 11.5 nm and maximum iterations per sample = 100.The output is obtained by choosing simulation engine to coherence vector type. Fig.11 and 12 shows simulated output of proposed 2-to-4 decoder. The output curves successfully represent all four combinations of inputs A & B However; outputs are achieved with same phases of clock cycle.

The main focus of this implementation is to reduce circuit complexity and increase efficiency. To procure highly integrated QCA layouts, several new methods have been used to propose decoder circuits have reduce maximum number of cell counts, reduced clock delays and consists of less area in comparison to Accordingly, However, in contrast, the proposed decoder shown in Fig. 10 has an influential role in overall circuit performance in terms of area occupation and cell counts as shown in Table 2. It is implemented using explicit QCA fixed cells. The proposed decoder has been testified for designing


max: 1.00e+000
A
min: -1.00e+000
max: 1.00e+000
B
min: -1.00e+000
max: 9.55e-001
D0
min: -9.51e-001
max: 9.58e-001
D1
min: -9.27e-001
max: 9.58e-001
D2
min: -8.84e-001
max: 9.54e-001
D3
min: -9.58e-001
max: 9.80e-022
Clock 0
min: 3.80e-023
max: 9.80e-022
Clock 1
min: 3.80e-023

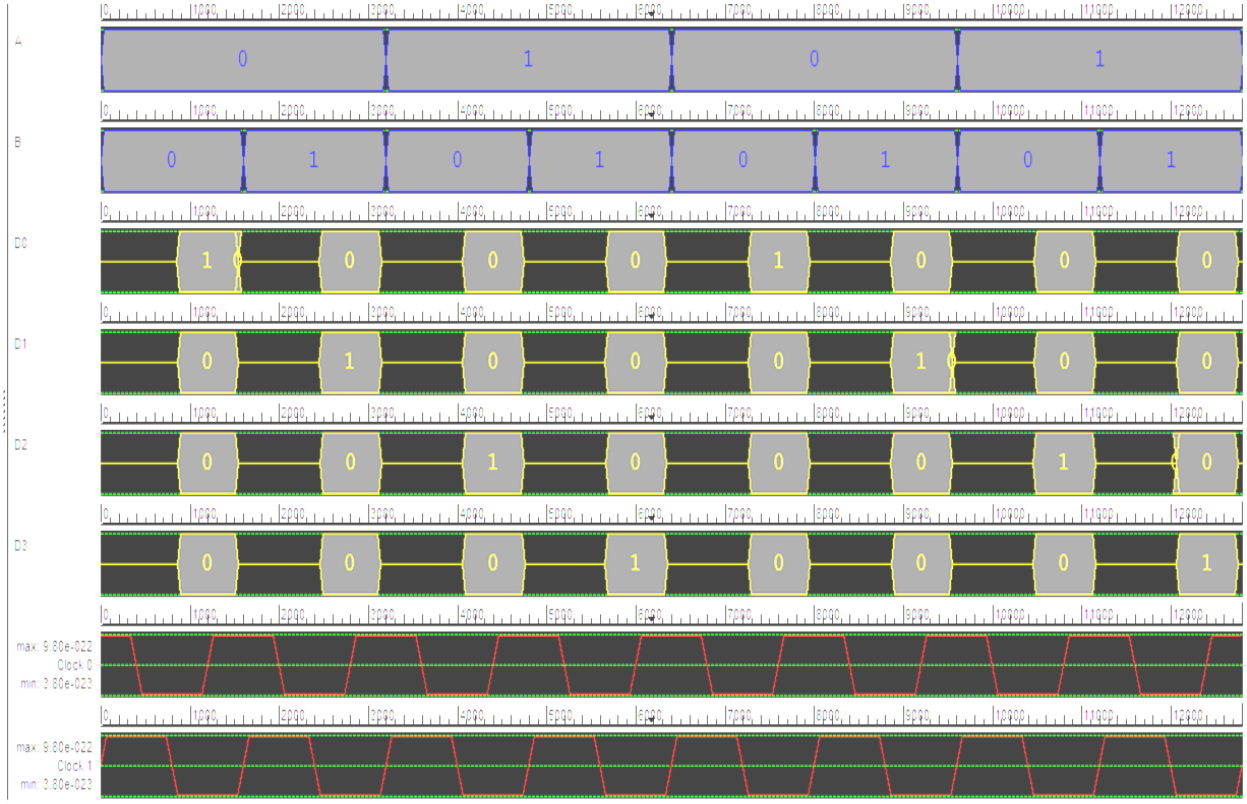
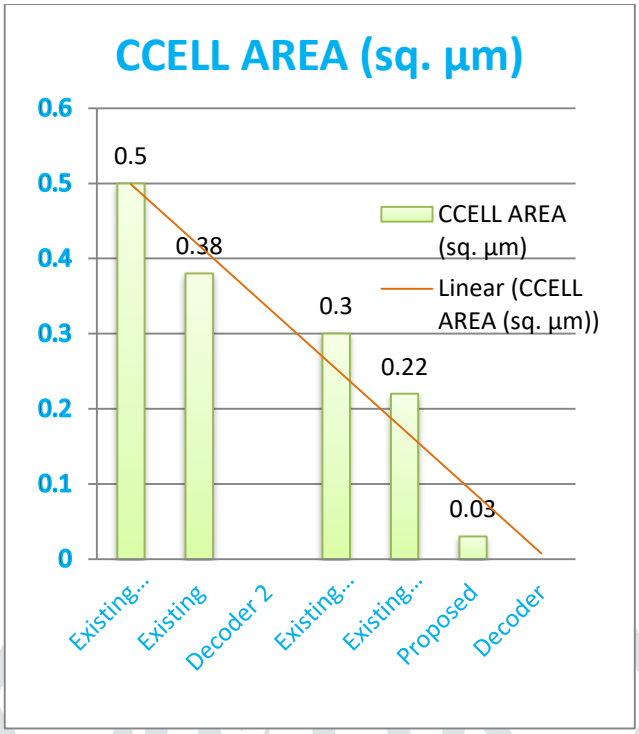


Figure 12 Simulation Bus Wave form Decoder design

Table 2: Comparison Table between exiting and proposed decoders

DESIGN	CELL COUNT	CCELL AREA (sq. µm)	CLOCK ZONE	CROSSOVERE
Existing Decoder 1	318	050	7	Yes
Existing Decoder 2	270	0.38	7	Yes
Existing Decoder 3	268	0.30	7	Yes
Existing Decoder 4	193	0.22	3	Yes
Proposed Decoder	49	0.03	1	No



Graph between area, cell area of existing and proposed design

As shown in Comparison table and graph shows the our proposed multiplexer design improved to exiting decoder designs in terms of area, cell count and the clock used in the design that calculate the delay of the design how much clock used in the design than delay are increased in the design circuit and latency are poor in that case.

CONCLUSION

In this paper an efficient 2-to-4 decoder has been presented, which is optimal in all aspects in comparison to other designs presented in this paper. We have simulated our design with the help of simulation tools "QCA Designer- 2.0.3". The proposed decoder is optimum in both "area complexity as well as in latency", in comparison to earlier designs of 2-to-4 decoder circuit. In terms of area complexity, the presented design requires optimum number of cells and this reduction in number of cells makes the circuit more compact and stable, which enjoys its extension with other structures like RAM and improves their performance.
Research is also needed for using the proposed design without wire crossing techniques in more complex circuits and the principal of using the dead computation time in clocking scheme should be exploited. Circuits that make use of clocking scheme can be designed and tested for efficiency in terms of power and performance.

.

REFERENCES

1. Robab Sherizadesh, Nima Jafari Navipour. Designing a2-4-to4 decoder on nano-Scale based on quntum-dot cellular automata for energy dissipation improving.S0030-4026(17)31693-5;IJLEO 60177; https://doi.org/10.1016/j.ijleo.2017.12.055
2. Lent, C.S., Bypassing the transistor paradigm. Science, 2000. 288(5471): p. 1597-1599.
3. Kianpour, M. and R. Sabbaghi-Nadooshan, A conventional design and simulation for CLB implementation of an FPGA quantum-dot cellular automata. Microprocessors andMicrosystems, 2014. 38(8): p. 1046-1062.
4. Mardoukhi, Y. and E. Räsänen, Optimal control of charge with local gates in quantum-dot lattices. The European Physical Journal B, 2014. 87(6): p. 144.
5. Tougaw, D., J. Szaday, and J.D. Will, A signal distribution grid for quantum-dot cellular automata. Journal of Computational Electronics, 2016. 15(2): p. 446-454.
6. Alkaldy, E., K. Navi, and F. Sharifi, A Novel Design Approach for Multi-input XOR Gate Using Multi-input Majority Function. Arabian Journal for Science and Engineering, 2014. 39(11): p.7923-7932.
7. Ghosh, B., J.S. Chandra, and A. Salimath, DESIGN OF A MULTI-LAYERED QCA CONFIGURABLE LOGIC BLOCK FOR FPGAs. Journal of Circuits, Systems, and Computers, 2014. 23(06): p. 1450089.

8. Sheikhfaal, S., et al., Designing efficient QCA logical circuits with power dissipation analysis. Microelectronics Journal, 2015. 46(6): p. 462-471.

9. Seitz, C.L., System timing. Introduction to VLSI systems, 1980: p. 218-262.

10. Kianpour, M. and R. Sabbaghi-Nadooshan. A novel modular decoder implementation in quantum-dot cellular automata (QCA). in Nanoscience, Technology and Societal Implications (NSTSI), 2011 International Conference on. 2011. IEEE.

11. Afroz, S. and N.J. Navimipour, Memory designing using quantum dot cellular automata: systematic literature review, classification, and current trends. Journal of Circuits, Systems, and Computers, 2017.

12. Seyedi, S. and N.J. Navimipour, An optimized design of full adder based on Nanoscale quantumdot cellular automata. Microprocessors and Microsystems, 2017.

13. Sasamal, T.N., A.K. Singh, and A. Mohan, An optimal design of full adder based on 5-inputmajority gate in coplanar quantum-dot cellular automata. Optik - International Journal for Lightand Electron Optics, 2016. 127(20): p. 8576-8591.

14. Navi, K., et al., A new quantum-dot cellular automata full-adder. Microelectronics Journal, 2010.41(12): p. 820-826.

15. Orlov, A., et al., Realization of a functional cell for quantum-dot cellular automata. Science,1997. 277(5328): p. 928-930.

16. Blair, E.P., E. Yost, and C.S. Lent, Power dissipation in clocking wires for clocked molecularquantum-dot cellular automata. Journal of computational electronics, 2010. 9(1): p. 49-55.

17. Kianpour, M. and R. Sabbaghi-Nadooshan. A conventional design for CLB implementation of aFPGA in quantum-dot cellular automata (QCA). in Proceedings of the 2012 IEEE/ACM International Symposium on Nanoscale Architectures. 2012. ACM.

18. Bhanja, S., et al., QCA circuits for robust coplanar crossing. Journal of Electronic Testing, 2007.23(2-3): p. 193-210.

19. Angizi, S., et al., Novel robust single layer wire crossing approach for exclusive or sum of productslogic design with quantum-dot cellular automata. Journal of Low Power Electronics, 2014. 10(2): p. 259-271.

20. Das, J.C. and D. De, User Authentication Based on Quantum-Dot Cellular Automata Using Reversible Logic for Secure Nanocommunication. Arabian Journal for Science and Engineering, 2016. 41(3): p. 773-784.

21. Das, J.C. and D. De, Operational efficiency of novel SISO shift register under thermal randomnessin quantum-dot cellular automata design. Microsystem Technologies, 2016: p. 1-14.

22. Mohammadi, Z. and M. Mohammadi, Implementing a one-bit reversible full adder using quantum-dot cellular automata. Quantum Information Processing, 2014. 13(9): p. 2127-2147.

23. Cho, H. and E.E. Swartzlander Jr, Adder and multiplier design in quantum-dot cellular automata.IEEE Transactions on Computers, 2009. 58(6): p. 721-727.

24. Lent, C.S. and P.D. Tougaw, A device architecture for computing with quantum dots. Proceedingsof the IEEE, 1997. 85(4): p. 541-557.

25. Amiri, M.A., M. Mahdavi, and S. Mirzakuchaki. QCA implementation of a mux-based FPGA CLB.in Proc. Int. Conf. on Nanoscience and Nanotechnology. 2008.

26. Timler, J. and C.S. Lent, Power gain and dissipation in quantum-dot cellular automata. journal ofapplied physics, 2002. 91(2): p. 823-831.

27. Tougaw, P.D. and C.S. Lent, Dynamic behavior of quantum cellular automata. Journal of AppliedPhysics, 1996. 80(8): p. 4722-4736.

28. Liu, W., et al., Are QCA cryptographic circuits resistant to power analysis attack? IEEEtransactions on nanotechnology,2012.11(6):p.1239-1251