Two stage conversion based SMPS for high Power Application

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Abstract: Designing of Switched mode power supply (SMPS) involve many challenges while developing for specific application. This study proposes two stage conversion based SMPS design with Interleaved boost as PFC stage and Phase shifted full bridge as DC-DC converter stage. The design is simulated to obtain 600W,16V output DC for universal input AC range. Stage wise power analysis is done which produces 98.48% and 93.27% efficiency for PFC and DC-DC converter stages respectively.

Index terms- SMPS, PFC, Interleaved boost, Phase shifted full bridge

Nomenclature-

\[ \begin{align*} 
V_{IN} & = \text{Rectified input voltage} \\
V_{OUT} & = \text{PFC stage output voltage} \\
I_{ripple} & = \text{Input ripple current at the PFC side} \\
P_{OUT} & = \text{Output Power of SMPS} \\
V_{OUT} & = \text{Output voltage of SMPS} \\
\eta & = \text{Converter stage efficiency} \\
 f_{LINE} & = \text{Input line frequency} \\
f_s & = \text{Switching frequency in converter stage} \\
D & = \text{Duty cycle of converter stage} \\
I_{ripple} & = \text{Output ripple current of converter stage} \\
V_{RDSON} & = \text{Voltage drop across MOSFET} \\
\end{align*} \]

I. INTRODUCTION

Switched mode power supplies are most popular power supply option in most of the industrial applications. SMPS term was first used in 1976 which was patent on power supply circuit for TV receiver. During 70s most of the application started moving from conventional linear supply to SMPS. Unlike linear supply which requires large transformer to convert low frequency AC to higher or lower voltage, SMPS is operated in high frequencies which reduces their sizes an make them compact.

A basic SMPS involves a switching element (MOSFETs or IGBTs) in which the switching is controlled by a controller which generates square wave according to the duty cycle requirement. This duty cycle will depend on the output voltage requirement and the input voltage. In some of the SMPS design a high frequency transformer used which is used to step down the DC voltage according to the output voltage requirement. While designing a SMPS one can choose different topology for the DC-DC conversion. There are non-isolated topologies such as Buck, Boost and isolated topologies such as Fly back, Forward, Half bridge, Full bridge topologies are popular. Each topology has its own limitations with respect to operating voltages and Power. For high power applications (greater than 500W) Half bridge and Full bridge topologies are more preferred. A phase shifted full bridge is the improved version of the full bridge which reduces the switching power losses by Zero Voltage Switching \[2\].

When AC signal drawn from the source, the Voltage (V) and the Current (I) might not be in phase with each other. This might be due to any passive component involving the circuit. Which leads to the lower value of the power received than the expected one. Due to the high-power application there might exists harmonic component of the input power i.e. the components of the input power with lower magnitude at different fundamental frequencies. A PFC circuit provide solution for both these cases \[3\].

Different equipment needs different supply based on the rating of the design. In many cases there might not be off the shelf product available for given specification. So, one must design customized product based on the specifications such as wattage, voltage rating. This work involves designing of Switch mode power supply module that gives 600W,16V DC output. SMPS design with two stages (Power factor correction and DC-DC converter) is proposed to meet the specification.

II. METHODOLOGY

The proposed SMPS architecture consists of mainly two stages i.e. Power factor correction stage and a DC-DC converter stage as shown in the Figure 1.
2.1 Rectification
Rectification is the conversion of the input AC to DC. For this one can use diode bridge. The universal input AC is converted to the DC in this stage.

2.2 Power Factor Correction (PFC)
Power factor correction block involves circuits that is used to maximize the real power available from the input. Due to various passive components the input voltage and current are not in phase. Also, high power input leads to the harmonic components. PFC circuits helps in reduction of harmonic losses as well as it makes sure that current and voltages are in phase. In the proposed design Interleaved boost type of PFC is chosen which gives nominal output voltage of 390V.

2.3 DC-DC Converter
This is the core block of SMPS which involves conversion of high DC input to lower DC voltage which will be constant throughout the time. SMPS converter block involves switching element which will be controlled by a controller which controls duty cycle given to the switch based on feedback provided by the output end. Designing of converter block is critical. Selection of topology and components based on the operating voltage and power plays important role. The design proposes Phase shifted full bridge converter to produce 16V DC from PFC stage output.

III. Design and Implementation of Two Stage SMPS
Based on proposed architecture 600W,16V SMPS is designed. Table 3.1 indicates the specification considered for the design. Universal AC of range 85-265V with line frequency 47-63Hz is considered as the input.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Terminology</th>
<th>Unit</th>
<th>Min</th>
<th>Typical</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage (AC)</td>
<td>$V_{ac}$</td>
<td>V</td>
<td>85</td>
<td></td>
<td>265</td>
</tr>
<tr>
<td>Line frequency</td>
<td>$f_{line}$</td>
<td>Hz</td>
<td>47</td>
<td></td>
<td>63</td>
</tr>
<tr>
<td>Output Power</td>
<td>$P_{OUT}$</td>
<td>W</td>
<td>600</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Voltage (DC)</td>
<td>$V_{OUT}$</td>
<td>V</td>
<td>16</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### 3.1 PFC Design
PFC stage comes before DC-DC converter stage do the job of maintaining low harmonics and maximizing power factor. In this design Interleaved boost PFC is selected which best suited for the PFC specification defined before design. Table 3.2 gives the input specification considered. Figure 2 shows two cell interleaved PFC circuit used for the design.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Terminology</th>
<th>Unit</th>
<th>Min</th>
<th>Typical</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage (AC)</td>
<td>$V_{ac}$</td>
<td>V</td>
<td>85</td>
<td></td>
<td>265</td>
</tr>
<tr>
<td>Output Power</td>
<td>$P_{OUT}$</td>
<td>W</td>
<td></td>
<td></td>
<td>750</td>
</tr>
<tr>
<td>Output Voltage (DC)</td>
<td>$V_{OUT}$</td>
<td>V</td>
<td>370</td>
<td>390</td>
<td>410</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>$f_s$</td>
<td>kHz</td>
<td></td>
<td>200</td>
<td></td>
</tr>
<tr>
<td>Efficiency</td>
<td>$\eta'$</td>
<td>%</td>
<td>90</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Duty cycle</td>
<td>$D'$</td>
<td></td>
<td></td>
<td></td>
<td>0.97</td>
</tr>
</tbody>
</table>

![Figure 2. Circuit used for Interleaved boost PFC](image)

3.1.1 Inductor Selection
Boost inductors L1 and L2 are selected based on the duty cycle value. And the operating duty cycle is calculated using Eq.1. With the calculated duty cycle inductor values are determined using Eq.2.

$$D' = 1 - \frac{V_{in}}{V_{OUT}} \quad (1)$$
\[ L_1 = L_2 = \frac{V_{\text{OUT}}' \times D'(1-D')}{f_s \times I_{\text{ripple}}} \]  

(2)

The input ripple current \( I'_{\text{ripple}} \) is calculated based on maximum rms current at the input. Eq.3 gives maximum rms current. And the Eq.4 indicates \( I'_{\text{ripple}} \).

\[ I_{\text{line, max}} = \frac{P_{\text{OUT}}'}{\sqrt{V_{\text{ac, min}}}} \]  

(3)

\[ I'_{\text{ripple}} = 0.5 \times I_{\text{line, max}} \]  

(4)

3.1.2 Capacitor Selection

The minimum value of the output capacitor can be determined using the Eq.5.

\[ C'_{\text{OUT}} \geq \frac{2 \times P_{\text{OUT}}'}{I_{\text{LINE}} \times (V'_{\text{OUT}})^2 - (V'_{\text{OUT}} \times 0.75)^2} \]  

(5)

3.1.3 MOSFETs Selection

In order to sustain input voltage stress and the rms current condition MOSFETs Q'1 and Q'2 are selected with 500V drain to source voltage capacity, 11A max current capacity.

3.3 DC-DC converter design

DC-DC converter is second stage of the proposed design. High DC output produced in the PFC stage is converted to the final required DC voltage. Table 3.3 gives the parameter considered for the DC-DC converter design. Phase shifted Full bridge topology is selected for the design. Figure 3 shows the topology used in the designing of the converter. The design based on synchronous rectifiers at the secondary side of the transformer as shown in the Figure 3.

<table>
<thead>
<tr>
<th>TABLE 3.3 DC-DC converter Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameter</td>
</tr>
<tr>
<td>Converter stage input voltage</td>
</tr>
<tr>
<td>Output Power</td>
</tr>
<tr>
<td>Output Voltage (DC)</td>
</tr>
<tr>
<td>Switching frequency</td>
</tr>
<tr>
<td>Efficiency</td>
</tr>
<tr>
<td>Duty cycle</td>
</tr>
</tbody>
</table>

\[ \alpha_1 = \frac{(V_{\text{IN,MIN}} - 2 \times V_{\text{RDS,ON}}) \times D_{\text{MAX}}}{V_{\text{OUT}}' + V_{\text{RDS,ON}}} \]  

(6)

The magnetic inductance is calculated by the Eq.7. And the Eq.8 give the duty cycle of the square wave given to the switching elements. For the calculation allowed output ripple current \( I_{\text{ripple}} \) is assumed as \((0.2 \times I_{\text{OUT}})\).

\[ L_{\text{MAG}} \geq \frac{V_{\text{IN}}(1-D_{\text{typ}})}{f_s \times 0.5 \times \alpha_1} \]  

(7)

\[ D_{\text{typ}} = \frac{(V_{\text{OUT}}' + V_{\text{RDS,ON}}) \times x_{\alpha_1}}{(V_{\text{IN}} - 2 \times V_{\text{RDS,ON}})} \]  

(8)

Figure 3. Circuit used for Phase shifted full bridge

3.2.1 Transformer Selection

The transformer used in the design is center tapped with one primary end two secondary coils. The turns ratio is calculated by the Eq.6.
3.2.2 Output inductor Selection
The output inductor value mainly depends on the output ripple current. Its value is calculated using Eq.9.

\[ L_{OUT} = \frac{V_{OUT} \times (1 - D_{TPP})}{I_{ripple} \times f_s} \]  

(9)

3.2.3 Output capacitor Selection
The output capacitor is selected based on the holdup time requirement. Eq.10 gives the holdup time condition and the Eq.11 gives the minimum value of output capacitor.

\[ t_{HU} = \frac{L_{OUT} \times P_{OUT} \times 0.9}{V_{OUT}} \]  

(10)

\[ C_{OUT} \geq \frac{P_{OUT} \times 0.9 \times t_{HU}}{V_{TRAN} \times 0.1} \]  

(11)

3.1.4 MOSFETs Selection
In order sustain input voltage stress, considering power and efficiency parameters MOSFETs Q1-Q4 are selected with 650V drain to source capacity, 20A max current capacity (Power MOSFETs). And MOSFETs Q5 and Q6 are selected with 75V drain to source capacity, 120A max current capacity.

3.4 Controller ICs for the design
Both PFC stage and the converter stage involves two separate controller ICs to produce square wave according to output voltage. UCC28950 controller is used for Phase shifted full bridge design and UCC28070 is used for Interleaved boost PFC design.

IV. SIMULATION RESULTS
Proposed design is simulated using TINA-TI Spice simulation tool. Transient response for each stage is observed by considering input AC as 230V, 50Hz. The design is verified for universal range. Figure 4 and Figure 5 shows the steady state output voltage waveforms at the PFC and converter stage respectively. The steady state output 15.89 V is obtained as shown in the Figure 5. The variation in the output voltage compare to the expected 16V is due to non-ideal characteristics of MOSFETs and the controller ICs.
Power Analysis is done to measure the output power and efficiency of each stages. Figure 6 shows the output power waveform. At steady state 596.47W output power ($P_{OUT}$) is observed.

Table 4.1 gives the efficiency of each stages and the line and load regulation of the design. With the design 98.48% efficiency at PFC and 93.27% efficiency at the converter stage is achieved.

### TABLE 4.1 Simulation results

<table>
<thead>
<tr>
<th>Stage</th>
<th>Efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>PFC stage</td>
<td>98.48%</td>
</tr>
<tr>
<td>Converter stage</td>
<td>93.27%</td>
</tr>
<tr>
<td>Overall</td>
<td>91.85%</td>
</tr>
<tr>
<td>Line regulation</td>
<td>0.05%</td>
</tr>
<tr>
<td>Load regulation</td>
<td>6.92%</td>
</tr>
</tbody>
</table>

**REFERENCES**


