Reduced Power and Delay using Fault Tolerant Technique in Self-Healing Architecture

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Abstract: **Hardware systems have been proposing imitations to biological organisms in the way they offer healing and recovery abilities. Digital systems with inspired homogeneous architecture have improved capabilities to compensate for any faults. Self-healing is defined by the ability of a system to detect faults or failures and fix them. The problems in current self-healing approaches is area overhead and scalability for complex structures considering they are based on redundancy and spare blocks. This project proposes a different approach for self-healing based on embryonic structures without a need for spare cells. The area overhead is lower compared to other approaches relying on spare cells. The proposed approach relies on time multiplexing two functions in one cell within one clock cycle. The reliability of the proposed technique is studied and compared to conventional system with different failure rates. This approach is capable of healing the cells where each cell can cover another neighbour failed cell at most. The area overhead for the proposed approach is much lower compared to other approaches using spare cell. The proposed architecture uses fault tolerant self healing architecture with embryonic reconfigurable hardware which helps in reducing the drawbacks of existing systems. The designs are synthesized by using Xilinx ISE 14.5 Tools and are functionally verified by using ISIM Simulation tool. The proposed algorithm implements the designin proposed when compared to existing design and 65% and 3% respectively.**

***IndexTerms*– Self-Healing, Embryonic hardware, Fault tolerant, Evolvable hardware.**

1. INTRODUCTION

With the increase in complexity of electronic circuits and systems, hardware failures happen due to heating, aging or surrounding environment parameters during operation. Such failures will be a hindrance to the system in order to work properly. Self-healing is a key approach for reliable electronic systems that run under harsh environments, such as cosmic radiation and cruel temperature in space applications. Self healing is done via multiple approaches and many of them are based on redundancy which relies on recovering faulty cells and the reintegration of them back into the system. Self-repair is the replacement of faulty cells by functioning spare cells. Self-healing term can be used for both concepts. The role of self healing is to recover the fault in the system to maintain the operation with highest performance and longest time possible. Self healing is done via multiple approaches and many of them are based on redundancy which relies on recovering faulty cells and the reintegration of them back into the system. Self-repair is the replacement of faulty cells by functioning spare cells.

Self-healing term can be used for both concepts. The role of self healing is to recover the fault in the system to maintain the operation with highest performance and longest time possible. Some of the self healing research in the circuit level is based on the circuit replication [1], [2]. Where, the faulty cell is replaced by the spare one after the detection of a faulty cell by the controlling part. Self-healing can be achieved in systems over different levels. The first is application level healing [3], which is the ability of an application, or a service, to heal itself. Next comes the System level healing [4], [5] which depends on a programming language and design patterns that we apply internally. Finally, the level of hardware healing from architecture and down to circuit techniques is the lowest level of healing [6].

There are multiple methods for self-healing such as Dual Modular Redundancy (DMR) [7], Triple Modular Redundancy (TMR) [8], Embryonic Hardware EmHW [6], [9], as well as other techniques like evolvable hardware and Intelligent Hardware System (IHW) framework that are designed with healing capabilities in mind [10]. DMR and TMR are two types of redundancy techniques. In DMR technique, there are two identical instances running in parallel for the same application and their outputs are connected to a comparator that triggers a mismatch whenever a fault occurs. TMR has three identical modules running in parallel to provide fault masking by a majority voter at their outputs to mask a signal fault. Embryonic hardware is a hardware system with self-healing based on replication of small building blocks with exact architecture and it is inspired by the multicellular organisms cell division and differentiation mechanisms. The drawbacks of current techniques are area and power consumption where they require redundant hardware which is an extra overhead. EmHW is the same principle of self healing mechanism of multi-cellular organisms for fault tolerance hardware system. Similar to multi-cellular organisms in nature the structure of circuits based on EmHW is two-dimensional array of electronic cells (e-cell) with hardware reconfiguration capability. E-cells have the abilities of adaptive self-healing (recovering) based on its structure.

This paper is organized as section II describes Literature review and in section III discussed about concept of vehicle tracking and Section IV describes in Proposed System methodology and Section V shows the Experimental results of proposed methods and section VI concludes the paper followed by references.

2. EXISTING SYSTEM

The self healing research in the circuit level is based on the circuit replication where, the faulty cell is replaced by the spare one after the detection of a faulty cell by the controlling part. Self-healing can be achieved in systems over different levels. The first is application level healing, which is the ability of an application, or a service, to heal itself. Next comes the System level healing which depends on a programming language and design patterns that we apply internally. Finally, the level of hardware healing from architecture and down to circuit techniques is the lowest level of healing. There are multiple methods for self-healing such as Dual Modular Redundancy (DMR), Triple Modular Redundancy (TMR), Embryonic Hardware EmHW, as well as other techniques like evolvable hardware and Intelligent Hardware System (IHW) framework that are designed with healing capabilities. DMR and TMR are two types of redundancy techniques. In DMR technique, there are two identical instances running in parallel for the same application and their outputs are connected to a comparator that triggers a mismatch whenever a fault occurs. TMR has three identical modules running in parallel to provide fault masking by a majority voter at their outputs to mask a signal fault. Embryonic hardware is a hardware system with self-healing based on replication of small building blocks with exact architecture and it is inspired by the multicellular organisms cell division and differentiation mechanisms.

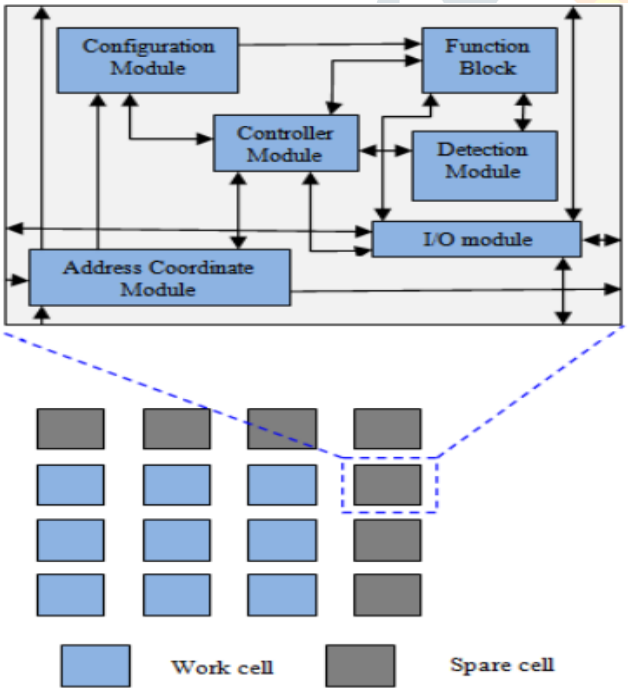


Fig. 1: Embryonic Hardware Architecture

A. *Self-Healing Technique*

Most of self healing approaches are based on redundancyby adding spare cells. When a failure happens, the faulty cellsare replaced by the spare cells after detection of faults. Alongwith the mentioned area overhead and scalability, the mappingof spare cells may cause delay overhead after self-healingbecause the nearest spare cell is very far away from the faultyone. For improved mapping and system's performance, addingmore spare cells will help but on the other side the area willbe higher. The area overhead can be reduced by adding lessspare cells. Less spare cells leads to major mapping challengesand more complex healing system with increasing number offaults over time and whole system failure or delays.

The proposed approach provides self-healing without addingspare cells which overcome area overhead problems. Authors proposed approach treats each cell as a spare cell for itsneighbor. Also, each cell can do its task and the task of theneighbor cell. The proposed technique is based on time divisionmultiplexing for self-healing. Each cell will be capableto run two tasks within the same clock when a fault happens.One operation runs during the first half of the clockcycleand the second during the other half of the clock. If the faultdetection module detects a fault then the neighbor of the faultyone will run its task along with the task of the faulty cell. The area overhead is very small compared to the previouswork. The mapping problem becomes similar to the case ofhaving a spare cell between each two neighbor cells which isa reasonable organization for mapping.

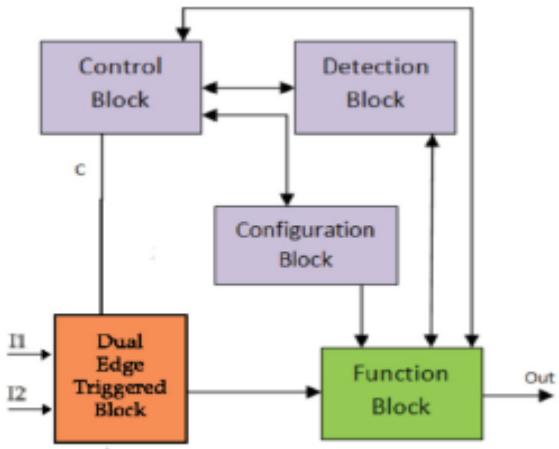


Fig. 2. Proposed cell structure

The operation of the proposed technique can be explainedas follows; when a fault is detected in a cell, the neighborcell will receive a control signal from controller to run thisfaulty cells task. The active cell divides run time between itstask and faulty cells task using a dual edge triggered"DET"cell. So, at the first half of the clock cycle with the positiveedge the active cell run its original task. In the second half ofthe clock cycle it runs the task of the faulty one. Fig. 2 showsthe cell structure of the proposed work. There are two inputsapplied to DET cell and selection of one of them depends onthe value of control signal (C) and clock (clk) value. When afault happens, the detection block detects fault location and thecontrol block pulls the signal C up for this specific location.Thus, the DET cell drives normal input (I1) when clk valuerises and selects input of faulty cell (I2) when clk value dropsas presented in Fig. 3.

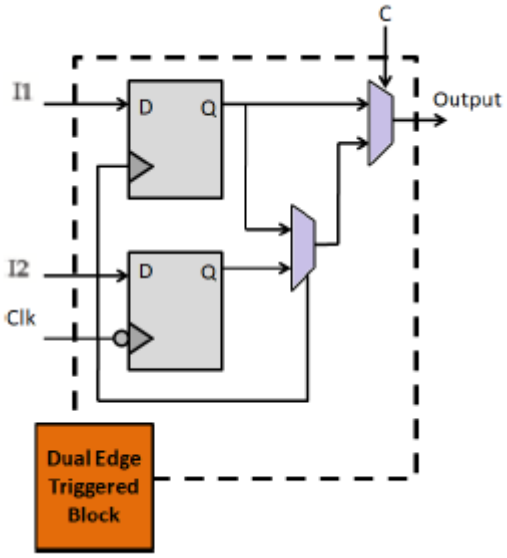


Fig. 3. Dual edge triggered circuits.

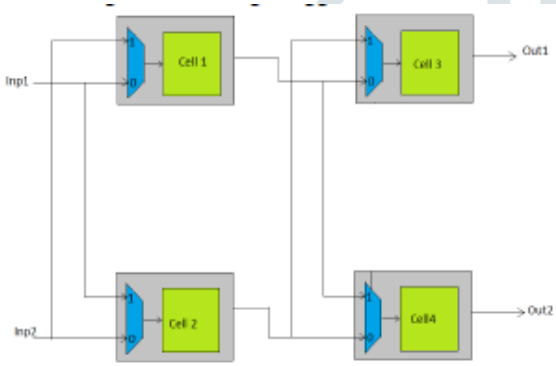


Fig. 4. Block diagram of the proposed technique.

Every cell is configured to perform only a specific function that is decided by the configuration information in each cell. When a cell fails the responsible module of self-diagnosis triggers self-healing and the faulty cell will be replace by the spare cell. Figure 1 shows general cellular structure, it is composed of six modules; I/O module, address module, configuration module, control module, function module, and detection module. The operation of each one is as follows; I/O module is used for transmission signals between different cells. Address module determines gene information from its coordinate of location information and determines the location of the cells. Configuration module stores the configuration information of all the cells which mimics DNA in biological cells. it also provides information for realization of self healing. Control module controls all operations of the cell such as fault case, transparent case, and idle case. Function module is the processing unit or the corresponding function which is determined by the configuration information. Detection module detects cell working status, if it is in a normal working condition or not. Self-healing is not only crucial for reliability but it's also one of the main aspects for an intelligent system.

Other self-healing approaches inspired from hardware intelligence paradigms include evolvable hardware, where a system can be evolved from an initial operating point with errors or low fitness until it finds a way around faulty cells through rearranging cells with genetic programming. Another mechanism can be considered where an online synthesis process takes place allowing the system to find a new synthesized architecture whenever a fault is detected. Such systems rely on a similar uniform organization like FPGAs or Genetic Programming units.

Most of self healing approaches are based on redundancy by adding spare cells. When a failure happens, the faulty cells are replaced by the spare cells after detection of faults. Along with the mentioned area overhead and scalability, the mapping of spare cells may cause delay overhead after self-healing because the nearest spare cell is very far away from the faulty one. For improved mapping and system's performance, adding more spare cells will help but on the other side the area will be higher. The area overhead can be reduced by adding less spare cells. Less spare cells leads to major mapping challenges and more complex healing system with increasing number of faults over time and whole system failure or delays. The proposed approach provides self-healing without adding spare cells which overcome area overhead problems. The proposed approach treats each cell as a spare cell for its neighbour. Also, each cell can do its task and the task of the neighbour cell. The proposed technique is based on time division multiplexing for self-healing. Each cell will be capable to run two tasks within the same clock when a fault happens. One operation runs during the first half of the clock cycle and the second during the other half of the clock. If the fault detection module detects a fault then the neighbour of the faulty one will run its task along with the task of the faulty cell. The area overhead is very small compared to the previous work. The mapping problem becomes similar to the case of having a spare cell between each two neighbour cells which is a reasonable organization for mapping.

Fig. 4 shows a simple array to demonstrate the idea. Assumethere is a fault in cell 1, according to that the detection blockit sends a signal for the neighbors to check there activationand select one on them. Now cell2 will compensate the faultycell1 and control signal C1 will be one. Cell2 has two inputsapplied to DET's input, one comes from the normal input andthe second which is supposed to go the input of cell1. Theselection input of DET selects one input to enter the cell 2depending on the clock value. Cell2 has the operation of cell1 task such that when cell2 receives a control signal C1, thecell2 selects the operation of cell 1 from configuration moduleto be done. For the negative value of clock and whether C1equals 1 or 0 the DET block selects inp2 and runs a functionof cell 2. During the positive value of clock and C1 equals1, the DET selects inp1 and runs a function of cell 1. Also,the output of cell 2 during the process time of cell 1's task isfed to cell 3. The same will happen on any cell where typicalevery cell has the same set of functions to be configured. So,instead of adding spare cells and increase area overhead, theself-healing is done on the system using the active cells itself.

3. PROPOSED METHOD

The proposed architecture uses fault tolerant self healing architecture with embryonic reconfigurable hardware which

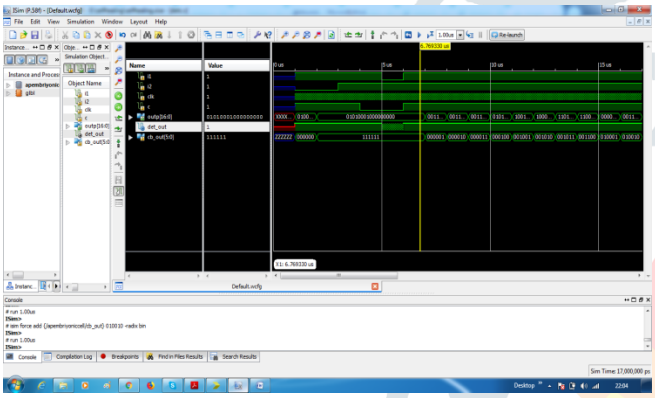
helps in reducing the drawbacks of author proposed approach. Also it uses the gate level fault tolerant techniques for each block of ALU Array. The proposed System may have Less Memory requirement, Optimal Area requirement, Less Delay or High Speed compare to existing methods

4. SIMULATION RESULTS

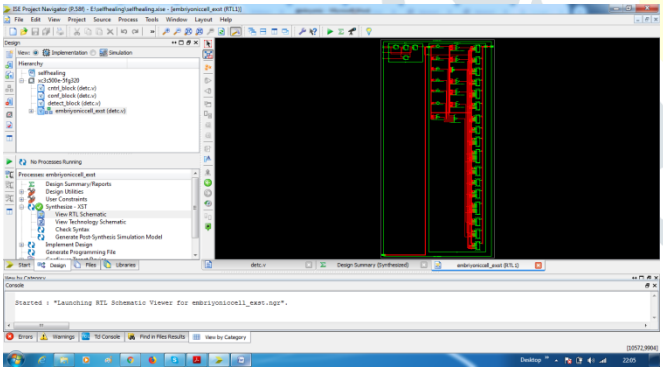
The designs are simulated by using ISIM Simulator for functional verification. The designs are modelled in Verilog HDL and are synthesized by using Xilinx ISE 14.5 Tool. The FPGA Device opted is XC3S500E with a speed grade of -5 and package of FG320.

A. Existing System

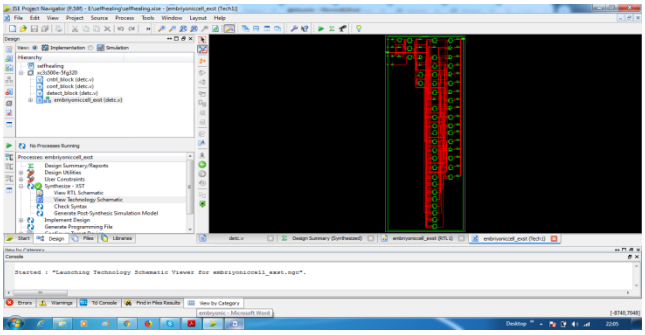
- *Simulation Result*



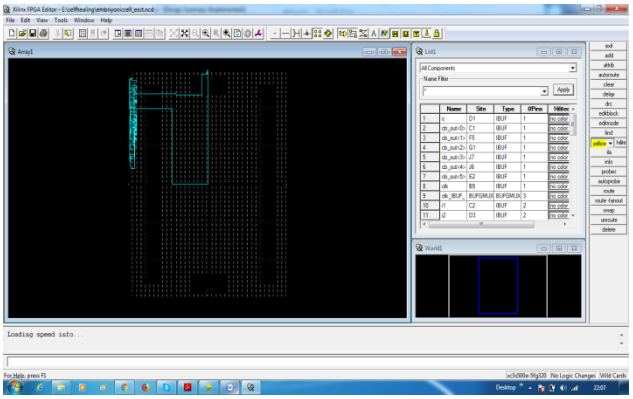
- *RTL Schematic*



- *Technology Schematic*

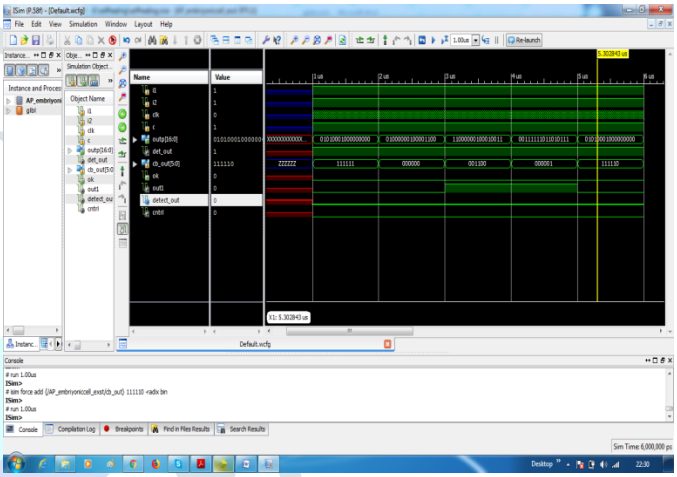


- *FPGA Implementation*

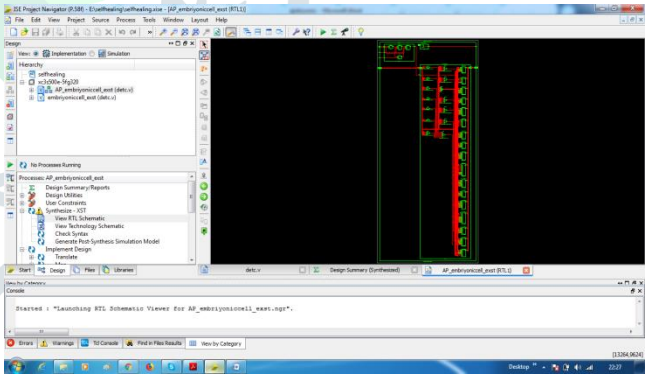


B. Author Proposed Design

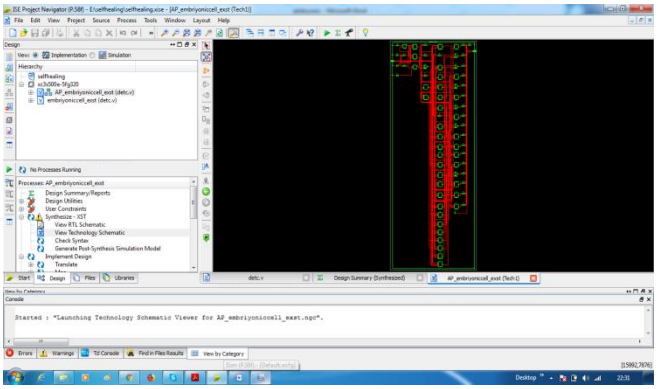
- *Simulation Result*



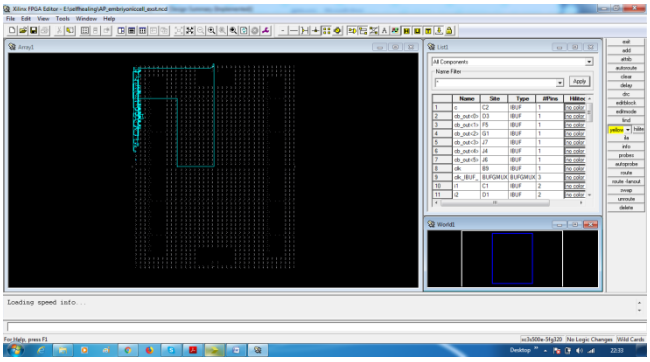
- *RTL Schematic*

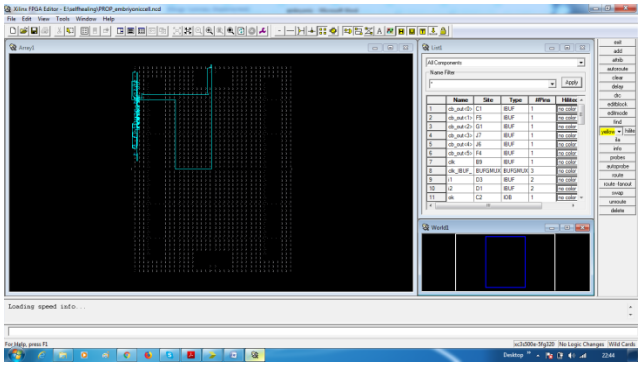


- *Technology Schematic*



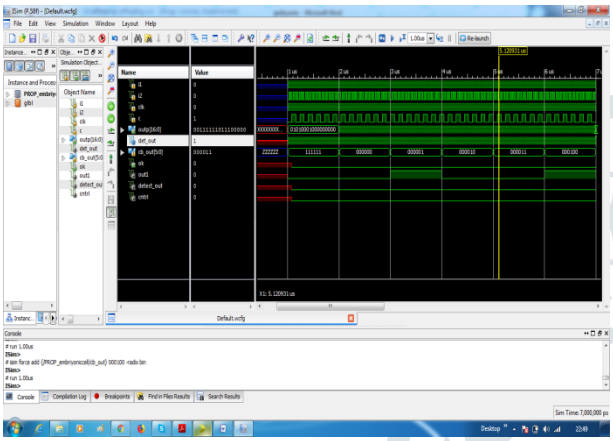
- *FPGA Implementation*



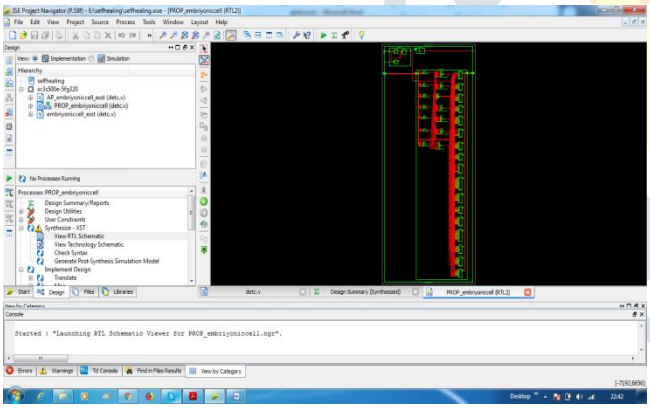


C. *Proposed Method*

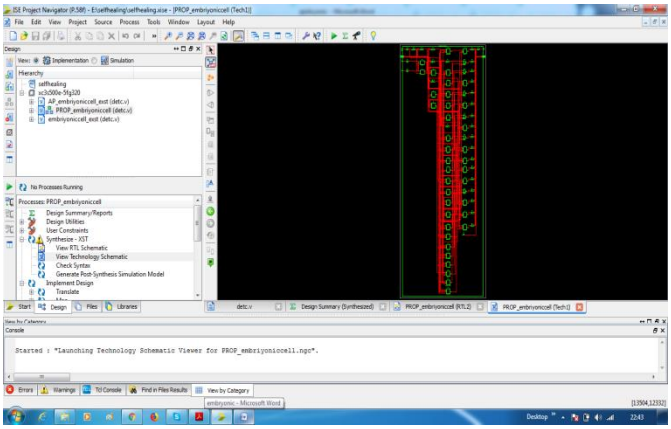
- *Simulation Result*



- *RTL Schematic*



- *Technology Schematic*



- *FPGA Implementation*

D. *Comparison Table*

Parameters	Existing Design	Author Proposed Design	Proposed Design
Number of Slices	20 out of 4656	20 out of 4656	20 out of 4656
Number of 4-input LUTs	37 out of 9312	37 out of 9312	36 out of 9312
Combinational Path Delay	9.252ns	9.252ns	8.974ns
Logic Power	0.00002	0.00003	0.00002
Signal Data Power	0.00003	0.00006	0.00003
I/O Power	0.00397	0.01018	0.00355

From the comparison table, it is clear that the power is increased by 61% in author proposed design when compared to existing design. The power and delay are reduced by 10.5% and 3% respectively in proposed design when compared to existing design and 65% and 3% respectively when compared to author proposed design.

5. CONCLUSION

The proposed architecture uses fault tolerant self healing architecture with embryonic reconfigurable hardware which helps in reducing the drawbacks of author proposed approach. Also it uses the gate level fault tolerant techniques for each block of ALU Array. The designs are synthesized by using Xilinx ISE 14.5 Tools and are functionally verified by using ISIM Simulation tool. The that the power is increased by 61% in author proposed design when compared to existing design. The power and delay are reduced by 10.5% and 3% respectively in proposed design when compared to existing design and 65% and 3% respectively when compared to author proposed design.

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