IMPLEMENTATION OF OPTIMIZED CARRY LOOK AHEAD ADDER USING CADENCE

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Abstract: In this paper, a discussion is done about 4-bit carry look ahead adder implementation with two different designs. The first design is Conventional carry look ahead adder (CLA) and second design is sketched using CLA equation it is called as carry chain structure. In first design of CLA, number of transistor count is more which increases power consumption and delay and in proposed design we reduce the transistor count. Schematic of two designs are implemented in cadence virtuoso tool in 180nm technology with 1.8V supply voltage and run the simulation. Two designs are compared based on their transistor count, power, and delay factors.

Index terms- Carry Look Ahead Adder (CLA), Carry Chain equation, low power, Cadence Virtuoso tool.

I. Introduction:

Carry look ahead adder is an electronic adder also called as fast adder, it is used in digital logic. For an integrated circuit design, the performance and other parameters are important for designing. The RAP-CLA is sketched by doing certain modification to carry look ahead adder to increase the efficiency (Omid Akbari). As technology is advanced it is implemented in different tool to improve the efficiency.

In devices like mobile, digital signal processing system it needs high performance less area and less power consumption and calculation must be fast. In arithmetic logical unit, adders are important block and perform different operations. The computation is done parallel by two independent carry chains for carriers of the adder and it has limited carry chain length and is implemented in multioutput of domino cmos logic, the operating speed is enhanced when compared to corresponding adders (C. Efstathiou).

To implement CLA with the help of carry synchronous section, it uses the idea of section carry to enhance the performance of CLA. It design the structure in three ways and improve the speed of operation (K.Preethi).

In carry look ahead adder the number of transistor used is more and circuit is little complex to build. In carry chain equation structure, reduce the transistor count by designing the model with carry equation of CLA.

II. CONVENTIONAL CARRY LOOK AHEAD ADDER:

A carry look ahead adder uses the idea of propagating and generating a carry bits during the addition operation. In two cases, the carry will be generated i.e., when two the inputs are high and when all inputs are high, output carry will be high. In this design full adder and other gates are used.

To calculate carry bits the amount of time it needs is less and improves the speed of operation when compared to ripple carry adder.
III. STRUCTURE OF CLA AND CARRY CHAIN:

CONVENTIONAL CARRY LOOK AHEAD ADDER

The carry propagation process is decomposed into subgroups of two bits \((G_i \text{ or } U_i)\) and \((P_i \text{ or } L_i)\) denotes generate and propagate functions,

Carry generation equation
\[ U_i = A_i \cdot B_i \]

Carry propagation equation
\[ L_i = A_i + B_i \]

The output carry of of last adder or \(i^{th}\) adder
\[ C_i = U_i + L_i \cdot C_{in} \]

Schematic of carry chain structure

The new modified CLA is based on carry equation and is designed using nmos and pmos transistor in cadence virtuoso tool with 180nm technology. The carry equations are denoted as \(C_0, C_1, C_2, C_3\).

\[ C_0 = U_0 + L_0 \cdot C_{in} \]
\[ C_1 = U_1 + L_1 \cdot C_0 = U_1 + L_1 + U_0 + L_1 \cdot L_0 \cdot C_{in} \]
\[ C_2 = U_2 + L_2 \cdot C_1 = U_2 + L_2 + U_1 + L_2 + U_0 + L_2 \cdot L_1 \cdot L_0 \cdot C_{in} \]
\[ C_3 = U_3 + L_3 \cdot C_2 = U_3 + L_3 + U_2 + L_3 + L_2 + U_1 + L_3 \cdot L_2 + L_1 \cdot L_0 + U_0 + L_3 \cdot L_2 \cdot L_1 \cdot L_0 \cdot C_{in} \]

All the propagate signals are connected in series with input carry and placed parallel to the previous signal in pull down network, in pull down network nmos transistors are present and to contrast nmos, the pull up network is designed using pmos transistor. In this structure, fifteen pmos and nmos transistor are used and an inverter is placed at output. The pmos is on or active when low input is given to it and nmos is in off, when high input is given to nmos, it is in on condition.
By using final carry equation of 4 bit carry look ahead adder, the circuit is designed and schematic view is shown in figure 2.

**IV. FLOW CHART**

The flow chart explain the procedure that will be followed to build the circuit in cadence virtuoso tool. In this tool the circuit is built in three different technology such as 180nm, 90 nm and 45nm. Here the circuit designed using transistors and convert them to block or symbol, before starting the design respective libraries need to be attached.

Once the circuit design is completed click on check and save and select ADEL to run the simulation. In this tool it determine different factors like transient response, DC, AC, Power, delay etc. few steps are followed to calculate power and delay and graphs will be displayed.
V. SIMULATION RESULTS:

Figure 3: output waveform of carry look ahead adder
The figure 4 shows output waveform of carry chain structure, consider three inputs generating and propagating signals and carry in, take the inputs bits as 1100,1100 and carry in as 0 then output carry is 1.

Table 1: Comparison of 4-bit CLA

<table>
<thead>
<tr>
<th>Design</th>
<th>Transistor count</th>
<th>DC power</th>
<th>Delay</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional CLA</td>
<td>276</td>
<td>3.74 uW</td>
<td>5.5 ps</td>
</tr>
<tr>
<td>Carry chain structure</td>
<td>32</td>
<td>170 uW</td>
<td>5.2 ps</td>
</tr>
</tbody>
</table>

To sketch the carry look ahead adder full adder and other logic gates are used, implementation is done the with nmos and pmos transistor total number of transistor used is 276, to design the carry chain structure 32 transistors are required, it occupy less area when compared to carry look ahead adder and less power is used. By supplying 1.8v to the circuit, run the simulation in cadence virtuoso tool. Comparison is done based on parameters such as delay and power.

VI. CONCLUSION:

In this paper, a circuit designed that use less area, power and reduce the delay factor such circuits are used in IC design to increase the efficiency and enhance the performance. Further designing the circuits for higher number and that can be used in digital signal processing system and other devices were computation must be done faster.

REFERENCES


