

Low-Power 18-Transistor True Single-Phase Clocking Flip-Flop Design Based on Logic Structure Reduction Schemes

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Abstract: In any design of digital circuit, the one of the most common & Important building blocks is Flip Flops. Power, performance, area are the factors that affecting the design. Efficient design must be optimized by three parameters. In a time constrained design the focus is on the optimization of power and performance. PPA (Power Performance Area) factors can be optimized by many techniques. In this paper low power 18-Transistor true single-phase clocking FF design is proposed. Master-Slave configuration is used to design the FF. It is designed using dynamic CMOS and complementary pass transistors logic. The FF is designed to reduce dynamic power consumption by avoiding floating internal nodes. The microwind and DSCH software is used for the implementation of the Flip Flop with supply voltage VDD of 1V and clock frequency of 500MHz. The FF design is implementing on 50nm technology. The results of the power dissipation and the delay is compared with 19-TSPC Results of the proposed design was found that it is more efficient than the other compared FF designs. In comparison with TSPC, the PDP improvement of the proposed design was 68% and 73% in overall and clock dynamic power, respectively, and 27% lower leakage.

KeyWords- Flip-Flops, True single phase clocking, Low structure reduction scheme, high speed, Microwind, DSCH.

I. INTRODUCTION

In very large-scale integration (VLSI) design, the latest updation in mobile battery-powered devices like personal digital assistants (PDAs) and mobile phones set new target. These goals consist the demand for high-speed digital circuits with low-power consumption. In any clocking system flip-flops and latches are the timing elements which is responsible for low power consumption & improved Latency in addition to the building blocks, become the most important components in synchronous VLSI system .

A flip-flop or latch is a electronic circuit which can be used to store digital information – a bitable multivibrator. The circuit can be formed to change state by applying signals to one or more control inputs and getting one or two outputs. Flip-flops are the basic unit for making digital models. Each flip flop consist the storage of one bit, that is a combinational model processes and the working at a given clock frequency will be synchronized. Flip flop is either positive edge triggered or negative edge triggered which signify that the input possess the output when the clock start from higher-to-lower or lower-to-higher logic, respectively. Flip flops have two types on the basis of data storing. Single-edge-triggered flip flops can be defined as the flip – flop which stores the data in either positive edge or negative edge of clock signal. Dual-edge-triggered flip-flops are the flip-flop which stores the data on both of the positive & negative edge of the clock signal. A flip-flop has two states in which one state represents a "one" and the other represents a "zero". Flip-flop used in a finite-state machine, in which the next state & the output not only depend on its current input, but also on its current state. Flip-Flop can also used for pulses counting & synchronizing variable timed input. Digital designs mostly adopt intensive pipelining techniques and assign many FF-rich modules such as first in first out (FIFO), shift register, and register file and shift register. It is also ejective that the power consumption of the clock system is as high as 50% of the power of total system which concurs of networks of clock distribution and storage elements. FFs thus allow a considerable portion of the area of chip and power consumption to the design of overall system.

Various techniques as well several flip-flops have been introduced recently to reduce redundancy in clock scheme/ system. There are various flip-flops given in the literature. Several digital and computational circuits use pulsed-triggered flip-flops either single or dual and master-slave.

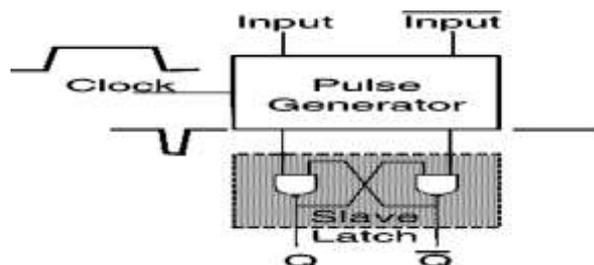


Fig 1: General structure of a flip-flop.

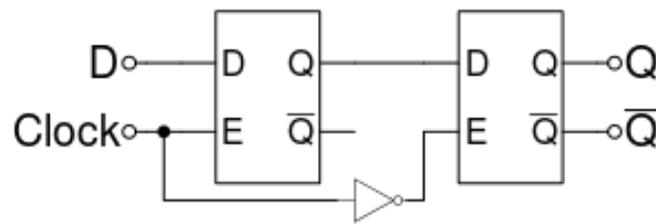


Fig 2: Master-slave edge-triggered D flip-flop block diagram

A master-slave D flip-flop. Its response on the falling edge of the enable input (usually a clock). An execution of a master-slave D flip-flop is triggered by the rising edge of the clock. A master-slave D flip-flop is formed by connecting two gated D flip-flops / latches in series, and changing the enabled input to one of them. It is known as master-slave because the second latch in the series inverts only in response to a change in the latch of first (master).

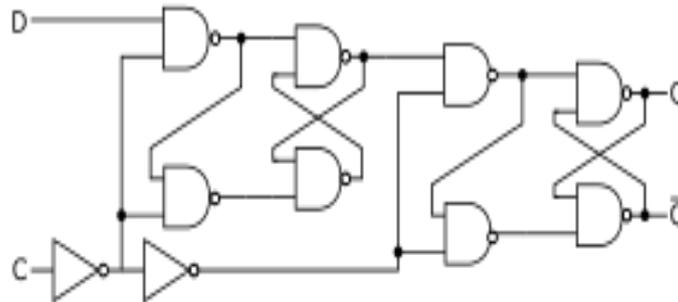


Fig 3: Master-slave edge-triggered D flip-flop

In a positive-edge triggered master-slave D flip-flop, when there is low signal clock (logical 0) firstly we seen "enable" or "master" D latch (the inverted clock signal) is high (logical 1. when the clock signal transitions from low to high then it allows the "master" latch to store the input value. As the clock signal goes high from 0 to 1 the inverted "enable" of the first latch which goes low from 1 to 0 and the input's value of the master latch is "locked". Nearly at the same instant, the twice inverted "enable" of the second or "slave" D latch transitions from low(0) to high(1) with the clock signal. This allows the signal to capture the rising edge of the clock by the now "locked" master latch to pass through the "slave" latch. When the clock signal returns to low from 1 to 0, the output is "locked", at the last rising edge of the clock the value seen is held while the "master" latch start to receive new values in preparation for the upcoming rising clock edge.

Master-slave and pulse-triggered flip-flops are used by several contemporary microprocessors. Traditional master-slave flip-flops are formed up of two stages, one master & one slave and they are Traditional master-slave flip-flops are made up of two stages, one master and one slave and they are represented by their hard-edge property. There are few Examples of master-slave flip-flops which include the transmission gate based POWERPC 603, push-pull D-type-flip-flop (DFF), and true single phase clocked (TSPC) flip-flop. Another edge-triggered flip-flop is the sense amplifier based flip-flop (SAFF).

1.1 Timing parameters

Setup time is defined as the minimum amount of time in which the data input should be kept steady before the clock event, so that the data is still sampled by the clock.

Hold time is defined as the minimum amount of time in which the data input should be kept steady after the clock event, so that the data is still sampled by the clock.

Aperture is defined as the sum of setup and hold time. The data input should be kept steady through this time period.^[28]

Recovery time is defined as the minimum amount of time the reset input or asynchronous set should be inert before the clock event, so that the data is still sampled by the clock. The time of recovery for the reset input or asynchronous set is thus common to the setup time for the data input.

Removal time is defined as the minimum amount of time the reset input or asynchronous set should be inert after the clock event, so that the data is still sampled by the clock. The time of removal for the reset input or asynchronous set is thus common to the hold time for the data input.

1.2 Metastability

Metastability is the basic problem which occurs in flip-flops, when two inputs, such as clock and reset or data and clock are changing at about the same time. When the order is not completed, within estimated timing constraints, the outcome is that the output may react unexpected, taking longer time than normal to reside to one state or the other, or even oscillating many times before residing.

Latches, timing elements and flip-flops, are delicate for the execution of digital systems because of the hard timing constraints and need for low power The most commonly schemes are single-phase and two-phase clocking. In this paper TSPC flip flop is proposed.

1.3 TSPC FLIP FLOP

The true-single-phase clocking (TSPC) flip-flops has been considered to be an accomplished methodology to obtain very high-speed digital VLSI design. The advantage of TSPC latches are less clock routing area, single-clock distribution, high speed and

no clock skew. In addition, a clock signal is defined as a global signal that must grow through the whole clock network before getting a transistor. Thus, the clock network must be possibly simple, and there should be minimum number of transistors controlled by the clock signal. By using this idea, we introduced a positive level-sensitive latch that uses a two-stage non-recharged version of the TSPC, and on other hand, a simple dynamic pulse generator is also designed for illation with the latch to establish a low-power high-performance. True single-phase clocking (TSPC) FF designs have been improved with the aim of reducing the load of clock signal. This is usually brought through circuit simplification. This design obeys the principle of TSPC operations to decrease the load of clock signal. TSPC is also secured and takes less clock signal routing area, one of the primary needs of a flip-flop for besides short latency, high speed digital design. True single-phase clocking (TSPC) is considered as the family of static and dynamic latches with such characteristics. The implementation of edge-triggered flip-flops is obtained by combining TSPC latches in several different ways. In this paper we improve the latency of TSPC. A way to reduce latency is to clock a single transparent latch with a very narrow pulse, as illustrated in Fig

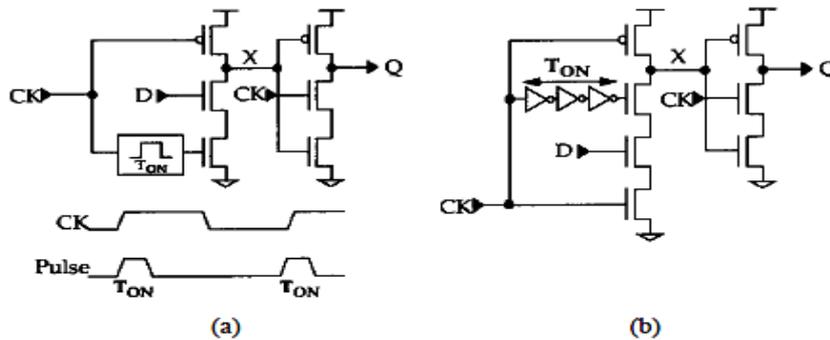


Fig 4: Single-phase pulsed flip-flop: (a) Concept (b) Possible Implementation

II. LITERATURE BACKGROUND

Compared appropriate FF. Fig 5 shows the Transmission Gate FF (TGFF) in master-slave configurations. It was applied using 24 transistors. The advantage of TGFF is using the number of transistors is less compared to FF designs concluded for the implementation applying CMOS logic. Applying the transmission gates is probabled in TGFF. The cons of TGFF are- i) TGFF consist of 12 transistors are clock driven due to this it has high capacitive loading due to high capacitive effect of loading the consumption of dynamic power is high even at low switch factor. ii) 2 clock phases required by TGFF which require extra circuitry to form 2 clock phases and the clock distribution strategy must be efficient to reduce clock jitter and skew issues. To conquer the cons of the using 2 phases of the clock, True Single Phase Clocking (TSPC) FF designs have been designed. In TSPC FF's only single-phase clock is used by both slave and master. This decreases the consumption of dynamic power and power need by the clock.

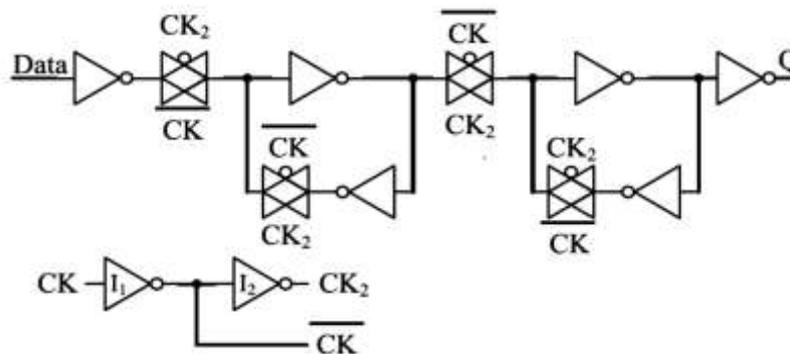


Fig 5: Transmission Gate FF (TGFF)

Fig 6 shows 11 transistor dynamic TSPC flip flop, whose Pros are- i) Single-phase of clock is used. ii) transistors need for the Flip-flop design is decrease to 11 thereby reducing consumption of power and area. Its cons are i) Increase dissipation of power due to floating nodes. Due to this, the circuit is subjected to noise. The drawbacks of dynamic TSPC FFs are conquer by

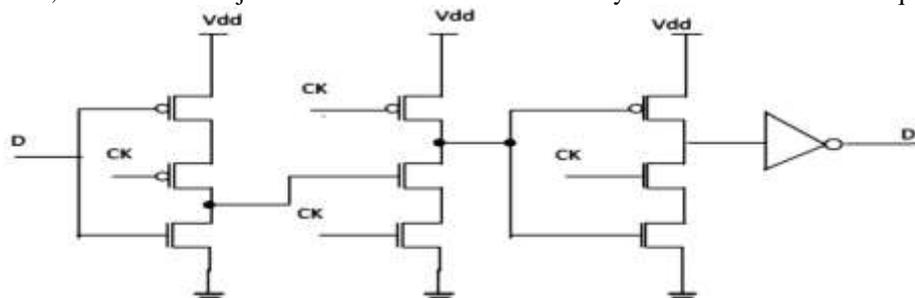


Fig 6: 11-Transistor dynamic Flip Flop

A static 21 transistor True Single Phase Clocking Flip-flop design with master-slave configuration called Topologically Compressed Flip-Flop (TCFF). The Pros of TCFF are Leakage power is decreased as the design has no floating. The cons of Topologically Compressed FF is increased time of setup due to feeble pull-up network in the design i.e. Two PMOS transistors only are connected directly to VDD and rest are connected to virtual VDD by applying method of topologically compression. The weak pull-up network consists of three transistors in series in the critical path. The setup time can be enhanced to getting results in the increased power consumption by raising the aspect size of PMOS transistors. An improve version of the TCFF called Logic structure reduction flip flop (LRFF) [1] was introduced by conquer the drawbacks of the TCFF .Fig 7 shows LRFF design acquired by reforming TCFF in logic structure reduction method 19-transistors applying. The advantages of LRFF are - i) Using single phase clock signal ii) To design FF needed number of transistors to reduce to 19 therefore lower power and area consumption. iii) setup time improves. iv) Reducing Leakage power the design has no motile. The drawbacks of LRFF In pipelining structure is as concise hold time which concretely lay a upper limit on the most propagation delay of the synthesis block.

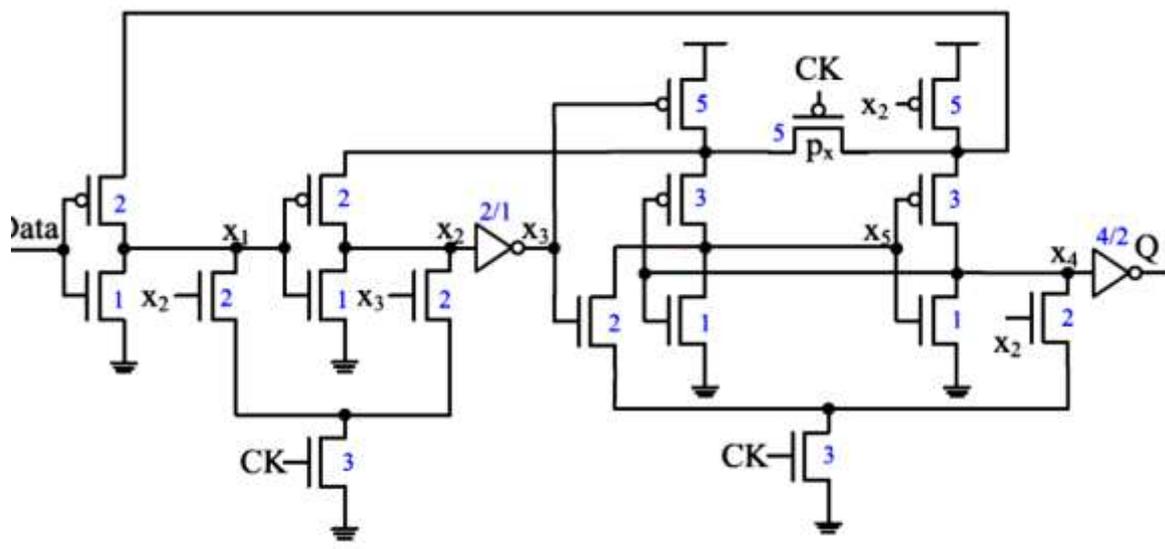


Fig 7: Topologically Compressed FF (TCFF)

III. PROPOSED TSPC FF DESIGN USING CIRCUIT SIMPLIFICATION METHOD

The proposed 18-Transistor TSPC FF design is acquired by renovating the 19-transistor LRFF. Logic structure optimization acquires the LRFF. The optimization is formed with regard to 2 parameters i.e. dynamic power and area.

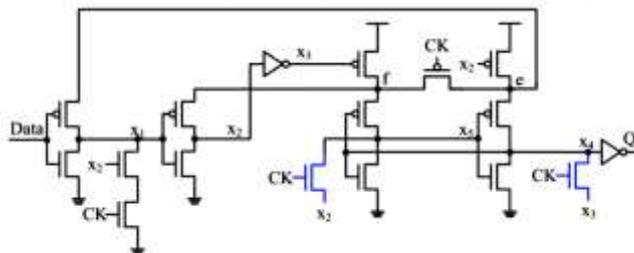


Fig 8: Logic structure Reduction FF (LRFF)[5]

3.1 Design

MOS circuit schematic of 19-Transistors TSPC Flip flop. MOS circuit schematic of proposed 18-Transistors TSPC FF. In LRFF there is two possible paths in which node t1 discharges to zero (as shown in Fig 9 which describes ON/OFF state of each transistor during process of data latching with dotted and solid view respectively) such as one is path A by N6 transistor as data is high. Other is path B connected N7 and N8 transistors BY the series when both node CK and T2 are high; if data is high that node t2 is high. When both CK and data are high so node t1 will liberate to zero by only path B .Therefore, as data is high and

3.2.3 18-transistor single-phase clocked (TSPCFF)

The purpose of TSPC FF designs is detracting the clock signal loading because; here the clock used only one phase. Cross-coupled set-reset latches were used in place of the Transmission gate based latch for peripheral single-phase-clock manipulation. TSPC is high-speed configuration which engrosses low power and employs less area. TSPC has several applications like, microprocessors, digital VLSI clocking system and buffers etc.



Figure 11: Proposed 18-transistor single-phase clocked (TSPCFF) and output-1

Figure 11 showing design of transistor single-phase clocked. AND gate, PMOS and CMOS component are using to design this circuit. To check result, when clk=1 d=1 then output=1.

Clk	D	Q	\bar{Q}
0	0	Q	\bar{Q}
0	1	Q	\bar{Q}
1	0	0	1
1	1	1	0

Table 1: Truth table of D flips flop TSPCFF

So in this case as again apply the high state in D and clock pulse then the output is also high. If the clock signal is low then output is also low. When the input of D is high and clock is low then the output is also high. On the other hand whatever signal state is applied in D, as same output is generate in the form of LED.

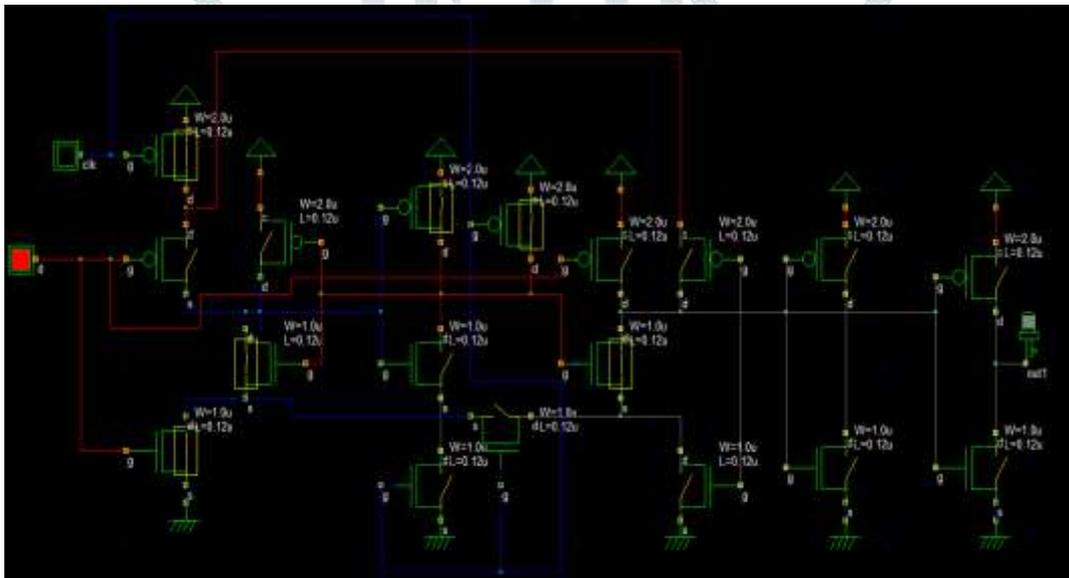
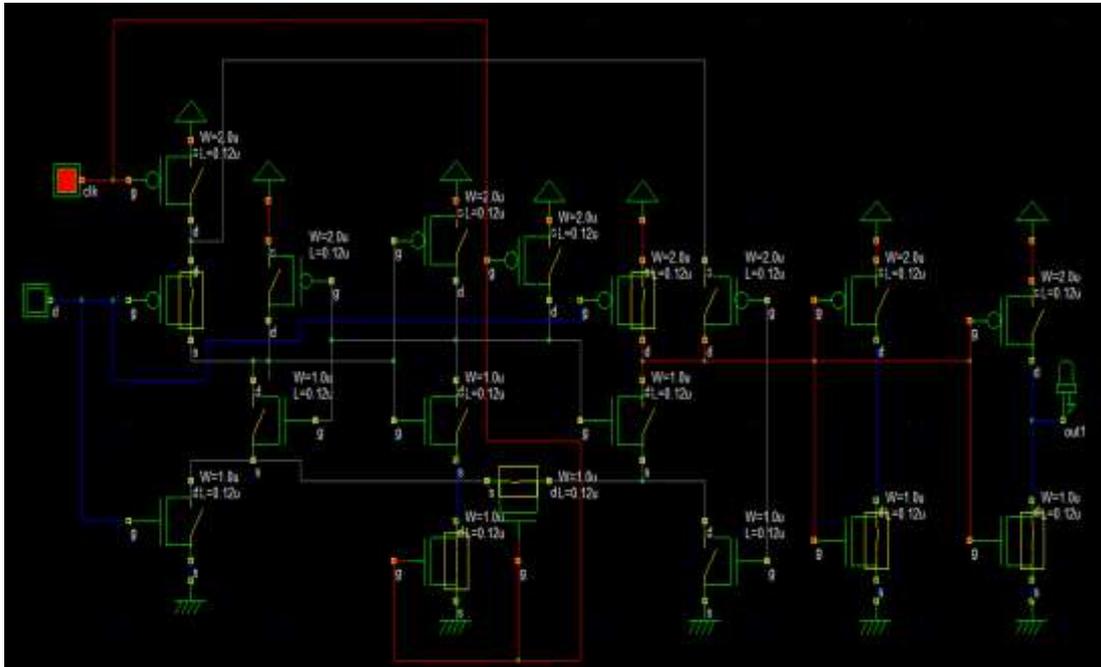
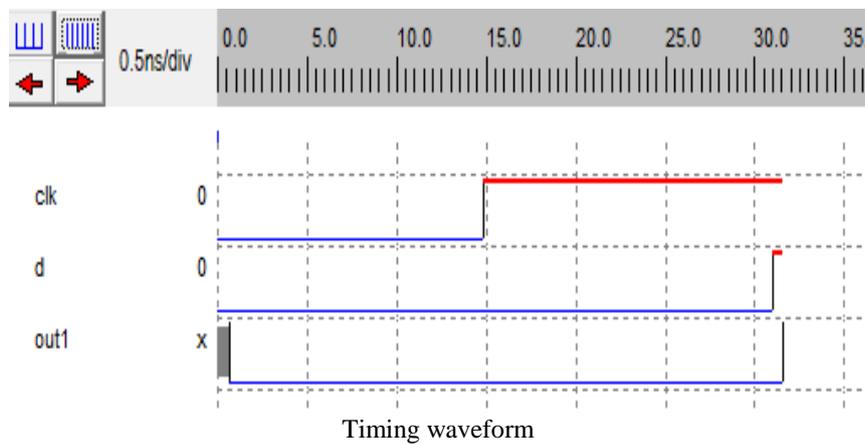


Figure 12: Proposed 18-TSPCFF and output-2

Figure 12 presenting, 18-TSPCFF when $clk=1$ $d=0$ and $out=0$, and when $clk=1$ $d=0$ then $output=0$.



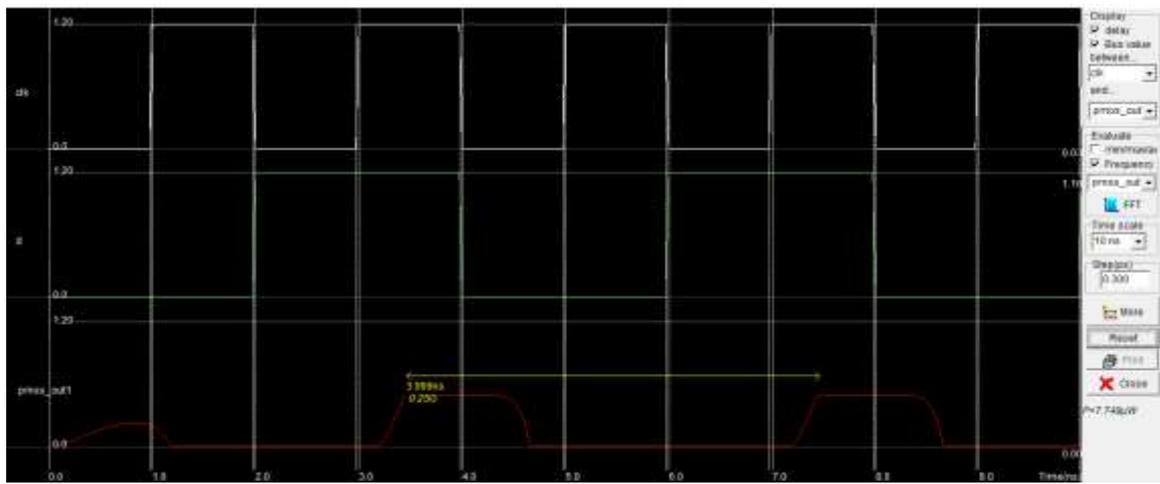


Figure 13: Voltage vs time of 18-TSPCFF

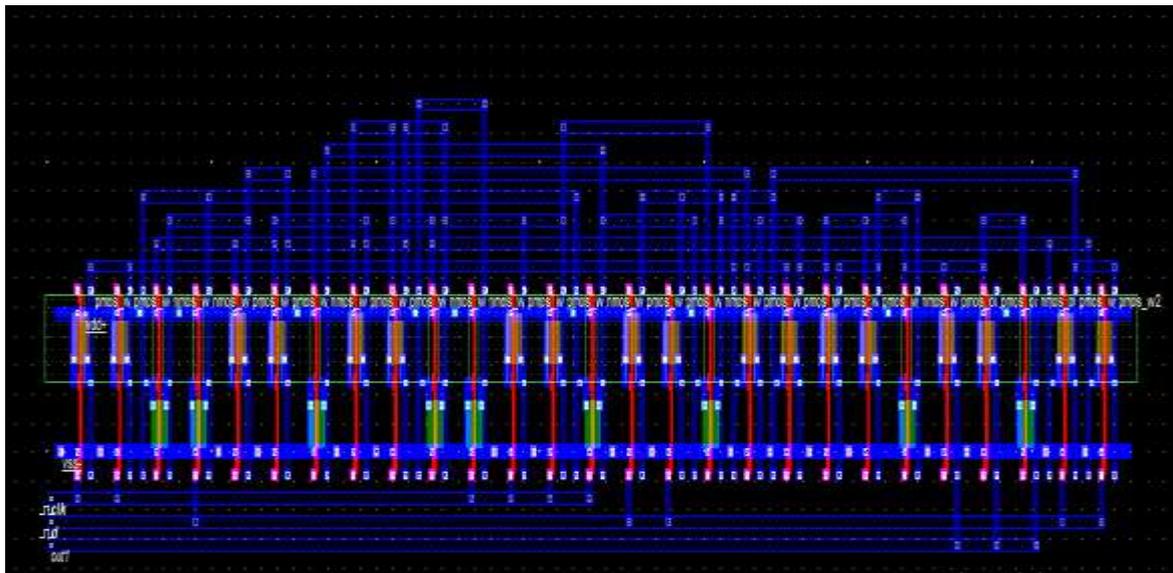


Figure 14: Layout of 18-TSPCFF

Sr No.	Parameters	Value
1	Area	374.0 μ m
2	Power	7.749 μ W
3	Delay	7ns
4	Power Delay Product (PDP)	542.43
5	Rise time	0.025ns
6	Fall time	0.025ns

Table 2: Simulation Parameter of 18-TSPCFF

S.N	Parameter	Existing Design	Proposed Design
1	Design	19-TSPC	18-TSPC
2	Technology	90 nm	50 nm
3	Topology	Gate level	Compressed Topology
4	Area (μm^2)	3265	374
5	Power(μW)	30	6.54
6	Delay (ns)	13.28	7
7	Setup Time(ns)	9.2	0.25
8	Hold Time(ns)	11	0.25

Table 3: Comparison of proposed designs result with previous designs

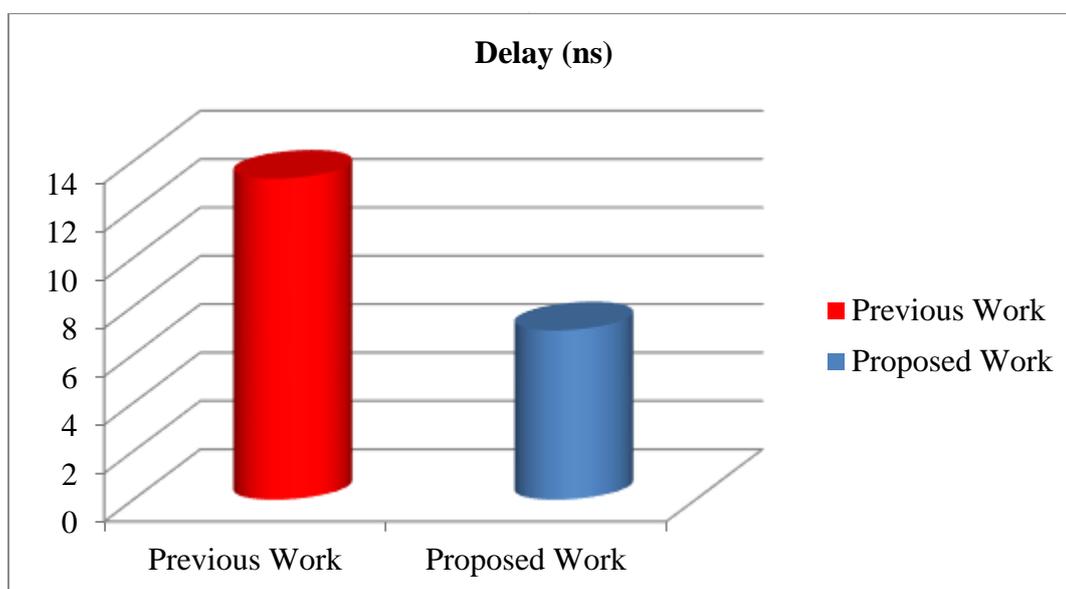


Figure 15: Delay plot of previous vs proposed design

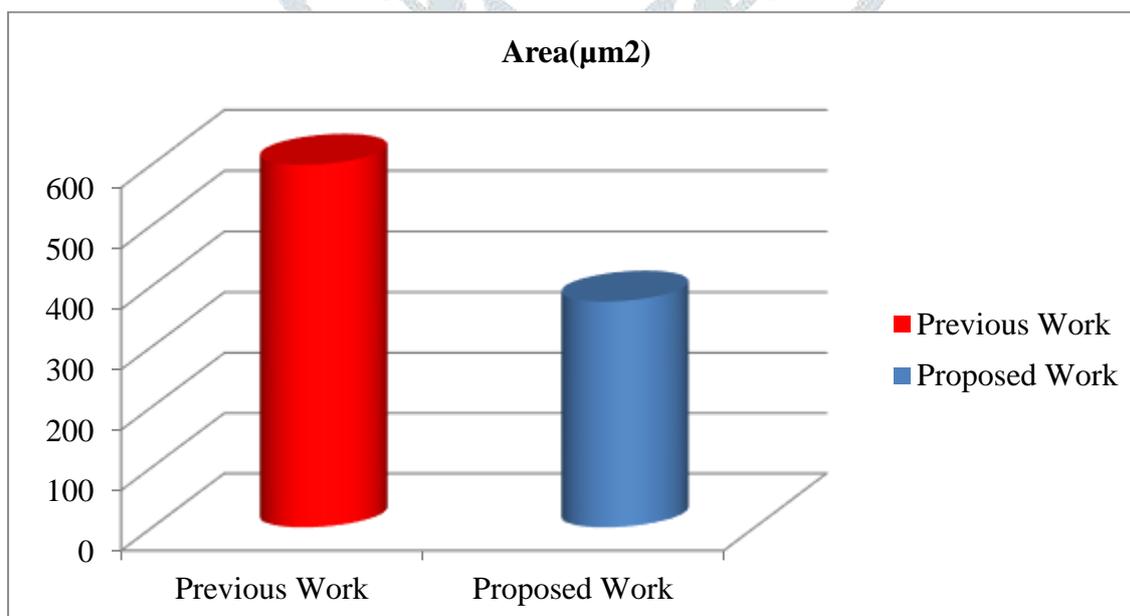


Figure 16: Area plot of previous vs proposed design

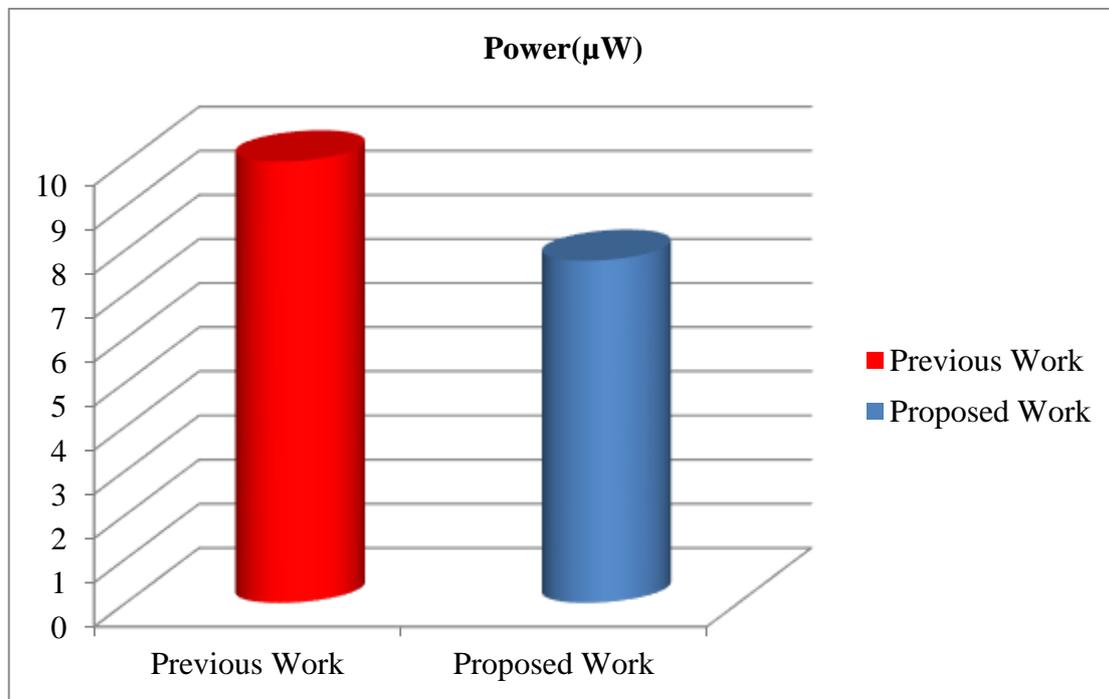


Figure 17: Power plot of previous vs proposed design

Therefore to see all simulated result and parameter values, it is observed that proposed design performance is better than Previous designs.

IV. CONCLUSION AND FUTURE SCOPE

In this paper, low power high speed 18-Transistor FF was designed, and its functionality was tested. The key idea was to solving these main issues are more look-up table (LUT), clock cycles ,consume high power, moderate throughput, more transmission time, low efficiency rate and more latency and improve the dynamic parameter by reduce transmission time ,power consumption and latency. Ambient simulations were conducted, and verified the functionality of the designs. The power delay product, average power consumption and delay was estimated and collated with apart designs. We also compute and compare the hold time and setup time with other designs. When compared with another designs, the introduced design was preferable in all the parameters.

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