Designing of low power MOSFET for amplification of Biomedical signal: A review

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Abstract- Biomedical signals play a vital role in the field of medical sciences and the information present in the signal is not easily extracted due to the low amplitude of the signals and the interference of noise. The device MOSFET has been introduced and it helped to some extent for the problem faced in cancellation of noise and the amplification of the signals, but there is still a room for improvement of the MOSFET. The MOSFET characteristics like output current, output voltage, gain and noise margin play a huge role in making the device useful. The MOSFET can also work efficiently with low frequency signals. Modeling of the MOSFET with suitable material can be accomplished to achieve the required outcomes after adjusting the designing it parameters. In this work the review of various MOSFET designs have been reviewed and this is required for knowing the shortcomings of the previously existing models and the requirement for the new models with some new specifications to overcome the problems that are present now and also that can occur in the near future.

Keywords **- MOSFET, 2D structural design, DGMOSFET, Visual TCAD, CMOS.**

INTRODUCTION

Biomedical signals are very important when it comes to any treatment for the human being and there are many signals present in human body generated by nerve cells and many other organs, like heart and brain generating ECG and EEG signals respectively. The understanding of these signals will help the medical personnel to give proper treatment. But the main problem lies in reading those signals.

The MOSFET is mainly used to do this amplification and the CMOS integrated circuits used are required to work with low power. The decreasing channel length of the MOSFETs limits the allowable voltage [1].

The Threshold voltage is the voltage required to turn the MOSFET 'ON', that means the drain current starts to flow only when the gate voltage reaches or exceeds the Threshold voltage (V_T). The threshold voltage depends on many factors out of which the oxide thickness, channel doping concentration, junction depth and channel length are important factors [9].

Generally the low voltage circuits are required as:

1. The threshold voltage of the devices is now being reduced to 2 Volts from 5 Volts, for the safety and reliability of the device.

2. In order to prevent the integrated circuit from overheating, as the IC should perform more functions than earlier ones.

3. For making the device portable which runs on battery which is a limited power supply, we should make the device consume very less power.

Now the MOSFETs scale lies in nanometer and it comes in many designs like Double Gate (DG) MOSFET, Dual Material Double Gate (DMDG) MOSFET.

Effect on the characteristics of MOSFET

Various factors can affect the characteristics of the MOSFET it can improve the device if it is used in a right way. The engineering techniques are applied in three different areas and they are: [8]

- Gate
    - Stack - By stacking the gate the leakage current can be reduced and E-field is also reduced.
    - Lateral - By lateral placement of gate the length modulation of channel is reduced.

- Channel
    - Pocket engineering - By this technique the V_{th} can be adjusted and depletion layer width is reduced at the junction.
    - Graded doping - This technique can be used to increase the drive current.
- Work
    - Changing of material - This study can be used to control the electric field at the drain region.

DEVICE STRUCTURE AND ANALYSIS

The double gate MOSFET has a very good control of the channel and it helps to attain higher current in the device.[3]

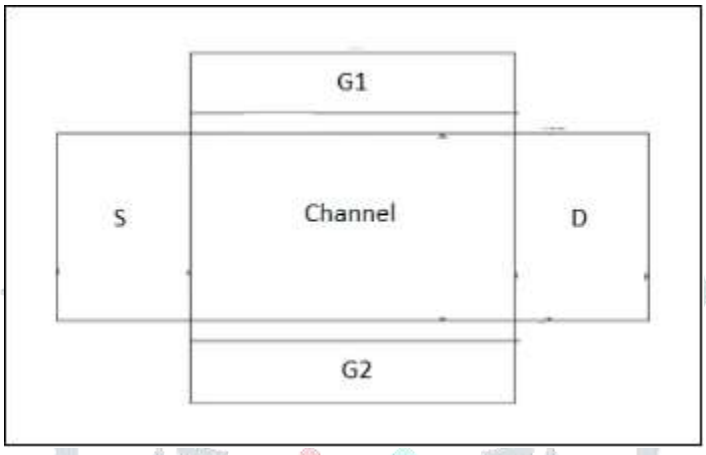

Fig 1. DG-MOSFET structure.

DGMOSFET can also be considered as an advanced form of normal MOSFET, both the gates can be shorted or can be used independently [4].

DG MOSFET are classified into two types namely

- Symmetric DGMOSFET
- Asymmetric DGMOSFET

Namrata et al.[5] in her work proposed “Heavily doped N+ pocket AJDGMOSFET”, which is an asymmetrical gate structure.

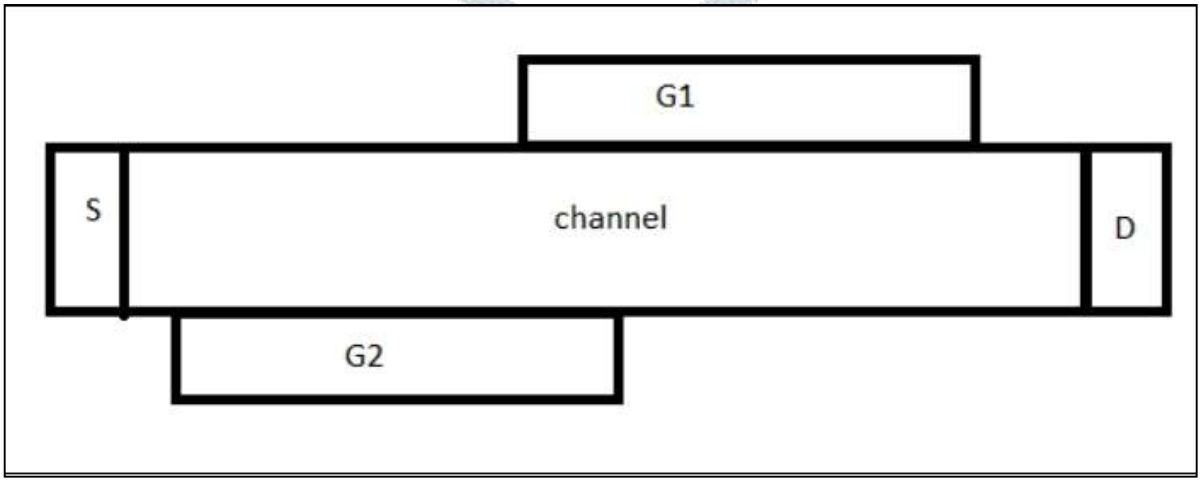

Fig 2. AJDGMOSFET.

Ajay et al, [6] in his work compared two different junctionless DGMOSFET with different underlap regions one device’s gate lies near Source end and another lies at the Drain end.

The model of 4 nm MOSFET device is proposed with HfO_2 as oxide and InGaAs as semiconductor material. The gate length is 4 nm and the channel length is taken as 21.6 nm and performed the analysis on them. Later a CMOS is also prepared using both pMOS and nMOS.

Fig 3. A 4 nm MOSFET schematic diagram

This CMOS is composed of two MOSFETs in which one is p-MOS and the other is n-MOS. The device is further used as an inverter and the data is mentioned in the paper[7].

This inverter is a basic gate which require both pMOS and nMOS and to test both of these devices the best way is to try the inverter which has one input and one output and which inverts the input signal.

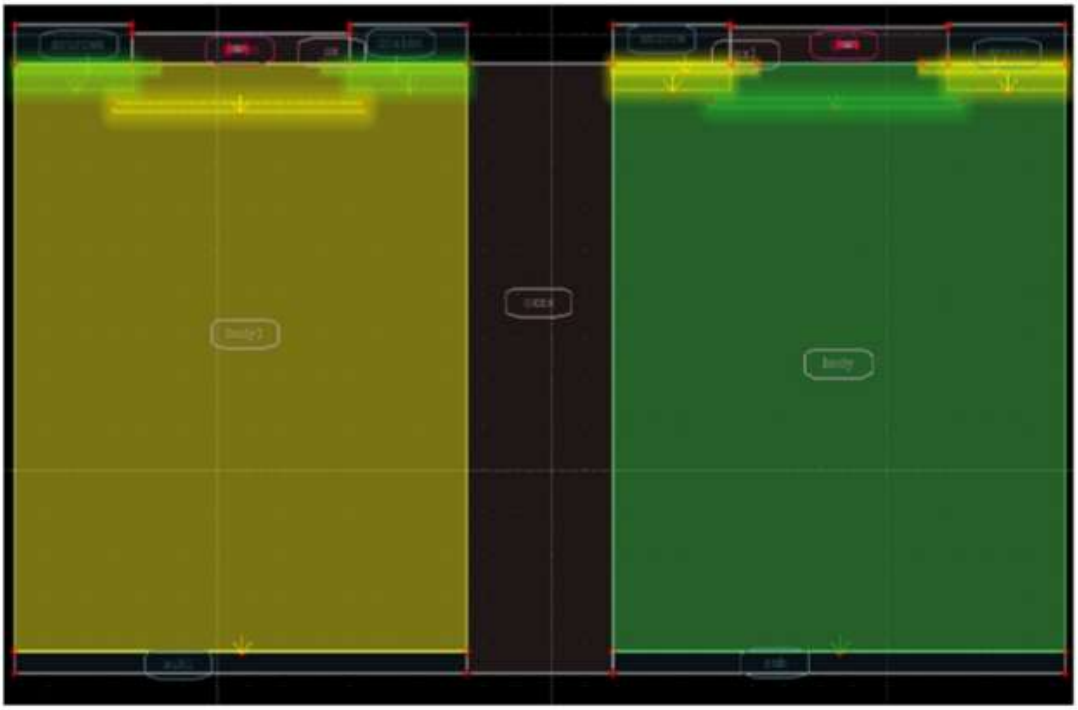

Fig 4. CMOS schematic.

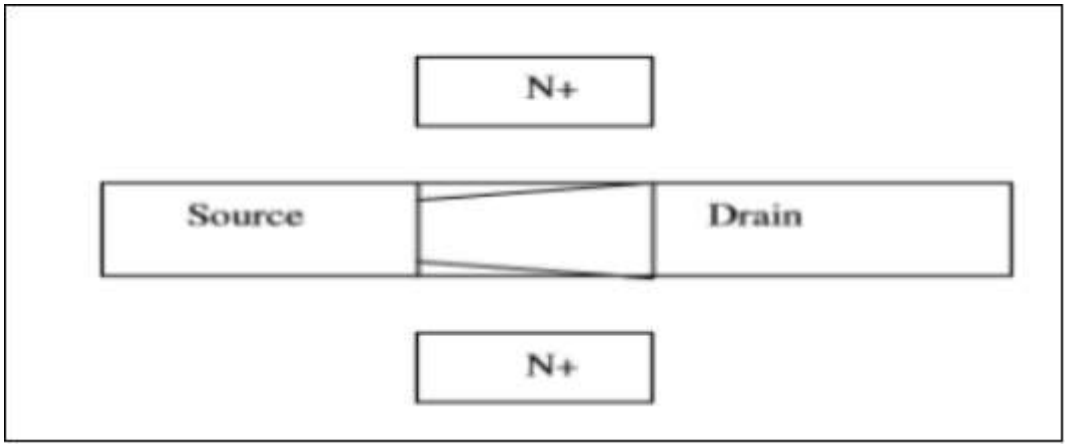

Fig 5. Symmetrical DG MOSFET.

The figure 5 shows the symmetrical Double Gate MOSFET in which the both gates can be shorted or given the same voltage and create the conducting channel in the substrate region.

The author created a 10 nm MOSFET model on the Visual TCAD and had done the mesh analysis and other performance tests and had plotted the results in his work [8]

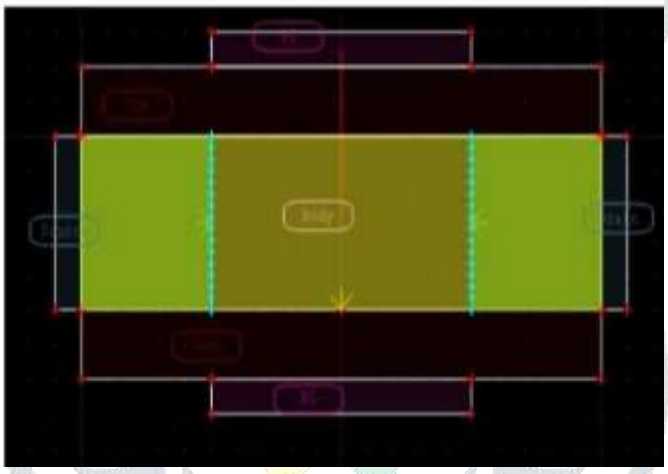

Fig 6. 10 nm double gate MOSFET.

DESIGNING OF DGMOSFET

In this work the designing of the double gate MOSFET has been done and the parameter of the design are :

Parameter	**Size**
Gate1 and 2 length	32nm
Channel length	38nm
Channel thickness	11nm
Oxide thickness	1nm
gate thickness	2nm

Table1 Dimensions of the device.

And the material used for the construction of DGMOSFET are:

Region	Material
Gate	NPolySi
Channel	Si
Channel doping	Acceptor $2*10^{15}$
Source/Drain doping	Donor $2*10^{21}$
Oxide	SiO_2

Table2 Type of material used.

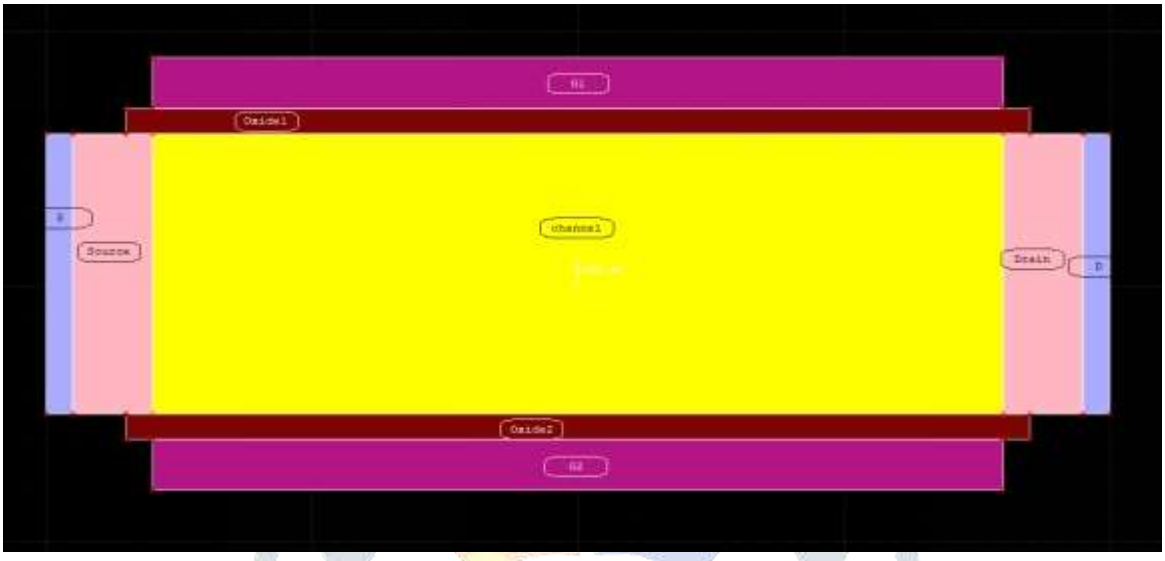

Fig 7- double gate MOSFET structure

RESULT AND DISCUSSION

The device with parameters channel thickness as 11nm, and channel length as 32nm have the results as followed V_T = 0.27V, I_{on} = $37*10^{-5}$A, I_{OFF} = $3.548*10^{-8}$A and the I_{ON}/I_{OFF} ratio as $1.05*10^4$ [3].

The 11nm CMOS deigned showed the improved threshold voltage that is 0.336V where as the previously existing was 0.232V the I_{OFF} current is decreased largely that means the leakage current is reduced from $77x10^{-8}$ to $20x10^{-10}$ this brings the increased value of the Ion/Ioff ratio of the device [7].

The Drain current vs Gate voltage graph of the DGMOSFET has been obtained for the design done in this work

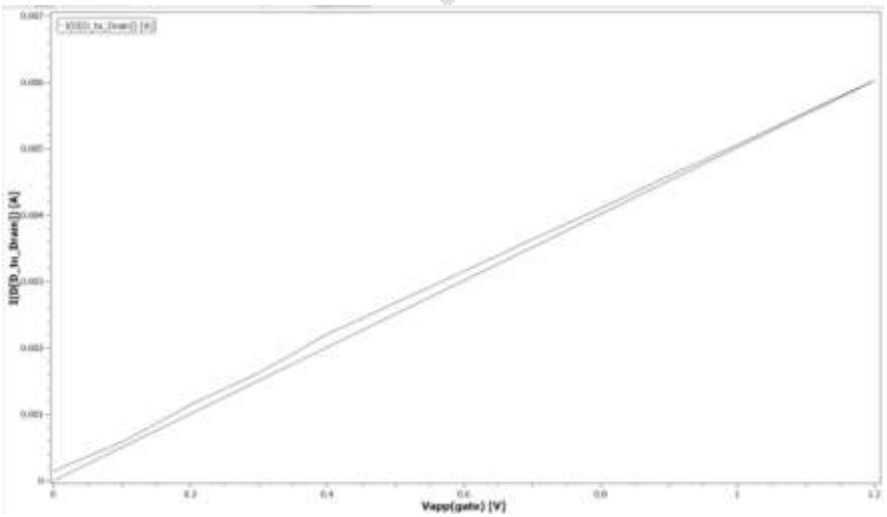

Fig 8- The drain current vs Gate voltage plot.

CONCLUSION

The DGMOSFET reduces the Drain Induced Barrier Lowering which gives good results of the Ion/Ioff ratio [3]. The N+ pocket AJDGMOSFET also have high Ion/Ioff ratio which is in order of 10^{13} [5].The 4 nm MOSFET designed with the InGaAs material had better performance when compared to conventional MOSFET in the characteristics like threshold voltage and some electrical behavior [7] the CMOS also performs an excellent job when used as an inverter.

The Drain Induced Barrier limiting (DIBL) is reduced and the leakage current is improved and this proves that the device dimension plays a crucial role in reducing short channel effects (SCE)

References

[1]- Sandhu, M. and Bala, M., 2012, January. Design of low voltage low power operational amplifier. In *2012 Second International Conference on Advanced Computing & Communication Technologies* (pp. 368-373). IEEE.

[2]- Buvaneswari, B. and Balamurugan, N.B., 2019. 2D analytical modeling and simulation of dual material DG MOSFET for biosensing application. *AEU-International Journal of Electronics and Communications*, *99*, pp.193-200.

[3]- Neetu, S.C. and Prasad, B., 2014. Simulation of Double Gate MOSFET at 32 nm Technology Node Using Visual TCAD TM Tool. *Advanced Research in Electrical and Electronic Engineering*, *1*(4), pp.9-13.

[4]- Hisamoto, D., Lee, W.C., Kedzierski, J., Takeuchi, H., Asano, K., Kuo, C., Anderson, E., King, T.J., Bokor, J. and Hu, C., 2000. FinFET-a self-aligned double-gate MOSFET scalable to 20 nm. *IEEE transactions on electron devices*, *47*(12), pp.2320-2325.

[5]- Mendiratta, N., Tripathi, S.L., Padmanaban, S. and Hossain, E., 2020. Design and Analysis of Heavily Doped n+ Pocket Asymmetrical Junction-Less Double Gate MOSFET for Biomedical Applications. *Applied Sciences*, *10*(7), p.2499.

[6]- Narang, R., Saxena, M. and Gupta, M., 2017. Modeling of gate underlap junctionless double gate MOSFET as bio-sensor. *Materials Science in Semiconductor Processing*, *71*, pp.240-251.

[7]- Chakraborty, R. and Mandal, J.K., 2018. Design of 4 nm MOSFET and its applications. *Microsystem Technologies*, pp.1-8.

[8]- Nitin Goyal , Nagendra Sah PG Scholar, Associate Professor, ECE Department, Punjab Engineering College, Chandigarh 2008. Review Article on Impact of Various Engineering on Double Gate MOSFET, International Journal of Electrical Electronics & Computer Science Engineering, Volume 5, Issue 2.

[9]- Zabeli, M., Caka, N., Limani, M. and Kabashi, Q., 2007, May. The impact of MOSFET's physical parameters on its threshold voltage. In *WSEAS Conference MINO* (Vol. 7, pp. 54-58).