Literature survey on Network on Chips

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Abstract

As the Present day SCOCs are becoming complex as it needs to incorporate large number of cores and peripherals within the single chip ,especially for the real time applications such as as deep learning, neural networks,AI chips,Robotics,bigdata applications,wireless,multimedia applications where parallel data processing takes place and also has to handle huge volume of traffic.The traditional bus based architectures fails here .This gave raise to a new on chip communication architecture called NOC(Network on chip) which is very much essential for designing the complex SOCs. Hence this paper is a survey of all the traditional and modern concepts involved in designing of a NOC. This paper is organised as Introduction, Challenges in NOC ,Topology, Emerging Topology, Routing,challenges in Routing,Emerging routing techniques and the Tools used in designing an NOC.

Keywords:SOC,NOC,Topology,Routing etc

Introduction

A Simple SOC consists of CPU ,instruction and data cache attatched to CPU and various peripherals such as DMA,LCD,BIU Instruction bus,CAN bus ,Instruction memory,datamemory etc In addition to these various slower peripherals such as WDT,Interruptcontroller,timer,real time clocks are logically interconnected around 20 peripherals and they communicate using the AMBA architecture .AMBA used with ARM processors and other

RISC 5 based processors.But modern SOC is complex with multiple bus

interface such as GPU,accelerators,graphic accelerators for sound processors error control code etc and peripherals numbers are increasing from 20 to 50 and further it keeps on increasing .So here the problem is hundreds of bus master talking to one bus and building such a system is complicated[4]. Such a system when converted from architectural level to the physical implementation in the process of synthesise, placement,and routing the tool tries to optimise area and wirelength blocks overlap each other, wiresgo around and the process becomes very bad and even the synthesis takes many days .Also for the smaller technology wire delay grows quadratically and current delivering capability of transistor reduces[5].

The transistor sizes are shrinking in the recent years ,and in the nano scale era there is a tremendous decrease in gate delay compare to the wire delay,also the complexity of components inside the SOC is increasing in this scenario the bus becomes narrow and in worst case it begins to block the traffic also bus based system cannot meet all the demands of an SOC [1] such as throughput, bandwidth,low latency, and reliable globalcommunicatio services performance, power, timing closure, scalability, small time to market ,high complexity and high performance[3] . Thus there is a need to look for a scalable communication architecture

W.Dallyproposed to change the way we look at the architectural specification itself, view the tiny blocks as routers/switches,and route packets instead of wires.This was the the idea behind an NOC. Interconnect is the heart of NOC architecture[2] Forthe present day complex applications which requires a structured and scalable architecture.NOC is the best choice..Thus making the communication inside the chip very important This also translates the complex SOC design from computation centric to communication centric. [2].

The above mentioned problems and performance parameters can be improved through the communication architecture called NOC[6].

Thus NOC is a scalable interconnection of various heterogeneous devices such as processors,embedded memories, application specific components ,mixed signal I/O cores which communicates each other by sending packetized data over the network [2].

The main characteristics associated with an NOC are Topology ,Routing algorithm, Switching strategy and Flow control. The main performance metrics are Bisection bandwidth and Flow control

CURRENT CHALLENGES IN NOC DESIGN

As large number of IP blocks are added to the chip the number of routes between cores grows by a squared ratio this increases the problem of congestion eliminating congestion has become one of the main challenges in NOC design[3] .As congestion increases the size of the die increases and more metal mask layers increases ,it also creates unpredictable paths and affects the timing closure.This poses a significant challenge to create a low cost and high performance chips[3].

Also as the technology shrinks the driving strength of the transistor reduces and signal propagation time is along the wire is growing ,this affects the speed of the chip.As the number of wires increases it increases the cost of the chip.

Apart from this the NOC designer faces Complex Multi-variable Problem,Large Design Space,Comfort around Simplistic Designs,Performance, Power and Area Tradeoffs,Buffer Sizing and Pipelines problems[2].

As the interconnect resources are very high and proves to be the bottle neck in performance, in order to handle huge traffic conditions NoC should support network level congestion control also ,buffering problems,channel width problemetc are increasing.NOC circuits should designed to overcome the difficulties and also should reduce the latency and increase the bandwidth[2].

Band width = fch*W

where fch is the frequency at which the channel operates To reduce latency channel width has to be increased.

Packet throughput= total packet completed *Packet length/(Number of IP blocks)*time

Apart from these the two other challenges for an NOC designers are in selecting the topology and Routing algorithms[6]

Network Topology

The network topology is the way how components are interconnected inside the chip. The traditional network topologies are mesh,torous,tree, butterfly,plygon,star etc.All these architectures were implemented as 2D ICs [7].

The proper selection of network topology improves some of the performance parameters such as network latency, throughput, area, fault tolerance and power consumption .

The above mentioned traditional topologies cannot meet the demands of the Present day applications such as hand held devices, Digital processors,G raphic accelerators,2D/3D video accelerators, digital cameras and also in the real world application domains such as deep learning, neural networks,AI chips,Robotics,bigdata applications,wireless ,multimedia applications ,image processing,pattern recognition ,cloud computing where massive data processing with high data parallelism with lesser power consumptions are required[7] .

These applications needs a complex SOC in which the number of cores and peripherals are increasing in larger. Also these traditional topologies cannot handle the high volume of traffic which is generated. This leads to the slow down of the overall performance of SOC . NOC channel width should be increased to handle high volume of traffic which leads to NOC power dissipation .Hence a high radix NOCs architectures with intelligent routing schemes which minimises the latency,congestion and energy consumption of NOC need to be implemented This gave rise to emerging NOC architectures [8]-[10].

Emerging NOC architectures

Emerging NOC architectures mainly sees how to route packets from one end to another end in a huge SOC by reducing the diameter of the network. Large scale research works are going on in the these Emerging NOC architectures which are as follows

- Multidrop links

In this architecture there are links where signal reaches multiple routers in same clock cycle.

In this architecture the diameter of the network gets reduced thus eliminating the need of high radix routers and thus improves the network latency.

These links can be built and also can be broken by sending bypass signals towards the destination

- Three Dimensional NOC

The number of cores are increasing at an exponential rate inside the chip ,the 2D ICs performance is getting lowered,there are also restrictions for the floor planning choices and the 2D ICs have larger die size in multiprocessor based applications also there are several difficulties associated with clock distributions. This gave rise to the 3D architectures[11].In a 3D NOC, a Vertical interconnection of multiple 2D layer one over the other with Near field coupling schemes where no physical connection between the layers through inductive and capacitive coupling to communicate to upper layers without physical connections .3D NOC increases the system performance and mainly used in real time and aerospace applications. There are several challenges in designing a 3D ICs[11]-[12] .

- RF interconnects

These are alternative to the VI signalling through the metallic wires. Here there are microchip transmission lines on the metal layers of the chip and the signals that need to be transmitted are first modulated using the carrier wave with very high frequency in Ghz range.These electromagnetic waves are then guided through the Transmission lines.

Nano Photonic NOC or Fibre optic NOC

In this technology the photonic devices and the properties of optical medium are used. On such technology is the Microring resonator Technology in which light of certain wavelength is diverted when an voltage is applied.

Wireless NOC

A wireless NOC has wireless access points which has wireless transmissizon capacity this is used for long distance communication within the chip .There are different wireless architectures such as Ultra Wide band NOC, mm wave wireless NOC, RF-waveguide wireless NOC. The major advantages of using wireless NOC are in Dead lock free Routing,l ow Latency,Multicasting ,Broad casting etc[17]-[18].

Routing

Depending on the routing algorithm used the routers will route the packets to their respective destination..The two main problems associated with Routing are Implementation complexity and performance .Apart from these the realistic traffic patterns are very different compared to the models and also should handle prescheduled and dynamic traffic. The following are the challenges faced in selecting the routing algorithm[13]- [14].

Challenges in Routing

Deadlock free Routing ,Live Lock free routing,Starvation,network flow control etc.

Dead Lock is a situation where two or more packets are waiting to get each others resources to route farward also the routers are not able to provide the resources until they get a new resource This makes the routing to get blocked Present day applications which needs to handle huge traffic and hence the possibility occurring of dead lock is more. Thus routing algorithms for present day applications should be designed so as to overcome this situation.

LiveLock is a situation where packets will never be able to reach its destination.

Starvation is a situation where all the available resources are always taken by the high priority packets and there are no chances for the low priority packets to get the resources and they are never able to reach their destinations. [15].

Packet transmission inside the network determines flow control of the network.

The traditional routing techniques are the XY routing,West first,North last,Negative last,Deterministic etc different applications needs different routing algorithms[15]

Emerging Routing Techniques

The above mentioned traditional algorithms are inefficient in solving the high dimentional NOC design with complex search process. The above mentioned applications especially for the real time applications ,there are lot of limitation and drawbacks using the traditional algorithms. For such problems, machine learning based routing techniques are used which solves most of the fundamental problems of networking such as traffic prediction,congestion, control,Resource and fault management QOS and QOE management etcThus machine learning based routing techniques yields better performance and better designs for all quality of metrics[16]-[18].

Tools used for Evaluating NOC

The Tools used depends on the applications for which NOC is used. NOC is an integral part of Present day embedded applications and most often these systems are subjected to the hard constraints of space,energy and ecxecution time Thus estimation of the NOC characteristics could be very helpful to the NOC designers.

The tools are are classified as synthesisers and simulators.Synthesise evaluates the quality of the architectures such as space and energy consumption. Whereas the simulators addresses two criteria power dissipations and performance parameters such as throughput,latency,and reliability.

The most popular tools used are NS-2 ,Noxim ,DARSIM ,ORION . Nowadays FPGA based evaluation methods are also used[19]-[20].

Conclusion:

As the processor technology is growing with many core processors with more than 100 cores on a single chip which increases the complexity and criticality in the on chip communication.This gave rise to the on chip communication architectures with improved SOC performance compare to a dedicated bus architecture.. But modern SOCs are further becoming complex with huge data processing which gave rise to emerging routing techniques and ML based routing schemes,for better performances of SOCs.

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