"Design and Analysis of Novel AC-AC Converter for Circuit Breaker Testing."

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***Abstract*— This paper presents a novel single-phase ac–ac converter with power factor correction and output current control for circuit-breaker testing according to the IEC 60898 standard. The important advantages of the proposed circuit are low component count and fast responses for the standard requirement, especially a current step at the beginning of the test. The proposed single-phase ac–ac converter can operate in either buck or boost mode to accommodate the need for a wide range of output current while satisfying the ramping and step current requirements in the standard. The control circuits consist of two parts, dc voltage control of dc-link capacitors and ac output current controls operating simultaneously. The proposed circuit is verified through both computer simulation and hardware experiment. An example of a 50 A circuit breaker testing according to the IEC 60898 is demonstrated in the paper.**

***Keywords*— Buck–boost capability, circuit-breaker (CB), continuous current mode (CCM), current control, power factor correction (PFC), single-phase ac–ac converter..**

I INTRODUCTION

A CIRCUIT-BREAKER (CB) is indispensable equipment in residential, commercial and industrial systems. It is designed to protect an electrical circuit from damage caused by overload or short circuit. The capability of interrupting the flow of the current to protect devices enables ts utilization in virtually every application. The time tripping characteristics of the CB and the test procedures detailed in IEC 60898 are necessary in the process of quality control. Commercially available current sources for CB testing are designed using a motor-driven tap-changing auto-transformer for ac output current regulation. Recently, several ac-ac converters have been developed and improved in terms of higher current rating capability and higher efficiency. Also, they have included the power factor correction (PFC) to regulate the input current to be sinusoidal wave shaping with nearly unity power factor. In practice, the ac-ac converters are widely applied to various industrial applications such as UPS, voltage stabilizer, electric welding, and etc.

Several topologies of single-phase ac-ac converter had been reported. The single-phase ac-ac two-leg, three-leg and four leg (two full-bridges) converters have been presents. They are widely adopted choices of converters in UPS, motor drive or grid-connected applications These topologies consist mainly of two stages; a controlled rectifier (e.g., boost PFC topology) and a single-phase inverter. They can be operated in either buck or boost mode for the desired level of ac output voltage. The output frequency is controllable and can be set to the values different from the input frequency. The three-leg and two-leg single-phase ac-ac converters are operated in hard switching scheme, producing the switching loss and electromagnetic interferences. In addition, the two-leg single-phase converter has high ripple voltage at the dc-link capacitors. In a buck-type ac-ac converter reported, the ac output voltage is controlled using the modified sinusoidal pulsed-width modulation (SPWM). This topology introduces a distortion on the ac output voltage at the zero-crossings. Also, the output voltage is limited to the values less than the input voltage due to its buck-type topology.

II. THE SINGLE-PHASE AC–AC CONVERTER.

The key requirements of ac–ac converter for circuit-breaker testing are a wide range of output voltage with low harmonic distortion and high input power factor. Therefore, it must be capable of operating in buck and boost modes with the required dynamics of step current and ramp rate specified in [1]. The single-phase ac–ac converter has been presented in the system application for CB testing [2] according to the CB testing standard (IEC 60898) in Table I. It used four switches to control input current and output current with the same ground. The first part integrates rectifier and boost converter to regulate the dc-link voltages and control the ac input current with sinusoidal waveform in phase with the ac input voltage. The output current control is based on half-bridge topology to drive the positive and negative pulses by means of SPWM technique to the output. Recently, a novel single phase ac–ac converter has been presented [3] and it is also suitable for CB testing application because it supports all key requirements of CB testing standard. This converter operates similarly with converter in [2], but its difference is about the converter output

separated ground instead of shared ground. The ac–ac converter application for CB testing does not require the ac current output sharing the same ground with ac input voltage. As a result, the novel ac–ac converter has been selected to implement the proposed system for CB testing application. In addition, the proposed system is realized by the digital implementation according to the CB testing standard (IEC 60898).

TABLE I
TIME–CURRENT OPERATING CHARACTERISTICS

Test	Type	Test current	Limits of tripping or non tripping time	Results to be obtained
a	B, C, D	$1.13I_n$	$t \geq 1h$ ($I_n \leq 63$ A) $t \geq 2h$ ($I_n > 63$ A)	No Tripping
b	B, C, D	$1.45I_n$	$t < 1h$ ($I_n \leq 63$ A) $t < 2h$ ($I_n > 63$ A)	Tripping
c	B, C, D	$2.55I_n$	$1s<t<60s$ ($I_n \leq 32A$) $1s<t<120s$ ($I_n > 32A$)	Tripping
d	B	$3I_n$	$t \geq 0.1$ s	No Tripping
	C	$5I_n$		
	D	$10I_n$		
e	B	$5I_n$	$t < 0.1$ s	Tripping
	C	$10I_n$		
	D	$20I_n$		

TABLE II

NUMBER OF COMPONENTS IN TWO CONVERTERS

Device	Four-leg	Novel
inductor	1	1
switch	8	4
DC-link Capacitor	1	2
diode	0	6

The novel ac–ac converter topology can be compared with the four-leg converters (two full-bridges) [7]. They are the same operation both input current control and output voltage control with separated ground between input and output sides.

A number of components is counted and compared between novel converter and four-leg converter as shown in Table II.

The novel topology has the reduced number of switches from eight to only four switches. Although the number of diodes is increased but the cost of switches is much more expensive than one of diodes.

The CB testing under the over current test condition consists of five tests, a, b, c, d, and e where the test currents vary from

1.13 to 20 times of the nominal rated current of CB (In) as shown in Table I [1]. The first three tests (a, b, and c) require that the peak of the test current is gradually varied whereas a step change is required in the other tests. The time current characteristics for over current CB test provided in Table I are the requirements for various CB types (B, C, and D). Note that the current characteristics of each test are determined by the initial condition specified in the standard. For instance, the initial condition for tests a, c, d, or e is cold, meaning that there is no previous loading of CB before testing. However, the initial condition of the test b is performed immediately after the end of test a.

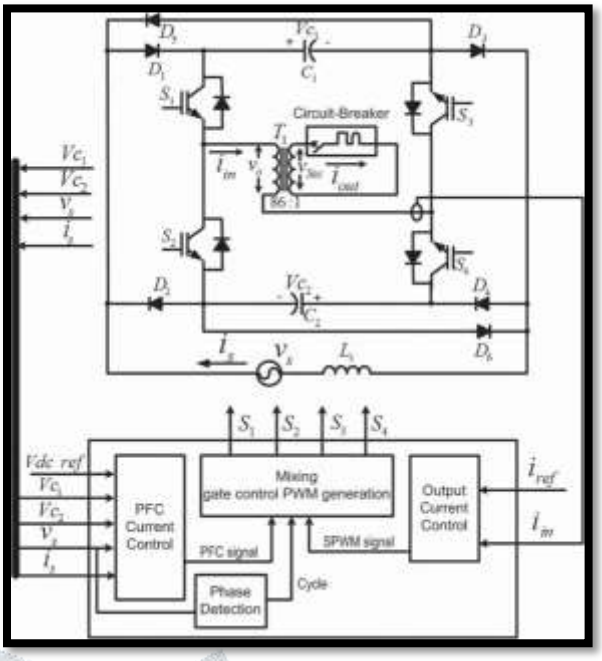

Fig. 1. Proposed ac–ac converter with dc-link voltage and ac output current controllers.

This paper is organized as follows. Section II presents principles of proposed system such as circuit operation and control strategy. Section III presents the simulation results which are then compared with experimental results in Section IV. Finally,Section V concludes the proposed system.

III. PROPOSED SYSTEM

The proposed system is shown in Fig. 1. The ac–ac converter topology consists of four main switches (S1–S4), two dc-link capacitors (C1 and C2), an inductor (Ls), diodes (D1–D6), and a power transformer (T1). In the system, the VC1, VC2, is and vs are measured and fed back to the digital controller. The dc-link capacitor (C1) is charged and VC1 is maintained constant dur- ing the positive cycle of vs while the capacitor voltage VC2 is charged and maintained constant during the negative cycle. The input voltage is used as the reference signal for controlling the input current, is. The output current is regulated by the switches S1 and S3 during the positive pulse while the switches S2 and S4 operate during the negative pulse, using the sinusoidal PWM (SPWM) technique. The primary winding of the power transformer T1, with a turn ratio of 86.3, is connected to the output of the DC–AC converter. The transformer's secondary winding is short-circuited through the CB during testing. The output current is amplified by an order of the T1's turn ratio. The proposed topology yields power factor in the range of (0.97–0.99) under various output frequencies.

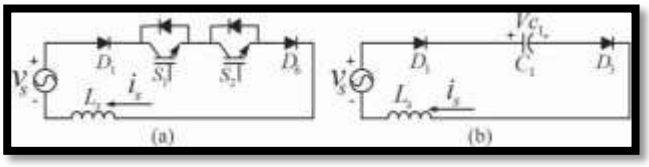

Fig. 2. Equivalent circuits of (a) charging and (b) discharging inductor current during positive cycle.

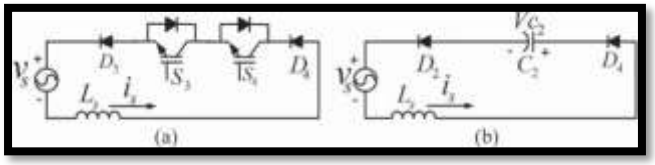

Fig. 3. Equivalent circuits of (a) charging and (b) discharging inductor current during negative cycle.

A. Integrated Rectifier/Boost Converter.

The integrated rectifier and boost converter in the proposed system include three functions as follows.

i. Rectifying the input voltage into a dc voltage signal.
ii. Boosting the dc voltage.
iii. Shaping the ac input current to be sinusoidal waveform.

The switches S1 and S2 are operated during the positive half cycle of the input voltage vs to boost the voltage of the dc-link capacitor C1. The waveform of the input voltage vs is used as a reference for shaping the inductor current (is). The aim is to force the input current is to be in phase with the input voltage for unity power factor. Meanwhile, the capacitor voltage, VC1, is maintained to a constant value. Figs. 2 and 3 show the circuit configurations during the charging and discharging cycles of the inductor current is. During the positive cycle of the input voltage, the switches S1 and S2 are turned on and the inductor current is increases as shown in Fig. 2(a). To complete the boost cycle, the switch S1 or S2 is turned off, depending on the output pulses, and the inductor current is is decreased, as shown in Fig. 2(b). Similarly, the operations of charging and discharging inductor current during the negative half cycle of the input voltage are repeated through switches S3 and S4, as shown in Fig. 3.

B. DC–AC Converter.

The proposed DC–AC converter is described in this section. The switches S1 and S3 are turned on to drive positive pulses to the converter output from the dc-link voltage, VC1, as shown in Fig. 4(a). Similarly, during the negative output pulse, the dc- link voltage VC2 is connected to the converter output by turning on the switches S2 and S4, as shown in Fig. 4(b). The output of the DC–AC converter is directly connected to the primary winding of the transformer T1.

The transformer's secondary winding is short-circuited through the CB under test. At this stage, the transformer leakage reactance and resistance form a low-pass filter path for the converter's output signal. With a proper selection of the switching frequency, a low distortion sinusoidal current at the transformer secondary can be obtained. The output voltage is given as

$$v_o = \frac{m_a}{\sqrt{2}} . V_{Ct} \qquad (1)$$

where ma is the amplitude modulation index and V_{Ct} is the dc- link capacitor voltage.

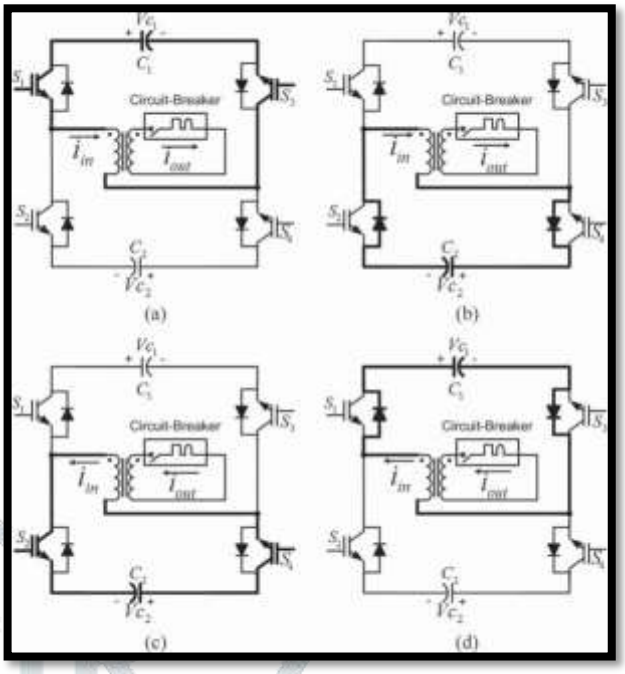

Fig. 4. Circuit configurations under (a) positive and (c) negative pulses of bipolar SPWM operation, (b) and (d) commutation current.

C. Power Transformer.

Since the current required for the CB testing is in the range of hundreds of amperes, a transformer is included in the proposed system. The addition of the transformer serves two purposes, a low-pass filter circuitry and a current amplification for the desired output current.

Taking the transformer's impedance into consideration, the cutoff frequency (fc) of the low-pass filter circuit is given as

$$f_c = \frac{R_{eq}}{2\pi L_{eq}} \qquad (2)$$

where X_{eq} and R_{eq} are the equivalent leakage reactance and resistance of the transformer, respectively. The important benefit of the current amplification capability enables the use of low current rating switching devices in the converter. Even though the converter supplies a bipolar SPWM signal to the transformer, the majority of the transformer's current is the line frequency component therefore, an iron core transformer is chosen. Note that during the CB testing, once the tripping mechanism is initiated, the current through the circuit breaker becomes zero indicating that the secondary of the transformer is open. However, there is a small amount of current supplying the transformer under no-load condition.

The proposed system has been designed the turn ratio of 86 for power transformer, using as the current gain amplifier. The output current is controlled by feeding primary side current back into controller for current regulation.

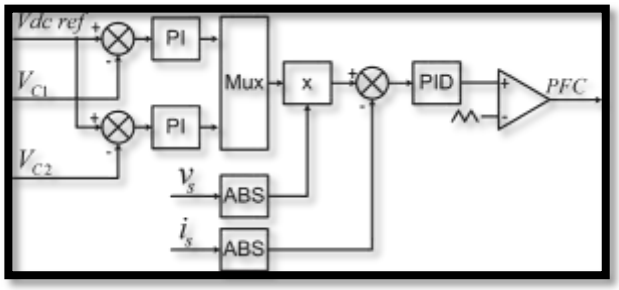

Fig. 5. Block diagram for PFC current control

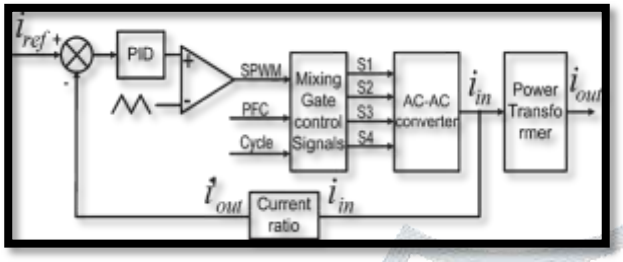

Fig. 6. Block diagram for output current control

D. Controller

The controls of the proposed system are divided into two parts. The first part is the ac input current control for PFC and the dc-link capacitor voltage control. The block diagram of the first part is shown in Fig. 5. The reference signal is obtained from the input voltage for shaping the input current. Each dc-link capacitor voltage is measured and fed through a PI controller. The outputs of two PI controllers are toggling alternately with the cycle of input voltage. The absolute ac input voltage is multiplied by the output of multiplex block to generate a reference signal for the input current. Next, the error of the input current is sent to a PID controller. The output of the PID controller is then modulated with a triangular signal to generate a PWM signal for the PFC part.

The second part is the output current control illustrated in Fig. 6. The PID controller is used as a control signal to create PWM signals for the switches S1, S2, S3, and S4, in Fig. 1. The output of DC–AC converter is connected to the primary winding of the transformer T1. Note that the current control is through the transformer's primary current. This means that the current transformation ratio must be known a priori to properly compensate for the secondary current control. In the mixing gate control signals block, there are two mixing controls, SPWM signals and PFC signal for ac input current control. The mixing of gate control signals can be logically expressed as follows:

$$S_1 = SPWM\ OR\ (PFC AND\ Cycle) \quad (3)$$

$$S_1 = \overline{SPWM}\ OR\ (PFC AND\ Cycle) \quad (4)$$

$$S_1 = SPWM\ OR\ (PFC AND\ \overline{Cycle}) \quad (5)$$

$$S_1 = \overline{SPWM}\ OR\ (PFC AND\ \overline{Cycle}) \quad (6)$$

TABLE III

PARAMETERS IN THE PROPOSED SYSTEM

Parameters	Value	Parameters	Value
L_s	1.5mH	v_s	220Vrms/50Hz
C_1	6,000μF	i_{out}	0-600A/50, 60 Hz
C_2	6,000μF	V_{C1}	400V
f_s	20kHz	V_{C2}	400V

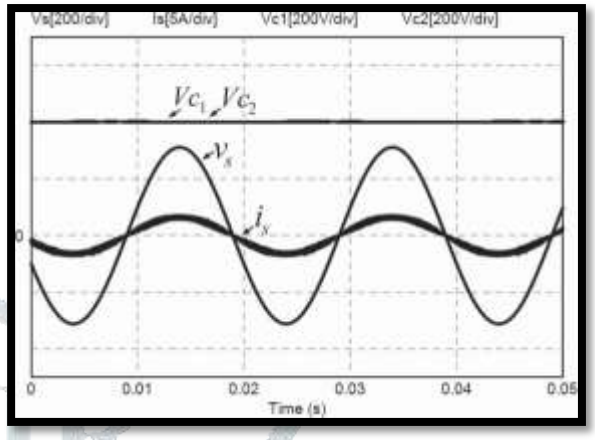

Fig. 7. DC-link voltage (Vc1 and Vc2) at 400 V and ac input voltage (vs) and current (is) waveforms.

where SPWM is a digital logic signal created by the SPWM switching scheme, PFC is a digital logic signal of the input current control and Cycle is a digital logic signal representing the positive cycle of the input voltage. The switches S1 and S3 deliver the positive pulse to the output when the SPWM logic status is high. On the other hand, the $\overline{SPWM}$ is active low to drive the switches S2 and S4 for negative pulse of the output signal. At the same time, the PFC logic and the cycle logic dictate the switching operation for the desired input power factor. When the Cycle signal is high, the switches S1 and S2 are employed to control the input current for the positive cycle of the input voltage. For the negative cycle of the input voltage, the $\overline{Cycle}$ is active low to enable the switches S3 and S4 for input current control.

IV SIMULATION RESULTS

A computer simulation has been carried out to examine the performance of the proposed system. Simulation results confirm the validity of the control algorithms including, input current control, power factor correction, dc-link voltage control, and output current control. The parameters in the proposed system shown in Fig. 1 are summarized in Table III. Fig. 7 shows the simulation results for steady-state response of the input current where the dc reference signal is set to 400 V. The input current, is, is sinusoidal and in phase with the input voltage. Fig. 9 shows the simulated steady-state behavior of the system with the reference set at 200 A(rms). Fig. 10 shows the simulation results for a step response of the output current from 100 to 200 A(rms). Once the output current is increased,

the dc-link capacitor voltage decreases. The PFC controller increases the input current to regulate the dc-link capacitor voltage at the targeted value. Fig. 11 shows simulation results for

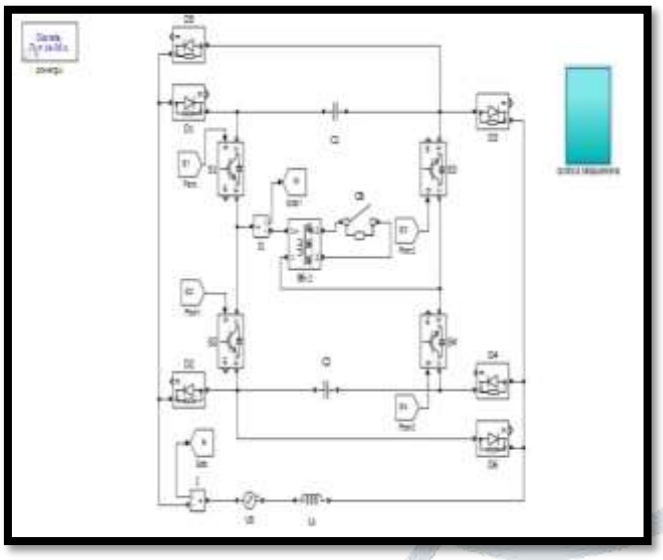

Fig. 8. Simulation of Proposed System

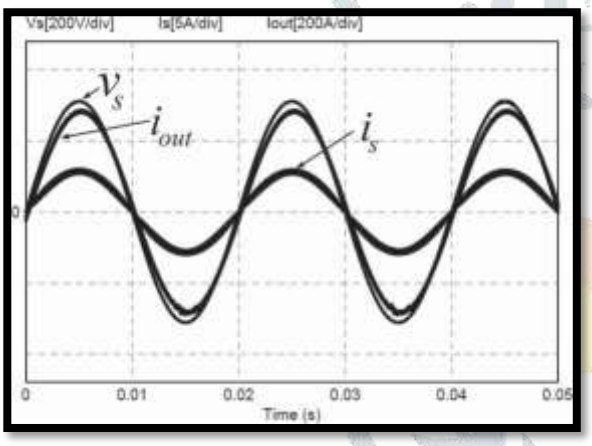

Fig. 9. Output current control at 200 Arms.

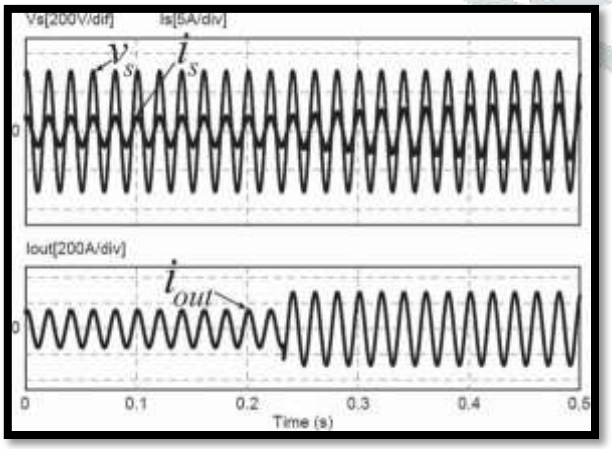

Fig. 10. Response to step change of ac output current from 100 to 200 Arms.

steady-state response of the output current control at 60 Hz, 100 A(rms) which is differed from the input line frequency at 50 Hz. Next, the simulation results of the current controls according to CB test case (a) where the test current is ramped from zero to 1.13In and the test case (d) where the test current is stepped from zero to 3In are demonstrated. A type-B CB with the current rating at 50 A is used as a device under test and the simulation results for test cases (a) and (d) are given in Figs. 12 and 13, respectively. Note that the tripping mechanism of the CB is not shown in the simulation study.

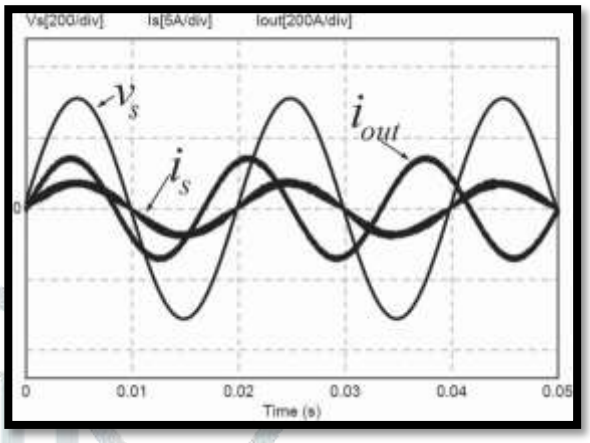

Fig. 11. Output current at 100 A(rms) with the frequency of 60 Hz.

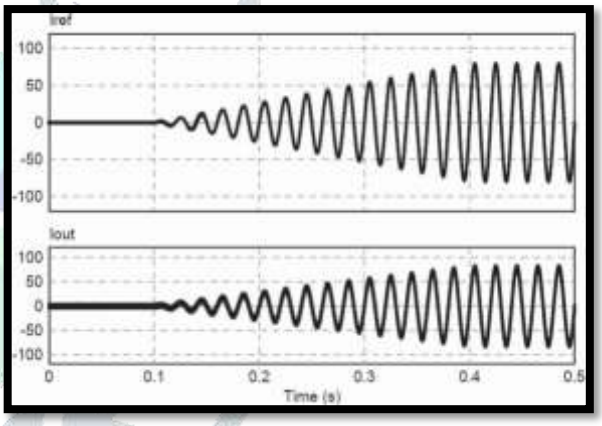

Fig. 12. Ramped current (0 to 56.5 Arms) for test case (a).

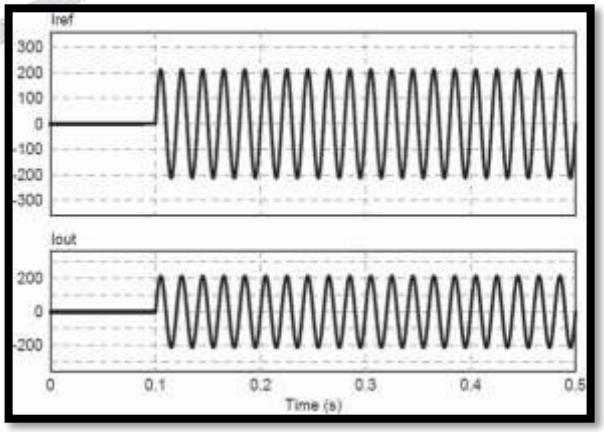

Fig. 13. Test current at 150 Arms for test case (d).

V. CONCLUSION

In this project, the novel single-phase ac-ac converter with ac output current controls will be Design The proposed system is simple and low cost with minimum number of switches employed. The boost PFC topology with dual dc-link voltage controls is also incorporated in the proposed system. The Result will be Observed Using the proposed topology accomplishes the sinusoidal input line current with unity power factor and low THDi of output current. The satisfactory transient step responses of output current will be obtained.

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