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Novel Cascadable Magnetic Majority Gates for Implementing Comprehensive Logic Functions

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Abstract— Quantum dot cellular automata is the recent trend in the field of technology for the designing of any digital circuit involving inverters and majority gates that has the potential to substitute the age old technology of CMOS at the order of Nano level. Herein a full adder and full subtractor circuit is proposed using 5-input majority gate. The new full adder and subtractor reduced the requirement of occupied area, number of cells and energy dissipation. A N-bit ripple carry adder is also designed by one bit full adder.

Keywords- Quantum-dot cellular automata (QCA) **, VLSI, Logic Gates,**

I. INTRODUCTION

Optimizations in VLSI have been done on three factors: Area, Power and Timing (Speed).Area optimization means reducing the space of logic which occupy on the die. This is done in both front-end and back-end of design. In front-end design, proper description of simplified Boolean expression and removing unused states will lead to minimize the gate/transistor utilization. Partition, Floor planning, Placement, and routing are perform in back-end of the design which is done by CAD tool .The CAD tool have a specific algorithm for each process to produce an area efficient design similar to Power optimization. Power optimization is to reduce the power dissipation of the design which suffers by operating voltage, operating frequency, and switching activity. The first two factors are merely specified in design constraints but switching activity is a parameter which varies dynamically, based on the way which designs the logic and input vectors. Timing optimization refers to meeting the user constraints in efficient manner without any violation otherwise, improving performance of the design.

Quantum-dot cellular automata (QCA) are an attractive emerging technology suitable for the development of ultra dense low-power high-performance digital circuits. Quantum-dot cellular automata (QCA) which employs array of coupled quantum dots to implement Boolean logic function. The advantage of QCA lies in the extremely high packing densities possible due to the small size of the dots, the simplified interconnection, and the extremely low power delay product. A basic QCA cell consists of four quantum dots in a square array coupled by tunnel barriers. Electrons are able to tunnel between the dots, but cannot leave the cell. If two excess electrons are placed in the cell, Coulomb repulsion will force the electrons to dots on opposite corners. There are thus two energetically equivalent ground state polarizations can be labeled logic “0”and “1”.The basic building blocks of the QCA architecture are AND,OR and NOT. By using the Majority gate we can reduce the amount of delay.i.e by calculating the propagation and generational carries.

II. EXISTING METHOD

There is a growing importance of decimal arithmetic in commercial, financial and internet based applications. These applications cannot tolerate errors that result from the conversion of binary format to decimal format. Thus, hardware support for decimal arithmetic is receiving considerable attention. Recently, specifications for decimal floating point arithmetic have been added to the draft revision of IEEE-754 standard for floating point arithmetic [43]. Despite the widespread use of binary arithmetic, decimal computation remains essential for many applications. Not only is it required whenever numbers are presented for human inspection, but is also often a necessity when fractions are involved. Decimal fractions are pervasive in human endeavors, yet most cannot be represented by binary fractions.

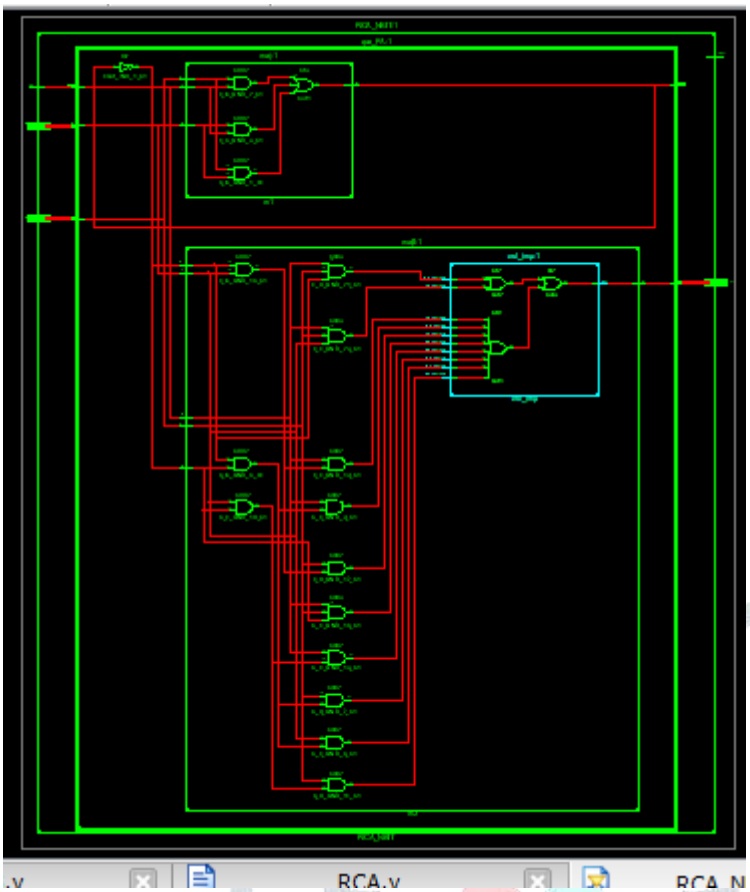
The value 0.1 for example, requires an infinitely recurring binary number. If a binary approximation is used instead of an exact decimal fraction, results can be incorrect even if subsequent arithmetic is correct. As the IEEE standard for decimal floating point is approved, hardware support for decimal floating point arithmetic will be incorporated in processors for various applications. Still, a major consideration while implementing Binary Coded Decimal (BCD) arithmetic is to enhance its speed as much as possible. BCD is a decimal representation of a number directly coded in binary, digit by digit. For example, the number (9527)10 is represented as (1001 0101 0010 0111)BCD . It can be seen that each digit of the decimal number is coded in binary and then concatenated to form BCD representation of the decimal number. To use this representation all the arithmetic and logical operations need to be defined.

III. DESIGN OF COMBINATIONAL LOGIC CIRCUITS USING QCA

Quantum-dot cellular Automata is an emerging technology which provides the various advantages such as faster speed, smaller size, and low power consumption etc. The fundamental device is a QCA cell and can be used to design the various types of circuits (Combinational and sequential). Thus it is a fundamental block of nano-electronic circuits. This chapter extends the design of QCA based combinational circuits and provides an extensive analysis of proposed designs. This chapter discusses the various types of combinational circuits which include the Adder, Subtractor, Multiplexers, Encoders, Code converters etc. In this work all the circuits have been designed using the majority gates.

IV. PROPOSED ARCHITECTURE

Quantum-dot cellular automata (QCA) are an attractive emerging technology suitable for the development of ultra dense low-power high-performance digital circuits. Quantum-dot cellular automata (QCA) which employs array of coupled quantum dots to implement Boolean logic function. The advantage of QCA lies in the extremely high packing densities possible due to the small size of the dots, the simplified interconnection, and the extremely low power delay product. A basic QCA cell consists of four quantum dots in a square array coupled by tunnel barriers. Electrons are able to tunnel between the dots, but cannot leave the cell. If two excess electrons are placed in the cell, Coulomb repulsion will force the electrons to dots on opposite corners. There are thus two energetically equivalent ground state polarizations can be labeled logic “0”and “1”.The basic building blocks of the QCA architecture are AND,OR and NOT. By using the Majority gate we can reduce the amount of delay.i.e by calculating the propagation and generational carries.



V. IDEA OF DESIGNING

Quantum Dot Cellular Automata (sometimes referred to simply as quantum cellular automata, or QCA) are proposed models of quantum computation, which have been devised in analogy to conventional models of cellular automata introduced by von Neumann. Standard solid state QCA cell design considers the distance between quantum dots to be about 20 nm, and a distance between cells of about 60 nm. Just like any CA, Quantum (-dot) Cellular Automata are based on the simple interaction rules between cells placed on a grid. A QCA cell is constructed from four quantum dots arranged in a square pattern. These quantum dots are sites electrons can occupy by tunneling to them.

VI. PROPOSED SYSTEM

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B. Cell Design

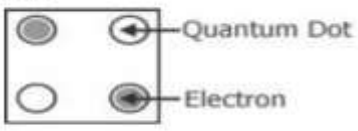


Fig: Simplified Diagram of QCA Cell

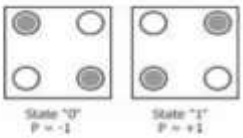


Fig :Four Dot Quantum Cell

C. Structure of Majority gate

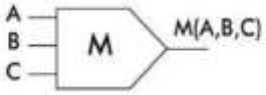


Figure 1:QCA Majority Gate

The QCA majority gate performs a three-input logic function. Assuming the inputs are A ,B and C, the logic function of the majority gate is M =AB+BC+CA

VII. QCA ADDER

FIVE INPUT MAJORITY GATE Initially the researchers have used 3-input majority gates to design the QCA circuits. After that with the requirement of more efficient circuits many five input MGs have been designed whose expression can be written by (1). We have compared some of the 5-input majority gates as given in Table I. Here, we can see that the majority gate designed in [9] has depicted in Fig. 1, which is more efficient than other in relations of area and number of cells with inputoutput accessibility of single layer. In it can also be seen that this majority gate has lesser energy dissipation than other.

$$M(A,B,C,D,E) = ABC + ABD + ABE + ACD + ACE + ADE + BCD + BCE + BDE + CDE \quad (1)$$

In the literature, many circuits for QCA full adder and full subtractor have been presented. Single layer designs are preferred over multilayer designs due to fabrication advantages. The important factor to design a QCA circuit is that it should have less complexity, lesser area and faster processing speed. A. 1-bit Full Adder In a single bit full adder circuit there are 3 input A, B and Cin, where A and B are two inputs being added and Cin is the carry input. Sum represented by S and output carry represented by Co are the two output. The equation can be represented by (2)

$$C_o = AB + BC_{in} + C_{in}A$$
$$S = ABC_{in} + A'B'C_{in} + A'BC_{in}' + AB'C_{in}' \quad (2)$$

$$C_o = M_3(A,B,C_{in}) \quad (3)$$
$$S = M_5(A,B,C_{in},C_o',C_o')$$

Where 3 M denotes the 3-input MG and 5 M denotes the 5-input MG. The schematic of full adder design using MGs is depicts in Fig. 2. The use of 5-input MG make the circuit more simple than using only 3-input MG and inverter.

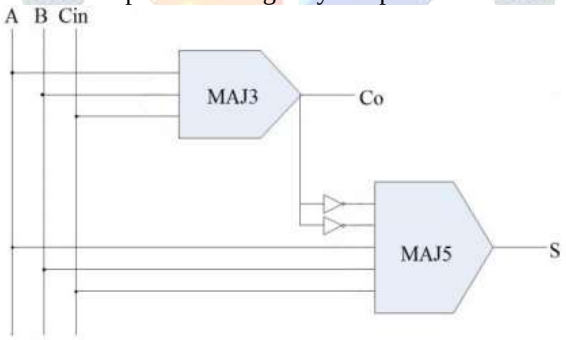


Figure. 2. Schematic of Full Adder design

VIII. RIPPLE CARRY ADDER

Arithmetic operations like addition, subtraction, multiplication, division are basic operations to be implemented in digital computers using basic gates likr AND, OR, NOR, NAND etc. Among all the arithmetic operations if we can implement addition then it is easy to perform multiplication (by repeated addition), subtraction (by negating one operand) or division (repeated subtraction).

Half Adders can be used to add two one bit binary numbers. It is also possible to create a logical circuit using multiple full adders to add N-bit binary numbers.Each full adder inputs a **Cin**, which is the **Cout** of the previous adder. This kind of adder is a **Ripple Carry Adder**, since each carry bit "ripples" to the next full adder. The first (and only the first) full adder may be replaced by a half adder. The block diagram of N-bit Ripple Carry Adder is shown here below –

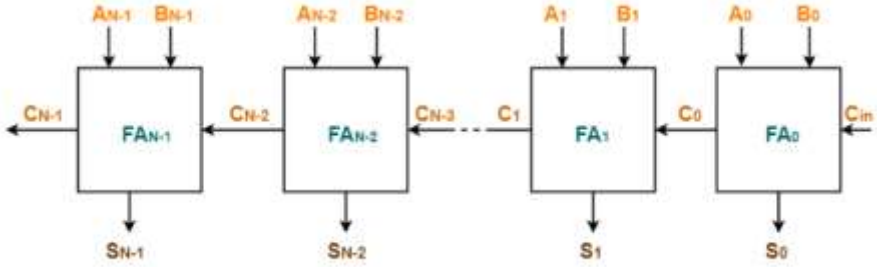


Figure 3 N-bit Ripple Carry Adder

The layout of ripple carry adder is simple, which allows for fast design time; however, the ripple carry adder is relatively slow, since each full adder must wait for the carry bit to be calculated from the previous full adder. The gate delay can easily be calculated by inspection of the full adder circuit. Each full adder requires three levels of logic.In a 32-bit [ripple carry] adder, there are 32 full adders, so the critical path (worst case) delay is 31 * 2(for carry propagation) + 3(for sum) = 65 gate delays.

IX. DESIGN ISSUES

The corresponding boolean expressions are given here to construct a ripple carry adder. In the half adder circuit the sum and carry bits are defined as

sum = A ⊕ B (4)

carry = AB (5)

In the full adder circuit the the Sum and Carry output is defined by inputs A, B and Carry in as

Sum=ABC + ABC + ABC + ABC (6)

Carry=ABC + ABC + ABC + ABC (7)

Having these we could design the circuit. But, we first check to see if there are any logically equivalent statements that would lead to a more structured equivalent circuit.
With a little algebraic manipulation, one can see that

Sum= ABC + ABC + ABC + ABC
= (AB + AB) C + (AB + AB) C

= (A ⊕ B) C + (A ⊕ B) C

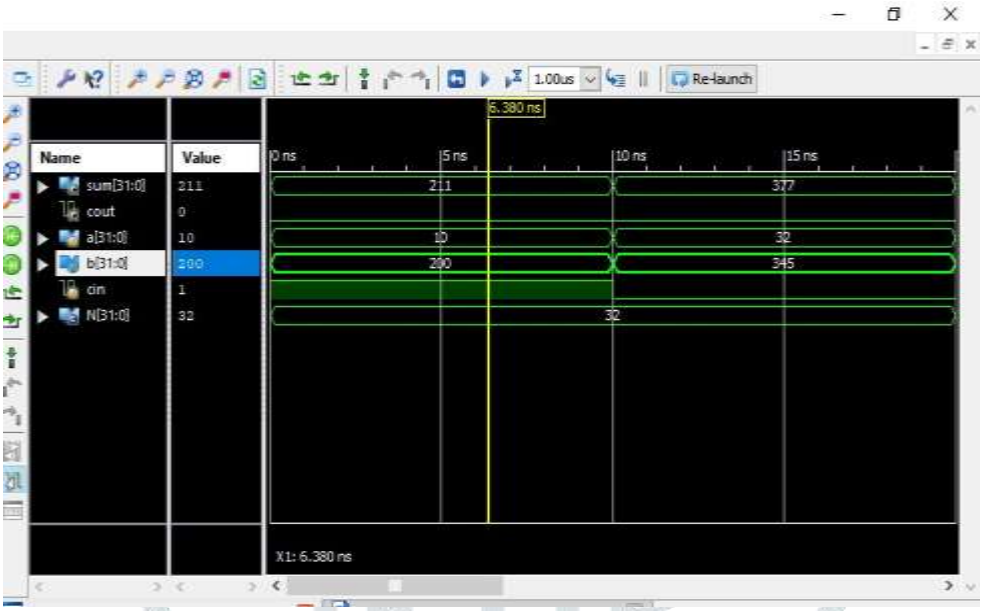
=A ⊕ B ⊕ C

Carry= ABC + ABC + ABC + ABC

= AB + (AB + AB) C

= AB + (A ⊕ B) C

X. SIMULATION RESULTS



Graph 1. Output Waveforms

The simulation result is comparison between existing ripple carry adder and proposed ripple carry adder and also using cadence tolls. Present algorithm is high accurate comparisons to existing method

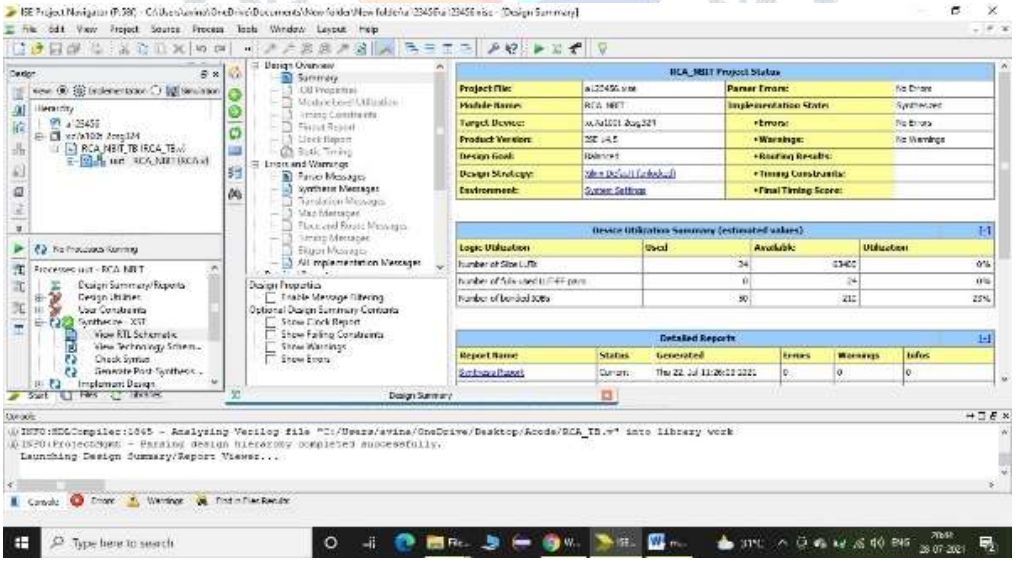


Figure 4: Design Summary

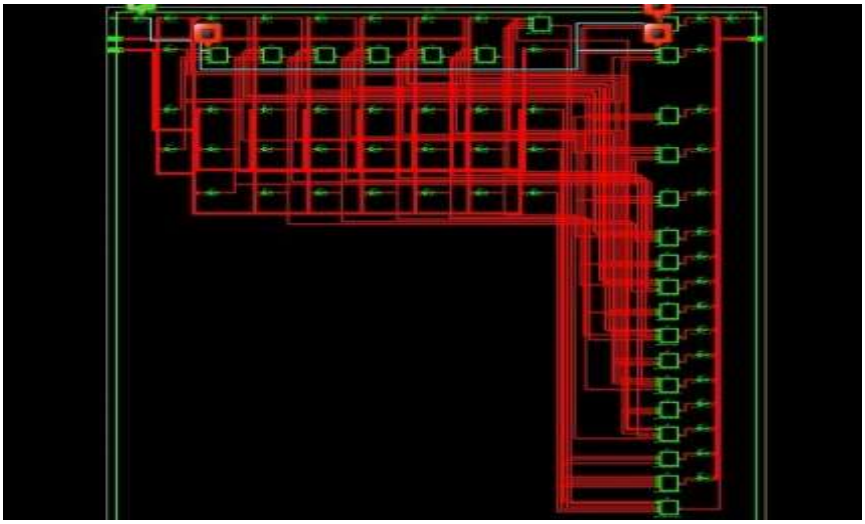


Figure 5. RTL Schematic

XI. COMPARISON BETWEEN EXISTING RIPPLE CARRY ADDER AND PROPOSED RIPPLE CARRY ADDER

For the conventional CMOS ripple carry adder, the total transistor count is 88 but for the proposed ripple carry adder, the transistor count is 50. And delay for CMOS ripple carry adder is 55.63ns but for proposed ripple carry adder delay is 5.207ns. The comparison for the proposed ripple carry adder and conventional ripple carry adder is shown in the table below

Table.-1 Comparison between Existing Ripple Carry Adder and Proposed Ripple Carry Adder

Parameters	Existing System	Proposal System
Transistor count	**88.0000**	**50.0000**
Delay(ns)	**55.6334**	**5.2078**
Power(mw)	**70.0000**	**42.0000**

XII. CONCLUSION

In this work, efficient full adder circuit have been designed using 5-input majority gate in "Xilinx ISE" with the requirement of lesser cell area along with less cell counts and clock cycles delay. An N-bit ripple carry adder circuit is also designed using proposed one bit full adder circuit. Proposed efficient structures can be used to design more complex and high performance QCA circuits at nano scale level in future.

XIII. FUTURE SCOPE

The reduced number of gates of this work offers the great advantage in the reduction of area and also the total delay. The QCA architecture is therefore, low area, low delay, simple and efficient for VLSI hardware implementation. It would be interesting to test the design of the modified 128-bit Novel adders.

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