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DESIGN OF AREA EFFICIENT LOGIC BIST TO TEST PSEUDORANDOM TEST PATTERN GENERATOR BY USING MODIFIED HYBRID TEST POINTS

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Abstract:

The Logic BIST have an extraordinary specialty, which is without having the direct connect with internal modules it will test whole design with the help of automated test pins. As a complement to on-chip test compression, BIST is increasingly being used for self-test, where extraordinary quality, minimal power, reduced silicon Area as well as along with negligible application time are the significant factors. Test points can help to reduce the test time as well as whole silicon area so that from this we can acquire the preferred test coverage along with marginal test patterns. Logic BIST configuration comprises of test pattern generator, response analyzer, ROM as well as comparator etc. The role of LFSR is to generate the test patterns inside the logic BIST which is more efficient than the binary counters. To diminish the ATPG pattern count, test points will be utilized without the assurance of anticipated random testability. To familiarize a fusion test point tactic, in this research which consumes the equivalent elementary set of test arguments to condense enrich fault recognition probabilities. The improved method incorporates pseudo - random number patterns delivered by regular scan chains in a test-per-clock form with hybrid monitoring assessment regions which acquire mistaken consequence each shifting phase in to the appropriate scan chains. The experimental findings acquired for industrial designs support the new schemes' practicality, and they are shown here.

I. INTRODUCTION

The idea of integrating on-chip test circuits, i.e. which of the built-in self-test circuits (BIST). Provides several benefits, including enhanced test portability. Low-level (probe) tests that are more efficient, and easier diagnosis of defective chips at the board level. Scan is a well-known and well-proven structured configuration for test (DFT) methodology in the industry. Scan enables the production of high-quality tests and the debugging of the first silicon, all of which have been currently facilitated by EDA tools, thanks to direct access to memory elements of a circuit under test. Indeed, 20,000 double-capture test patterns would need 8,000,000 as well as 40,000 shift or rather capture cycles, respectively, in a system with 400-cell long scan chains. As a result, testing consumes as little as 0.5 percent of all cycles.

Interestingly, LBIST maintains up with emerging technology needs for a viable test alternative, such as in the rapidly growing automotive electronics industry. This industry's integrated

circuits must meet strict quality and reliability criteria, which are determined by safety standards like as ISO 26262 and Automotive Safety Integrity Level objectives. ISO 26262 compliance necessitates the implementation of additional test measures.

Random Test and Logic BIST:

During experimentation, random pattern development has been used. This method is particularly well suited to Built-In-Self-Testing, in which on-chip circuitry is employed to generate pseudo-random arrangements that are then deployed to the Circuit under Test. They are considered pseudo-random even though, while they have many properties with weird shapes, the structures transmitted to the circuit may be determined ahead of schedule using knowledge of the circuit that generates them. Encourage the implementation modelling can sometimes be performed to anticipate the right response because of pseudo-random patterns to be implemented are established ahead of time.

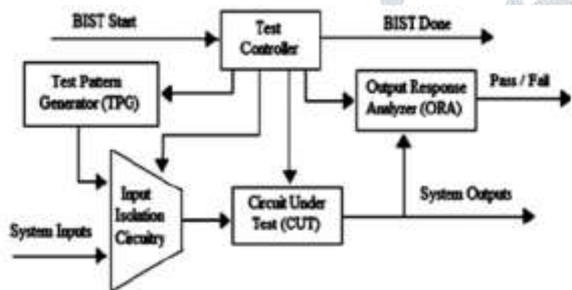


Figure.1: Built In Self-Test design .

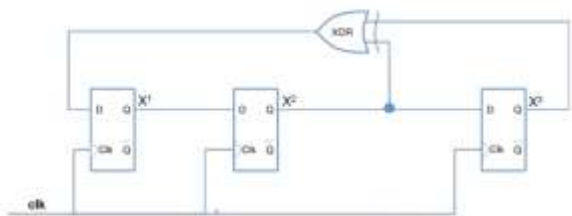


Figure 2: Linear feedback shift register with polynomial of third degree

$$P(x) = 1 + x2 + x3$$

The sequence of flip-flops inside the Linear Feedback Shift Register is n. Except for the combination that corresponds to all 0s, which correlates to all imaginable n-bit permutations.

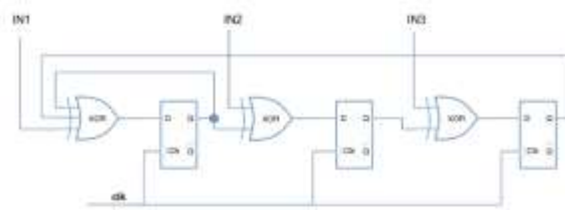


Figure 3: Signature Register with Multiple Inputs (MISR)

Automatic Test-Pattern Generator:

To discover a malfunction, a test pattern should meet two requirements: stimulation as well as monitoring. To trigger the failure, stimulation of the defect produces a distinct binary value at the fault location among the faulty as well as fault-free networks. The parameter A should be switched to a logic one1 to trigger the clogged defect Q. After the failure has been triggered, the fault's consequences must be transmitted to the Carry outcome.

Scan-Chain:

Because sequential circuits cannot be set in an arbitrary state quickly, as well as some network locations might transmit unique contents to a network outcome instantaneously, Automatic Test pattern Generator is significantly more difficult for sequential circuits than that for combinational circuits. Furthermore, propagating a problem to a flip-flop does not instantly make it visible.

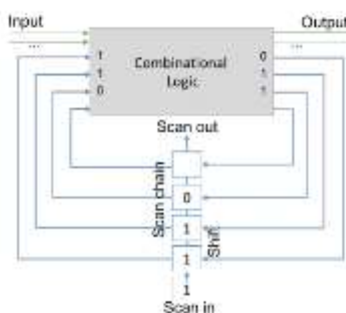


Figure.4: Scan chain

II. RELATED WORK

Despite the functional similarities between the two systems, Logic Built in Self-Test and test compression both used discrete algorithms. Nevertheless, by exchanging some on-chip resources, a combining of Logic Built In Self-Test as well as test compression evolves that may outperform its traditional hybrid kin. Furthermore, there are various production including in-system test requirements that a proposed methodology must fulfil. A combination technique, for example, must continue to

be a significant manufacturing test solution with higher fault coverage, minimal testing data volumes, as well as quick test times.

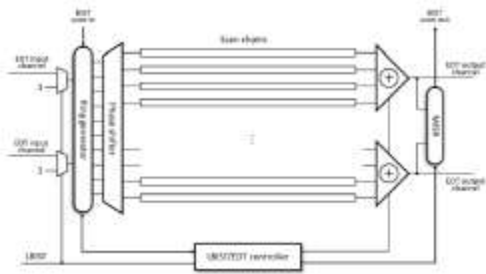


Fig. 5.

Hybrid LBIST/EDT architecture.

The hybrid arrangement works in two phases to reduce external test data as well as pseudo-random configurations. And first primarily, a Pseudo Random Sequence Oscillator generates a specified quantity of pseudorandom stimulus in terms of generating surprise inspections failures.

One such definition encompasses technologies such as Linear Feedback Shift Register sequencing as well as flexible Linear Feedback Shift Register overseeding. Although overlapping fundamental test components with Automatic Test Pattern Generator as well as LBIST might have been mutually beneficial, orthogonally of their test points can quickly elevate a corresponding semiconductor genuine above reasonable standards.

TEST POINTS:

One of most typical purpose of LBIST test points is to generate ridiculous resistant logic better observable. To propagating errors across gated G1 (observe Fig. 6), for illustration, the other input of this gate must be set to 1. G2 is governed by pseudo - random number patterns, therefore the likelihood of receiving 1 on its outcome are negligible.

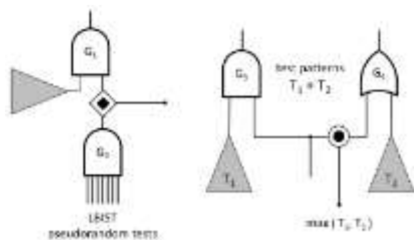


Fig. 6. LBIST and EDT test points

Unlike Logic Built in Self-Test test points, the conflict-aware (or EDT) test points mentioned earlier are primarily concerned with lowering ATPG pattern counts as well as test data volume.

HYBRID TEST POINTS:

With 2 categories of test points to choose from, the challenge now is whether EDT test points can enhance LBIST-based test coverage or else Logic Built in Self-Test test points could diminish ATPG-based pattern counts.

A. Fault propagation:

One of the primary parameters used to determine the most acceptable sites for hybrid test points is the quantity of faults propagating through a network. A fault propagation analysis follows the gate level order of a circuit. Starting at the first level, the amount of faults that occur at each gate's output is calculated as the sum of faults that reach its inputs.

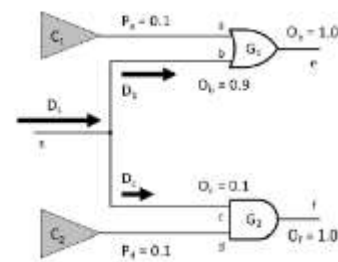


Fig.7. Fault propagation

B. Control points:

Take a look at the circuit in Figure 6. Line x must be set to 1 at least Bx = D1 + D3 times from the standpoint of EDT test points.

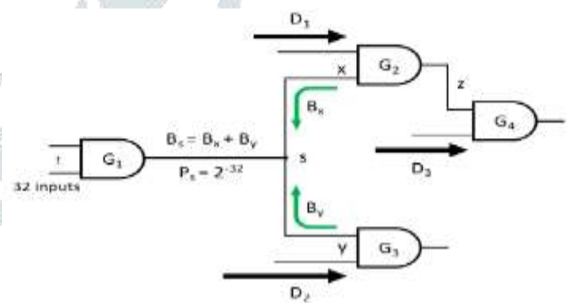


Fig.8. Hybrid conflict.

As appealing as gate G1's outcome for EDT as well as Logic Built In Self-Test test points appears, additional support is required in locating such mutually beneficial positions. So because regulating value at a gate's entry prevents flaw transmission, the metrics b as well as B about how many non-controlling quantities must be assigned to this input to make the gate outcome susceptible to arriving faults may be calculated.

C. Observation points

Due to the extreme propagation circumstances in many circuits, faults are difficult to detect. Observation sites can help shorten propagation pathways in certain situations. Observation performance of Wx of line x monitors to detect minimal observability lines broadcasting to huge number of mistakes.

$$Wx = - Dx \, log10 \, Ox$$

The Dx as well as Ox are the amount of fault propagations at net x as well as line observability.

III. PROPOSED METHOD

The underneath specified figure demonstrations the Logic Built in Self-Test outline. The scan cells (white colored) which we deliberate from previously existing method triggers either in shift mode or in capture mode. The control test points will be fixed to some specific values internally, the shift mode could be operate in two ways based on flip flop associated with it: 1. the first scan chain which is mentioned in below figure, which hosts only the drivers of control points, 2. The second scan cells which are mentioned in figure shows the driving control points are interposed among the other scan chains.

There are two types of test points will be presented in the scan chain methodology those are observation points as well as control points. Since, while performing the shifting operation we will get more testing time as well as more area.

The observation points indicated by the green color which are mentioned in figure are arranged into individual scan chains which accumulates test responses by utilizing XOR gates positioned in the forward facing of scan chains (Fig.9).

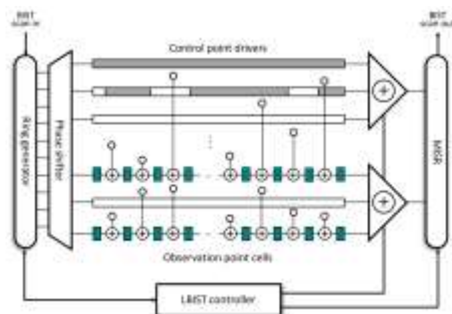


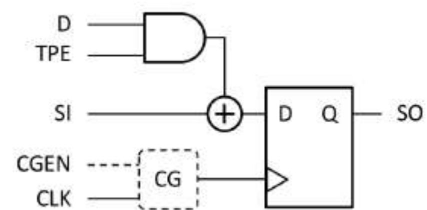
Fig.9: LBIST architecture

Within the single clock cycle, shift as well as the capture mode will be summarizes. The following description reveals about the classical LBIST employing the suggested methodology. Primarily, the whole scan chains capture the every single test response once pseudo-random test pattern is shifted in. To capture as well as accumulate each and every clock cycle by using observation points we need to enable test responses. MISR collects produced responses single-bit per-cycle.

It's worth noting that we limit the input variables that CUT relies on so that test results gathered by scan chains in compaction mode don't dictate the design. Fault simulation is rendered easier as a result of this.

Test responses will be captured when scan chain & compaction chains are fully loaded.

To overcome this problem we can change the Architecture by using only one set of test point in each scan chain which can have both the operations so that area and testing time may get reduced. For this operation we can change the design of Scan cell.



Scan cell for observation point and scan points

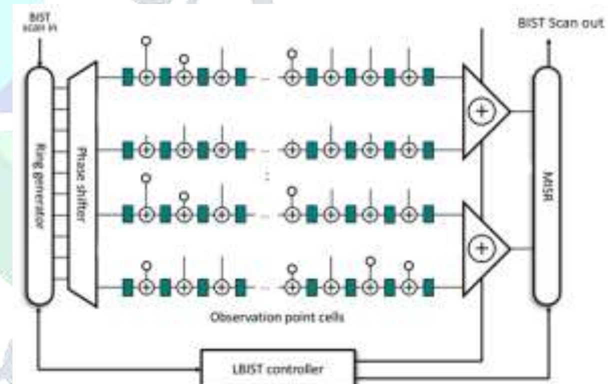


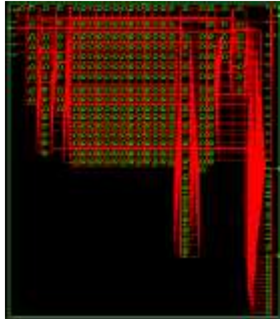
Figure.10: Proposed LBIST

Successively, we recommend n Logic BIST scheme which drastically diminishes the test time by having pseudorandom test patterns transferred to a test-per-clock procedure over scan chains.

RESULTS

By comparing with the existing method, in the proposed method we are getting reduced test application time as well as area will be minimized.

RTL Schematic of Proposed Hybrid architecture



Technology Schematic of Proposed Hybrid architecture

Area and delay report:

	Area	Delay
Existing	199	1.965
Proposed	160	2.065

CONCLUSION

We proposed a new Logic Built In Self-Test methodology in this proposal which dramatically reduces test time as well as area by providing pseudorandom test patterns in a test-per-clock manner through the usage of traditional scan chains, hybrid observation points detects most sensitive fault propagation paths. By consuming only one set of test point in each scan chain which can have both the operations so that area along with testing time may get minimized.

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