



## Enhancement of Power System performance using Series FACTS Controller

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**Abstract:** Static Synchronous Series Compensator (SSSC) is a voltage sourced converter based series FACTS device that provides capacitive or inductive compensation independent of line current. This paper presents the achievement of the required active and reactive power flow into the line for the purpose of compensation as well as validation of enhancement of the power system performance of a transmission line by connecting the SSSC on appropriate location. The effect of variation of the phase angle of the injected voltage on the power system parameters such as sending end voltage, transmission angle, active power, reactive power, and overall power factor with and without SSSC have also been incorporated. The Performance of power system has been tested on IEEE 14-Bus System.

**Key words:** flexible ac transmission (FACTS), static synchronous series compensator (SSSC), voltage sourced converter (VSC), static compensator (STATCOM).

### I INTRODUCTION

The static synchronous series compensator (SSSC) can be operated without an external energy source as reactive power source with and fully controllable independent of transmission line current for the purpose of increasing or decreasing the overall reactive voltage drop across the transmission line and thereby controlling the electric power flow. The SSSC device can provide either capacitive or inductive injected voltage compensation. If AC injected voltage in SSSC lags behind the line current by  $90^\circ$ , capacitive series voltage compensation is obtained in the transmission line. On the contrary, if AC injected voltage of the SSSC leads the line current by  $90^\circ$ ; an inductive series compensation is achieved. The injection of the voltage into the line must take place only when the power is to be subtracted from or added into the line [9].

The SSSC is connected to the line using a quasi-resonant DC supply to provide the soft switching and close loop control for synchronization, compensation and PWM signal generation. The quasi-resonant topology is used in the system which is deviated DC supply in the sense that the

output voltage is not constant value but occasionally goes down to zero when a resonance is triggered. However, it is incorporated into the power system through a series coupling transformer as contrary to the shunt transformer found in STATCOM. The series transformer is used to inject an independently controlled voltage in quadrature with the line current for the purpose of increasing or decreasing the overall voltage drop across the line and thereby controlling the transmitted power. In essence, the SSSC can be considered to be controllable effective line impedance. Since SSSC has a VSC topology, the DC capacitor is used to maintain the DC voltage enabling the SSSC to increase or decrease the transmitted power across the line by a fixed fraction of maximum power. Since the SSSC has the ability to absorb or supply reactive power from or to the line, it makes the surrounding power system impervious to classical sub synchronous resonance (SSR). This paper presents the enhanced power system performance of a transmission line by static synchronous series compensator (SSSC).

### II SERIES REACTIVE COMPENSATION

The desired power flow through the line is translated into the required injected voltage. The control of DC bus voltage plays a vital role in power flow into the line. The operating principle of SSSC and the corresponding phasor diagram have been shown in Figures 1 and 2 respectively. It acts as resistor when DC capacitor is charging and as generator while discharging. The powerflow control is achieved through reactive part of the voltage injected. It is also noted that SSSC acts as capacitor when power flow through the line is increased and as an inductor when power flow is to be decreased. The system shown in Figure 3 describes the basic configuration of static synchronous series compensator using 48 pulse static synchronous series compensator. The capacity of SSSC is  $\pm 70$  MVAR whereas the main transformer has the capacity of 300MVA (approximately 4 to 5 times). The other major challenge in the implementation of VSC based SSSC is sufficiently high value of storage capacitor and therefore not cost effective. With the passage of

time, the charge on capacitor decreases on account of increased real power demand at the receiving end and reactive power compensation for the line. The high value of storage capacitor is suitable for long line compensation in order to sustain the long term and dynamic stability. In case of distribution Static Synchronous Series Compensator (DSSSC), there is a need to bring down the value of storage capacitor which aims at achieving the cost effectiveness and short-term and long-term dynamic stability to suppress sub synchronous resonance (SSR) [12].

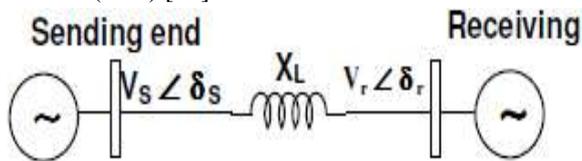


Figure 1: Basic transmission System

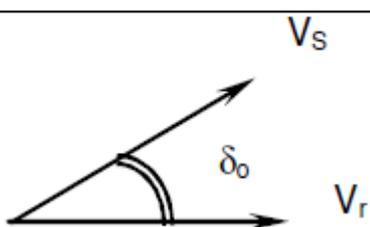


Figure 2: Phasor diagram

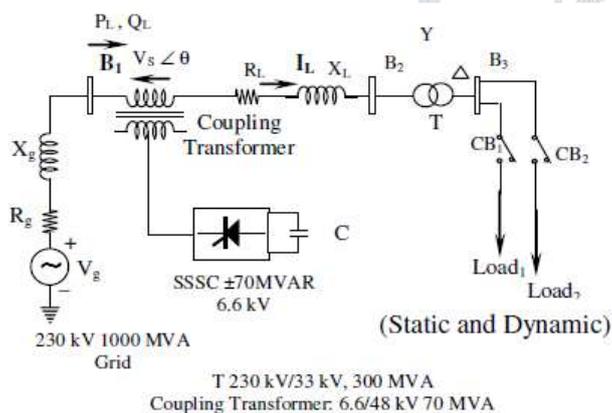


Figure 3: Schematic diagram of SSSC

$$P = \frac{V_s V_r}{X_L} \sin(\delta_s - \delta_r) = \frac{V^2}{X_L} \sin\delta^2 \tag{1}$$

$$P = \frac{V_s V_r}{X_L} [1 - \cos(\delta_s - \delta_r)] = \frac{V^2}{X_L} (1 - \cos\delta) \tag{2}$$

$$\delta = (\delta_s - \delta_r) \tag{3}$$

$$V_s = V_r = V \tag{4}$$

$$Pq = \frac{V^2}{X_{eff}} \sin\delta = \frac{V^2}{X_L [1 - \frac{X_q}{X_L}]} \tag{5}$$

$$Qq = \frac{V^2}{X_{eff}} [1 - \cos\delta] = \frac{V^2}{X_L [1 - \frac{X_q}{X_L}]} [1 - \cos\delta] \tag{6}$$

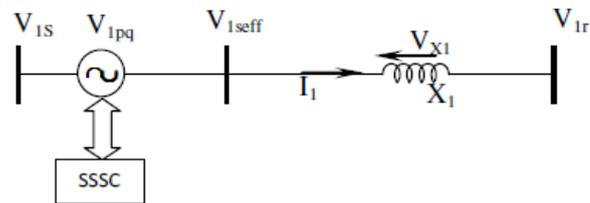


Figure 4: Effect of injected voltage

Where,

- P Active power in p.u.
- Q Reactive power in p.u.
- V<sub>s</sub> Sending end voltage in p.u.
- V<sub>r</sub> Receiving end voltage in p.u.
- X<sub>L</sub> Line reactance in p.u.
- δ<sub>s</sub> Voltage angle at sending end
- δ<sub>r</sub> Voltage angle at receiving end
- P<sub>q</sub> Active power at bus B2 p.u.
- Q<sub>q</sub> Reactive power at bus B2 in p.u.
- X<sub>eff</sub> Effective total transmission line reactance between its sending end and receiving end power system.

The series connected FACTS device can control active or reactive power flows in the line to share power between lines. This serves two purposes namely: reduce line losses and avoids overloads for an instance. Power system performance includes security of power system in terms of flow of active and reactive power. In order to maintain the power flow, the SSSC of appropriate rating has to be connected to weaker bus or line. In this research, IEEE 14-Bus system is taken as a test system.

To identify weaker bus or line we use contingency analysis technique. Since contingency analysis process involves the prediction of the effect of individual contingency cases, the above process becomes very tedious and time consuming when the power system network is large. In order to alleviate the above problem contingency screening or contingency selection process is used.

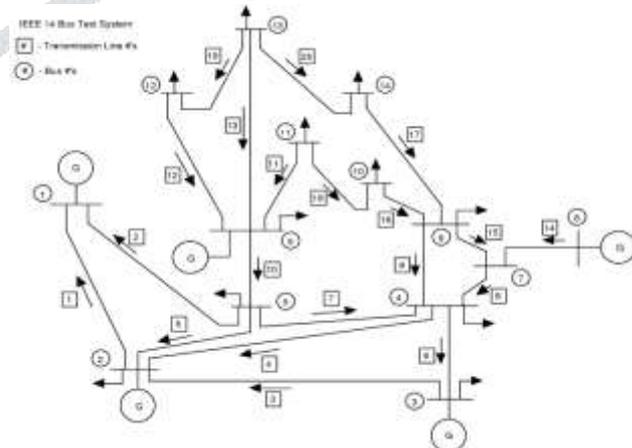


Figure 5: IEEE 14 Bus test system

### III FAST DECOUPLED LOAD FLOW METHOD:

The fast decoupled power flow method is a very fast and efficient method of obtaining power flow problem solution. In this method, both, the speeds as well as the

sparsity are abused. This is actually an extension of Newton-Raphson method formulated in polar coordinates with certain approximations which result into a fast algorithm for power flow solution [14].

**Algorithm of FLDF:** The main advantage of the Fast Decoupled Load Flow Method (FDLF) as compared to the NR method is its reduced memory requirements in storing the Jacobian. There is not much of an advantage from the point of view of speed since the time per iteration of the FDLF is almost the same as that of NR method and it always takes a greater number of iterations to converge because of the approximation [15].

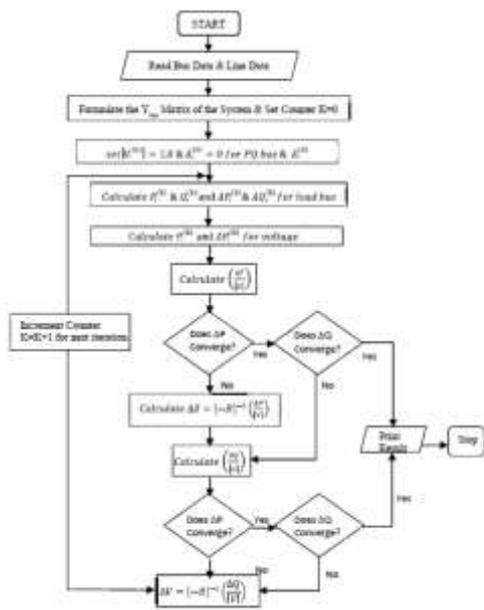


Figure 6: Flowchart for the load flow using FDLF algorithm [15].

### III CONTINGENCY ANALYSIS

Practically it is found that all the possible outages do not cause the overloads or under voltage in the other power system equipments. The process of identifying the contingencies that actually leads to the violation of the operational limits is known as contingency selection. The contingencies are selected by calculating a kind of severity indices known as Performance Indices (PI) [6]. These indices are calculated using the conventional power flow algorithms for individual contingencies in an off-line mode. Based on the values obtained the contingencies are ranked in a manner where the highest value of PI is ranked first. The analysis is then done starting from the contingency that is ranked one and is continued till no severe contingencies are found. There are two kind of performance index which are of great use, these are active power performance index (PIP) and reactive power performance index (PIV). PIP reflects the violation of line active power flow and is given by equation (7)

$$PIP = \sum_{i=0}^l \left( \frac{Pi}{P_{max}} \right) \tag{7}$$

Where,

Pi = Active power flow in line i,

Pi max =Maximum active power flow in line i,

N is the specified component,

L is the total number of transmission lines in the system.If n is a large number, the PI will be a small number if all flows are within limit, and it will be large if one or more lines are overloaded, here the value of n has been kept unity. The value of maximum power flow in each line is calculated using the formula,

$$P_{imax} = \frac{vi*vj}{x} \tag{8}$$

Where,

Vi = Voltage at bus i obtained from FDLF solution

Vj = Voltage at bus j obtained from FDLF solution

X = Reactance of the line connecting bus i and bus j. Another performance index parameter which is used is reactive power performance index corresponding to bus voltage magnitude violations.

It mathematically given by equation No.9,

$$PIV = \sum_{i=1}^{Npq} \left[ \frac{2(Vi - Vinom)}{Vimax - Vimin} \right] \tag{9}$$

Where Vi = voltage of bus i, Vimax and Vimin are maximum and minimum voltage limits, Vinom is average of Vimax and Vimin. Npq is total number of load buses in the system [6].

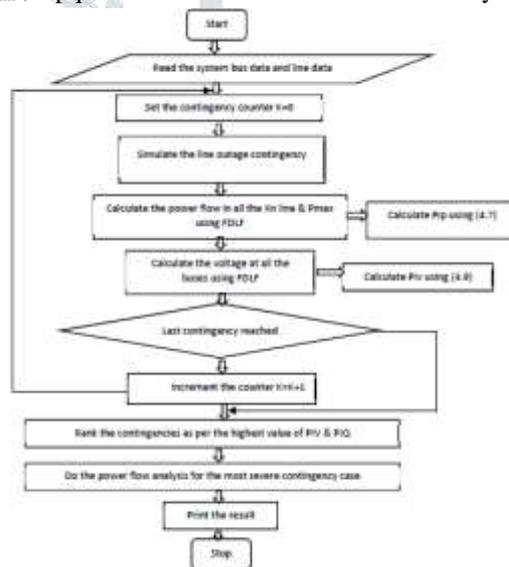


Figure 7: Algorithm for the selection contingency ranking [17]

### IV CONTINGENCY RANKING OF IEEE 14 BUS SYSTEM

To Find the Contingency Ranking Following method is adopted:

The AC power flow program for contingency analysis by the Fast Decoupled Load Flow (FDLF) provides a fast solution to the contingency analysis.

**Table 1: Contingency Ranking**

Outage Line No.	PIP	PIV	Ranking
1	1.1693	7.3032	10
2	0.9807	7.6696	11
3	1.1654	10.0014	7
4	0.9999	7.3213	12
5	0.9820	8.8759	9
6	0.9640	13.2572	2
7	0.9915	0.3566	19
8	1.0747	1.1753	17
9	0.9807	10.5776	4
10	1.2396	1.6047	16
11	1.0142	9.5907	8
12	1.0127	1.8089	15
13	1.0569	1.3669	18
14	1.0072	10.4518	6
15	1.0759	0.0844	20
16	1.0114	13.3464	1
17	1.0164	2.3482	13
18	1.0030	10.5217	5
19	1.0008	12.5538	3
20	1.0076	2.2891	14

The system has a total 20 no. of transmission lines; hence we evaluate for 20-line contingency scenarios by considering the one line outage contingency at a time. The performance indices are summarized in the above Table 1 shows that where it can infer that fault in the line no.16 is the most harmful one and it will result a great impact on the whole system. The high value of PIV for this outage also suggests that the highest attention be given for this line during the operation.

The contingency has been ordered by their ranking where the most severe contingency is being ranked 1 and the least has been rank 20. As per the contingency ranking, we are taken the example of line no.16 which is most severe and attention to be required.

**V RESULTS:****Table 2: Fault at Line No.16**

Bus No.	Bus voltage (main)	Bus voltage after fault	Bus Voltage with SSSC
1	1.06	1.06	1.06
2	1.045	1.045	1.045
3	1.01	1.01	1.01
4	1.00737206	0.9996581	1.012
5	1.00978292	0.9992733	1.008
6	1.07	1.07	1.07
7	1.05120246	1.0452759	1.052
8	1.09	1.09	1.09
9	1.04020686	0.9292870	1.056
10	1.03543270	0.9475309	1.051
11	1.04780211	1.0432581	1.051
12	1.04926356	1.0469203	1.052
13	1.04198704	1.0384292	1.05
14	1.01653643	1.0078093	1.026

Above table 2 shows after fault in presence of Facts device of SSSC the system voltage maintained at enhancement level.

**Table 3: Power flow variations after fault at Line No. 16**

As per the table 3 shows with and without fault in presence of Facts device of SSSC the active power and reactive power shown at enhancement level.

Fault Results			SSSC Results		
Branch	Active Power with Fault (MW)	Reactive Power with Fault (MVAR)	Branch	Active Power with SSSC (MW)	Reactive Power with SSSC (MVAR)
1	219.0753	18.84322	1	220.2856	18.46079
2	103.6593	4.466605	2	113.9695	4.375956
3	101.2825	0.607916	3	111.3562	0.595578
4	76.41618	0.816925	4	84.01668	0.800345
5	56.67178	2.421043	5	62.30846	2.371908
6	30.21541	9.147034	6	33.22069	8.961395
7	80.70368	11.87065	7	88.73062	11.62973

8	37.18052	4.393197	8	40.87856	4.304037
9	21.16201	0.857426	9	23.26682	0.840024
10	60.7738	4.148849	10	66.81848	4.064648
11	10.56111	4.366196	11	11.61154	4.277584
12	10.71925	2.120212	12	11.7854	2.077182
13	24.43719	6.373292	13	26.86776	6.243946
14	88.00586	12.94472	14	96.75909	12.68201
15	37.18052	6.817665	15	40.87856	6.6793
16	6.468626	1.486933	16	7.112007	1.456755
17	12.21696	1.709293	17	13.43208	1.674603
18	5.646241	2.797119	18	6.207827	2.740352
19	2.365423	0.770169	19	2.600692	0.754539
20	8.171436	2.37265	20	8.984182	2.324497

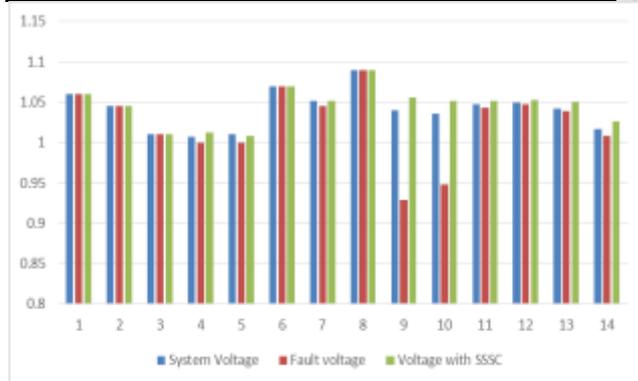


Figure 6: Voltage variation at line No. 16

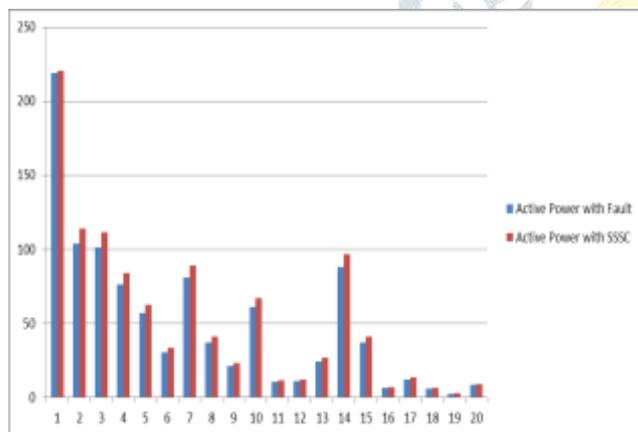


Figure 7: Active power flow at Line No.16

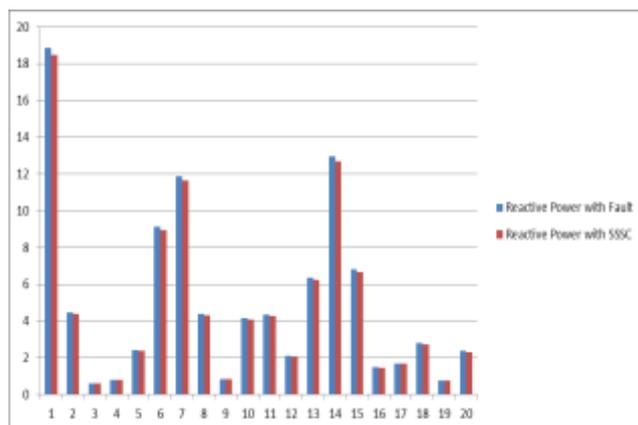


Figure 8: Reactive power flow at Line No. 16

**VI Conclusion:**

From the results we can observe that, the bus voltages under fault conditions are drops down as well as power flow is also disturb. After connecting the SSSC to faulty lines, the results are improved within a specified limit not only where fault is occurred but also power flow improved nearby lines. The bus voltages of faulty lines are improved within a range of 0.06 to 0.4 pu. Active power flow varies within a range of 2MW to 3MW Reactive Power flow varies between 0.2 MVAR to 0.8 MVAR.

**References:**

[1] Jun Yan, Student Member, IEEE, Yufei Tang, Student Member, IEEE, HaiboHe, Senior Member, IEEE, and Yan Sun, Member, IEEE “Cascading Failure Analysis With DC Power Flow Model and Transient Stability Analysis” IEEE TRANSACTIONS ON POWER SYSTEMS, VOL. 30, NO. 1, JANUARY 2015

[2] Abbas Rabiee, Student Member, IEEE, and MostafaParniani, Senior Member, IEEE “Voltage Security Constrained Multi-Period Optimal Reactive Power Flow Using Benders and Optimality Condition Decompositions” IEEE TRANSACTIONS ON POWER SYSTEMS, VOL. 28, NO. 2, MAY 2013.

[3] StéphaneFliscounakis, Patrick Panciatici, Member, IEEE, Florin Capitanescu, and Louis Wehenke, Contingency Ranking With Respect to Overloads in Very Large Power Systems Taking Into Account Uncertainty, Preventive, and Corrective Actions”, IEEE TRANSACTIONS ON POWER SYSTEMS, VOL. 28, NO. 4, NOVEMBER 2013.

[4] EsmaeilGhahremani and Innocent Kamwa, Fellow, IEEE “Optimal Placement of Multiple-Type FACTS Devices to Maximize Power System Loadability Using a Generic Graphical User Interface” IEEE TRANSACTIONS ON POWER SYSTEMS, VOL. 28, NO. 2, MAY 2013.

[5] Yubin Yao ,Mingwu Li, “Designs of Fast Decoupled Load Flow for Study Purpose”, 2012 International Conference on Future Electrical Power and Energy Systems, Energy Procedia 17 ( 2012 ) 127 – 133, ELSEVIER.

[6] Amit Kumar Roy, Sanjay Kumar Jain, “IMPROVED TRANSMISSION LINE CONTINGENCY ANALYSIS IN POWER SYSTEM USING FAST DECOUPLED LOAD FLOW” International Journal of Advances in Engineering & Technology, Nov. 2013.

[7] ToshiMandloi, Anil K Jain “A study of power system security and contingency analysis” International Journal of Scientific Research Engineering & Technology (IJSRET), ISSN 2278 – 0882 Volume 3, Issue 4, July 2014.

[8] S. Ravindra, V. C. Veera Reddy, S. Sivanagaraju, “Power System Security Analysis under Generator Outage Condition” International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, Vol. 4, Issue 1, January 2015.

[9] Dr.P.G.Burade,Dr.J.B.Helonde, “ Optimal Location of FACTS devices on Enhancing system security,” IJSER,vol.2,issue 4, April 2012,pp.1-9.

[10] H.Chahkandi, Nejad, R,Jahani, M Mahvy, “ Applying Imperialist Competitive Algorithm for Optimal Placement of UPFC in power system,” American Journal of Scientific Research, july-2011,pp-2033.

[11] Dr.P.G.Burade,Dr.J.B.Helonde, “ By using Genetic Algorithm Method for Optimal Location of FACTS devices in the deregulated power system,”JATIT,vol.2,2010, pp.64-71.

[12] AlirezaSeifi, SasanCholami and Amin Shabanpour (2010),

“Power flow study and comparison of FACTS: Series (SSSC), Shunt (STATCOM) and Shunt – Series (UPFC)”, The Pacific Journal of Science and Technology, Volume 11, No 1, pp 129 – 137.

[13] Dr.P.G.Burade,Dr.J.B.Helonde, “ A Novel Approach for Optimal power Dispatch using Artificial Intelligence (AI) Methods,” IEEE-Xplorer,2009,pp.1-6.

[14] Akor Titus Terwase, Agber Jonathan Uhaa, Ame-OkoAgaba, “Contingency Modelling and Analysis of Power System Using Load Flow Solution: A Case Study of Makurdi, 33kV Distribution Network” American Journal of Engineering Research (AJER), Vol. 8, Issue-3, pp-251-258, 2019.

[15]T. A. Ramesh Kumar and I. A. Chindambaram,“Power System Security Enhancement using FACTS devices in a Power System Network with Voltage Dependent Loads and ZIP Loads” International Journal of Computer Applications (0975 – 8887) Volume 45– No.4, May 2012.

[16]S. Ravindra, V. C. Veera Reddy and S. Sivanagaraju, “Power System Severity Analysis under Generator Outage Condition” International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, Vol. 4, Issue 1, pp. 317-323 , January 2015.

