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A Clock Gating Technique Using Different Techniques

[1]P.Rajesh,[2] K.Hemaltha, [3]R.Chandrika[4]C.Mallikarjuna Reddy[5]Kalyani Anil Kumar

[1]Assistant Professor, Department of ECE, Annamacharya Institute of Technology and Sciences, Tirupati,A.P. India.

[2,3,4,5]B.Tech Student, Department of ECE, Annamacharya Institute of Technology and Sciences, Tirupati, A.P. India.

Abstract: **In the design of ICs, power dissipation is an important parameter that indicates the need of Low Power circuits in modern VLSI design. In IC chip design various techniques invented for low power design. In several techniques Clock gating is one of widely used technique, which provides very effective solutions for reduction of dynamic power dissipation. Many researchers are modified clock gating techniques in many different ways. This paper included comparative analysis of power in Clock Divider circuit using different clock gating techniques. The look ahead clock gating based on auto gated flip flops method combines the previously three methods. Several techniques to reduce the power have been developed of which clock gating is predominant. This look ahead clock gating computes the clock enabling signals of each flip flop one cycle ahead of time, based on the present cycle data of those flip flops on which it depends. It avoids the tight timing constraints of auto gated and data driven by allotting a full clock cycle for the computation of the enabling signals and their propogation. A look ahead clock gating model is presented which is based on the auto gated flip flop. The comparison between the look ahead, data driven clock gating is done. This clock gating is very useful for reducing the power consumed by digital systems. Power consumption plays an important role in any integrated circuit and is listed as one of the top three challenges in international technology roadmap for semiconductor.**

***Index Terms*: Clock Gating, Flip-flop, Latch, Look ahead, Gate etc.**

1. INTRODUCTION

This project introduces the technique called "A look ahead clock gating based on auto gated flip flop". Previously three gating methods are known. First is synthesis based, deriving clock enabling signals based on the logic of the underlying system. It leaves the majority of the clock pulses driving the flip flops redundant. A data driven method stops most of those and yields higher power savings, but its implementation is complex and application dependent. A third method called auto gated flip flops is simple but yields small power savings. This project presents a look ahead clock gating based on auto gated flip flops[1]. Look ahead clock gating computes the clock enabling signals of each flip flop one cycle ahead of time, based on the present cycle data of those flip flops on which it depends. It avoids the tight timing constraints of auto gated flip flop and data driven clock gating by allotting a full clock cycle for the computation of the enabling signals. The clock gating which enables the clock signals from the clock distribution networks. This technique activates the clock which is needed for the operation of the circuit. The unnecessary clock signals are not activated during the clock gating this saves the power consumption of the circuit. In the earlier period, the VLSI designers were more bent towards the performance and area of the circuits Reliability and cost also gained core importance whereas power consumption was a peripheral consideration. In recent years however a power being given equal importance in comparison to area and speed. As technology scales down, short circuit and leakage power becomes comparable to dynamic power dissipation. Consequently, the identification and modelling of different leakage and switching components is very important for the estimation and reduction of power consumption especially for high speed and low power applications. Clock gating is predominant to reduce the power consumption. With clock gating, the clock signals are ANDed with explicitly predefined enabling signals, clock gating is employed at all levels, system architecture, block design, logic design and gates. Previously, three gating methods are known, first is the synthesis based, deriving clock enabling signals based on the logic of the underlying system. It unfortunately leaves the majority of the clock pulses driving the flip flop redundant. A data driven method stops most of those and yields higher power savings, but its implementation is complex and application dependent. A third method called auto gated flip flop is simple but yields relatively small power savings. Synthesis based clock gating is the most widely used method by EDA tools. Clock enabling signals are very well understood [1] the system level and thus can effectively be defined and capture the periods where functional blocks and modules do not need to be clocked. Those are later being automatically synthesized into clock enabling signals are manually added for every flip flop as a

part of a design methodology still, when modules at a high and gate level are clocked, the state transistor of their underlying flip flops depend on the data being processed. It is important to note that the entire power consumed by a systems stems from the periods where modules clocked signals are enabled. The data driven clocked gating method was proposed to address the flip flops redundancy[2]. The clock signal driving a flip flop is disabled when the flip flops state is not subject to change in the next clock cycle. In an attempt to reduce the overhead of the gating logic, several flip flops are driven by the same clock signal, generated by ORing the enabling signals of the individual flip flops. As consumers continue to demand more functionality in smaller, more energy efficient devices, power optimization rules a hardware designer life. It typically takes multiple iterations over weeks of optimization to achieve power goals and budgets. While power should be optimized at all stages of the design flow, many times it is only addressed after initial register transfer level synthesis runs inefficiencies. RTL clock gating is the most commonly used optimization technique for improving energy efficiency, but lead to the question of how well a design is clock gated. The traditional method of looking at the percentage of registers clock gated is not inductive of the energy efficiency because it does not take into account switching activity. The average clock gating efficiency is a much better indicator of energy consumption because it measures of both the number of register gated and the duration they are turned off. The clock signals have been a great source of power dissipation because of high frequency and load. Clock signals do not perform any computation and mainly used for synchronization. Hence these signals are not carrying any information. So, by using clock gating one can save power by reducing unnecessary clock activities inside the gated module. In many applications, the power consumption of the IC clock system is one of the main sources of chip power dissipation. To address the redundancy from the synthesis based, a data driven clock gating is proposed for flip flops. There the clock signals driving a flip flop is disabled when the flip flops state is not subject to change in the next clock cycle. The data driven gating suffers from a very short time window where the gating circuitry can properly work. The delay of the XOR, OR, latch and the AND gater must not exceed the set up time of the flip flop. Another difficulty of data driven clock gating is its design methodology. The low power look ahead clock gating method combines the previously three methods. The major dynamic power consumers in computing and consumers electronics products is the systems clock signal, typically responsible for 30% to 70% of the total dynamically switching power consumption. Several techniques to reduce the dynamic power have been developed of which clock gating is predominant.

The whole paper is organized as explained in section II through Clock Gating method Section III discusses the proposed system. Section IV shows the Simulation Results The conclusion has been given of the discussed in Section V.

2. CLOCK GATING

Clock gating is proved efficient approach for low power design in IC technology. It is invented in 90's for reducing clock switching in the circuit. Clock gating technique requires to extra clock logic to generate the clock signal which used to control the logic cell. This clock gated signal enabled only when attend logic 0 or 1. This technique reduces the power as well as area of the circuit. The main objective of clock gating technology is reducing the unwanted switching activity through clock pulses when they are not in use. In flip-flop circuit this activity achieved when logic changes from 0 to 1 or 1 to 0, as switching activity increased more power consumed by the circuit. In registers their toggling condition achieved high power dissipation. To implement clock gating technique first find to best place to reduce the major power consumption. Then create logic at particular place to clock enabling signal. Clock enabling signal is find there is no activity for particular unit. That unit is blocked when no need of clock pulses for that circuit. By this scheme dynamic power is reduced and also reduced the area of the circuit.

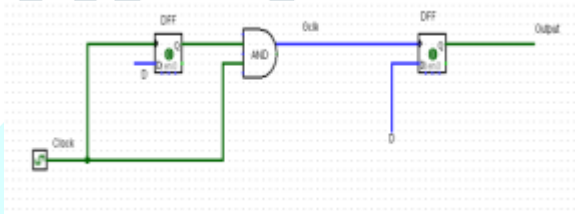

Fig.1 Clock Gating Technique

In figure-1, shows a simple clock gating scheme with individual clock and enabling signal for processing. The gate based clock gating logic is shown in figure, there are clock and enable signals given to the external clock circuitry and then further the gated clock signal given to the logic circuit for further processing. This scheme increases the area as well as power consumption will be more because of individual clock circuitry. In circuit a simple AND gate based clock gating proposed which used only one clock and enable signal with AND gate and this gated clock signal further given to the logic. Some of most commonly used clock gating techniques listed as below

1. Auto gated clock gating
2. Flip-Flop based clock gating
3. Gate based clock gating
4. Latch based clock gating
5. Look ahead clock gating

3. PROPOSED METHOD

In this paper clock divider circuit is designed with all effective clock gating techniques. Clock divider circuit is used to divide clock. For operating a sequential circuit a clock signal is needed as a function. A clock divider is generally defined as a functional device. The clock divider used an input clock as input function and produced an

output clock to corresponded function. The output clock function is defined as the result of the input frequency divided by an integer. Another name of the clock divider circuit is known as pulse divider circuit. After receiving gate pulses at input of clock divider, the circuit only passes a fraction of the pulses at the output node. In this paper Clock divider circuit is implemented with clock gating techniques for low power design. Here also introduced clock divider circuit using various effective clock gated designs. The experimental setup is done with Model-Sim simulator and LogiSim simulator. There is compared the results with each technique. The RTL schematics and circuit diagrams of each circuit is shown as below. The simulated results of clock divider circuit with implementation of each clock gated design are described as below as output waveforms to corresponded input signals. A clock divider circuit without implementation of clock gating technique is shown in fig as below. Simply two inputs reset and clock provided to input nodes and one output as clock_out taken at output node. Two signal count and temp is provided for control the circuit.

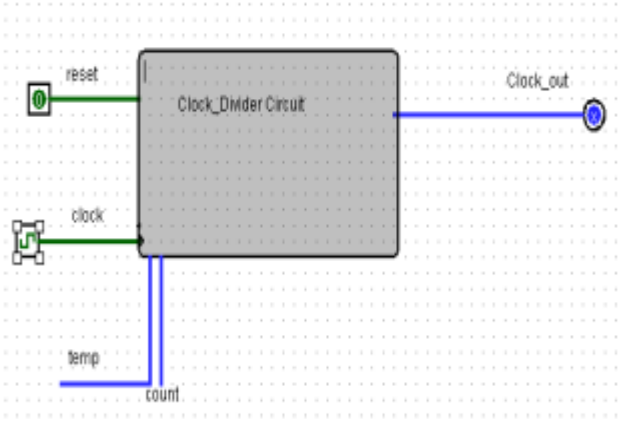

Fig.1: Clock Divider Circuit diagram

1. Clock Divider Using Auto Gated Clock Gating

AGCG is new implementation with clock gating technique; by using master and slave flip-flops the gated signal is generated. There is implementation using AGCG scheme and RTL schematic is shown in figure.

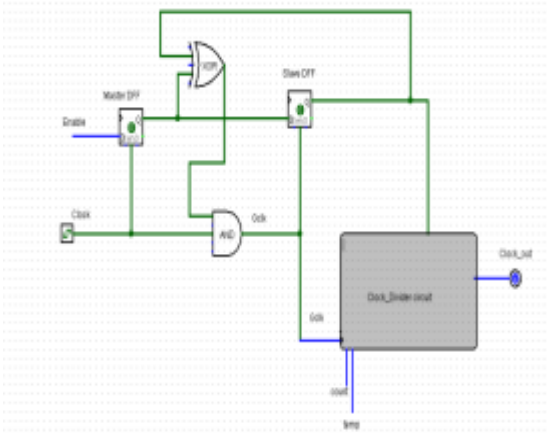

Fig.2: Auto Gated Clock Gating Circuit diagram

2. Clock Divider using FLIP-FLOP based CG

The flip-flop based clock gating technique is implementing on clock divider circuit in this section. This design is considered a D-flip-flop to generate a gated clock and this gated clock signal is provided to clock divider circuit as input signal to process the output.

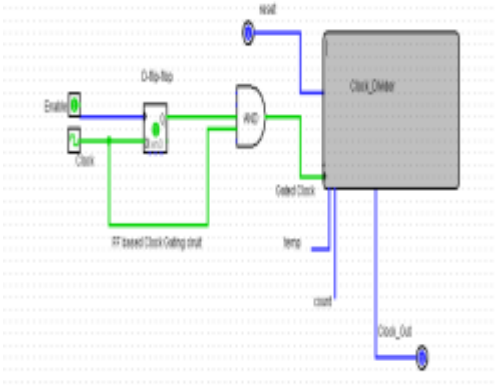

Fig.3: Flip-Flop based Clock GatingCircuit diagram

3. Clock Divider using Gate based CG

Gate based clock gating technique is implemented on clock divider circuit. There is AND gate is used for generating the gated clock signal. RTL schematic of design is shown in figure as below.

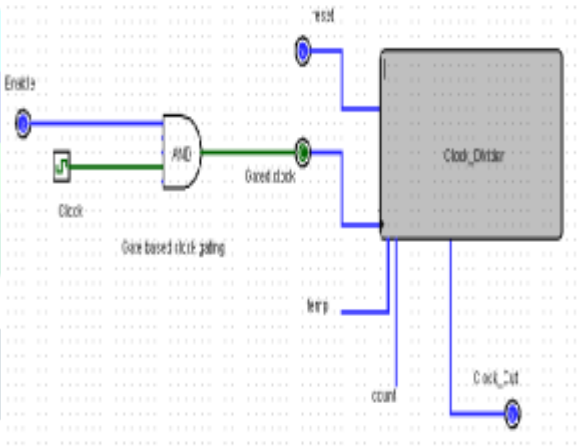

Fig.4: Gate based Clock GatingCircuit diagram

4. Clock Divider Circuit using Latch based CG

Now we implement the circuit using clock gated designs. The latch based clock gating design is consider an external clock gating circuitry with D latch and an AND gate for generate the gated signal. This gated signal is provided to clock divider circuit which processed for low power design.

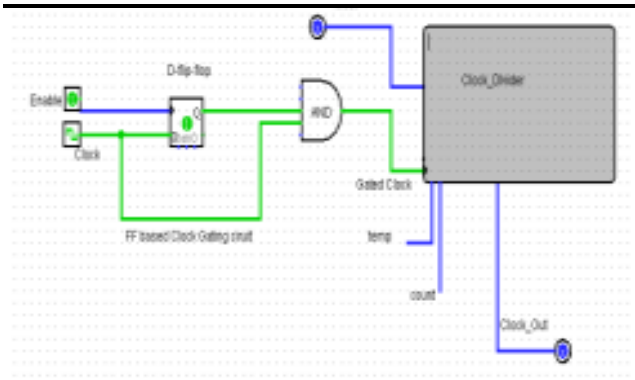

Fig.5: Latch based Clock Gating Circuit diagram

5. Clock Divider Circuit Using Look Ahead Clock Gating

Clock divider circuit is also implemented using LACG technique shown in this section.

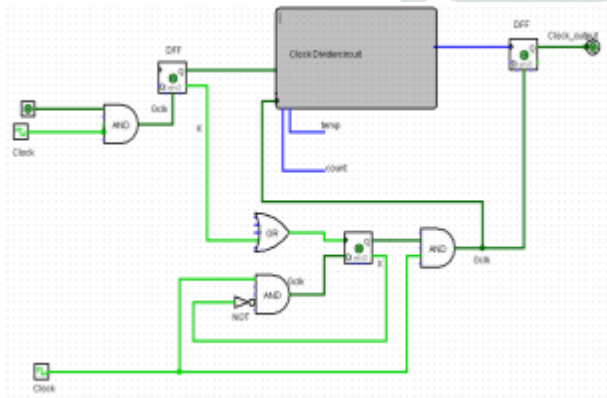

Fig.6: Look Ahead based Clock Gating Circuit diagram

The basic circuit used for look ahead clock gating is auto gated flip flops. This look ahead clock gating takes the auto gated flip flop a leap forward, addressing three goals; Stopping the clock pulse also in the master latch, making it applicable for large and general designs and avoiding the tight timing constraints. Look ahead is based on using the XOR output to generate the clock enabling signals of other flip flops in the system, whose data depend on that flip flop. Here the look ahead clock gating includes the flip flops, XOR gate, AND latch, OR gate and the logic is inverter. The look ahead clock gating circuit is design in the Tanner

This clock gating is a popular technique used in many synchronous circuits for reducing power consumption. Clock gating saves power by adding more logic to a circuit to prune the clock tree. Pruning the clock disables portions of the circuitry so that the flip flops in them do not have to switch states. Switching states consumes power. A flip flop finds out that its clock can be disabled in the next cycle by XORing its output with the present input data that will appear at its output in the next cycle. Here the output of XOR gate are OR to generate a gating signal for flip flops, which is then latched to avoid glitches. When not being switched, the switching power consumption goes to zero, and only leakage currents are incurred. Here clock gating works by taking the enable conditions attached to registers, and uses them to gate the clocks. Therefore, it is imperative that a design must contain these enable conditions in order to use and benefit from clock gating. This clock gating process can also save significant die area as well as power. This clock gating is a popular technique used in many synchronous circuits for reducing power consumption. In general, finding sets of flip flops that minimize the number of redundant clock pulses is not enough to maximize power savings. Grouping must account for the on-die locations of flip flops and gaters, which affect the power consumption due to the capacitive loads resulting from their connections. The physical location of flip flops affect also the delay, and it is therefore desirable for flip flops driven jointly by the same clock gater,[4] to be placed in proximity of each other. Using a flip flop for gating is a considerable overhead that will consume power of its own. This can significantly be reduced by gating flip flop since the flip flop is oppositely clocked and its data is sampled at the clock falling edge, its clock enabling must be negated. In look ahead clock gating, also a flip flop is an ordinary flip flop where the internal XOR gate is connected. Real implementation may require long wires to generate the clock enabling signals, so the grace of a full cycle is a big relief. Clock gating, clock gating limits the clock from being given to every register or flip flops in the processor. In clock gating the gated areas will still be provided with bias power. In this the Tanner tool is used for designing the circuit and for taking their simulation. Other intelligent clock gating techniques are used to minimize the activity portions of the design that do not contribute to the design output for that clock cycle. Clock gating reduces power by preventing logic not used in a given clock cycle from toggling in the clock cycle. Additionally, it prevents the clocks to the flip flops in cases where the clocking either does not produce new data or flip flop outputs are not used by subsequent logic in a given clock cycle. These gating techniques reduces the dynamic and total power consumption.

4. SIMULATION RESULTS

A. Automated based Clock Gate Divider

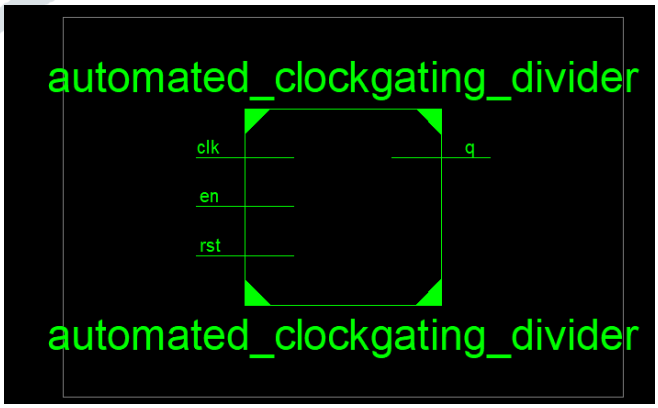

Fig.7: RTL Schematic of ACGD

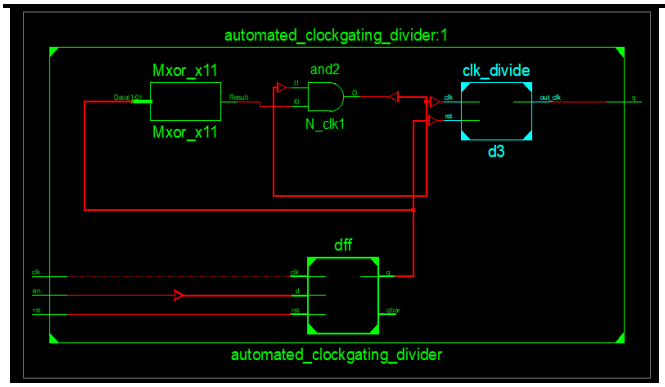

Fig.8: Technology Schematic of ACGD

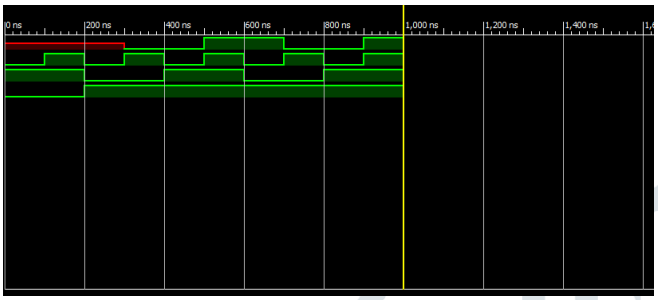

Fig.9: Simulation output for ACGD

B. Flip-Flop based Clock Gate Divider

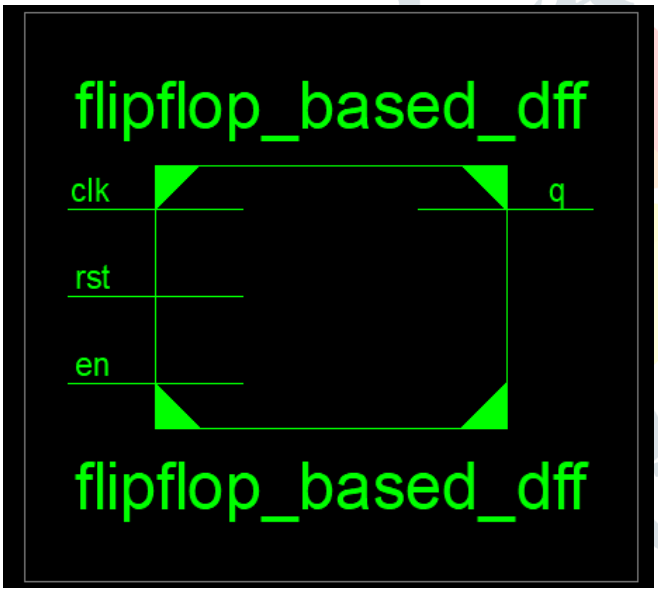

Fig.10: RTL Schematic of FBCGD

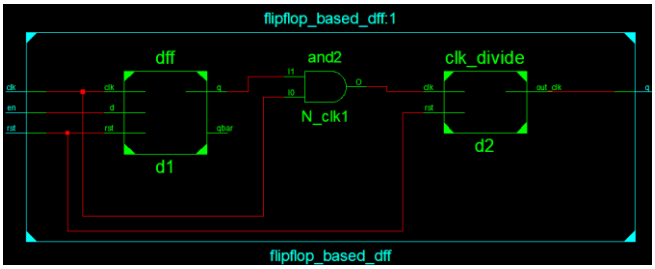

Fig.11: Technology Schematic of FBCGD

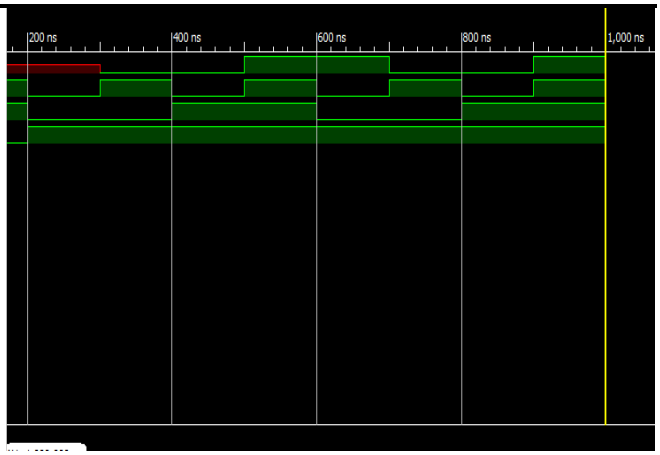

Fig.12: Simulation output for FBCGD

C. Gate based Clock Gate Divider

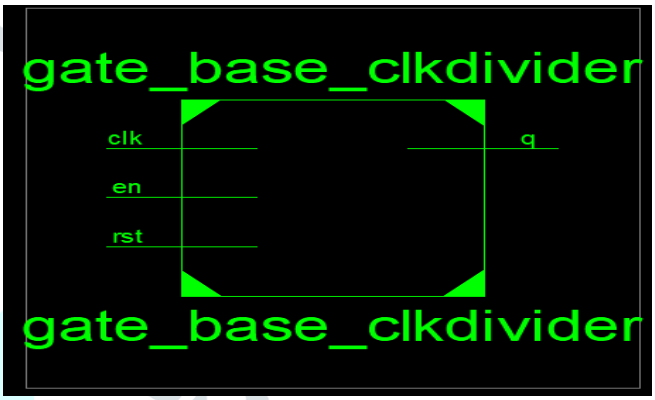

Fig.13: RTL Schematic of GBCGD

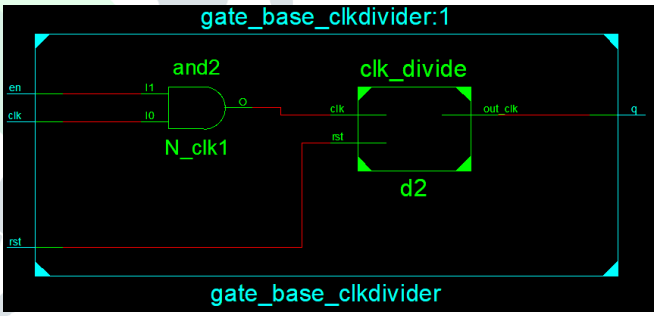

Fig.14: Technology Schematic of GBCGD

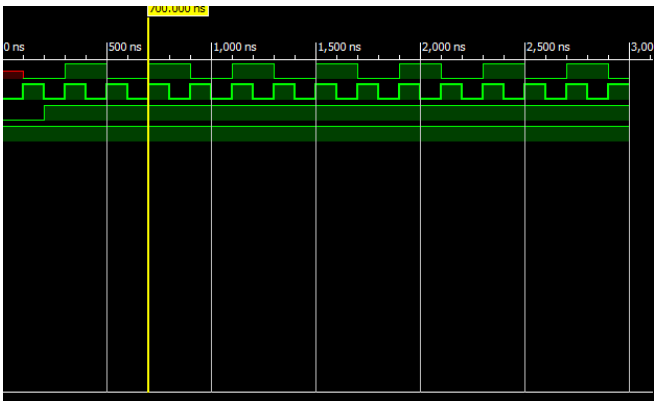

Fig.15: Simulation output for GBCGD

D. Latch based Clock Gate Divider

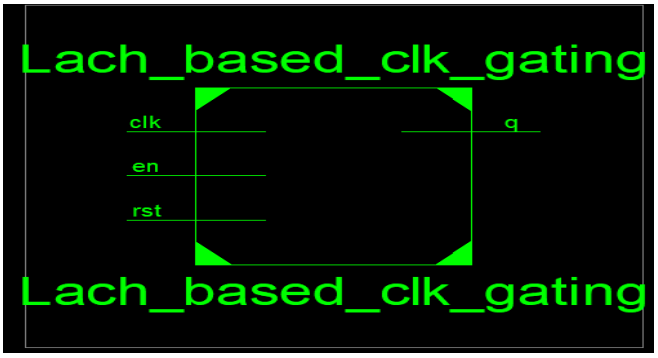

Fig.16: RTL Schematic of LBCGD

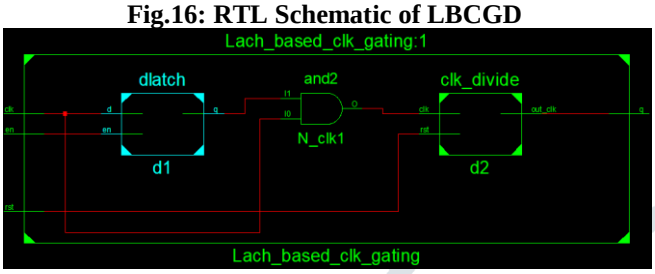

Fig.17: Technology Schematic of LBCGD

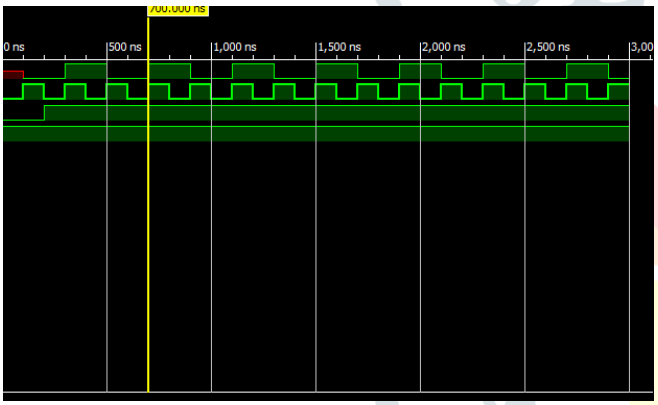

Fig.18: Simulation output for LBCGD

E. Look Ahead based Clock Gate Divider

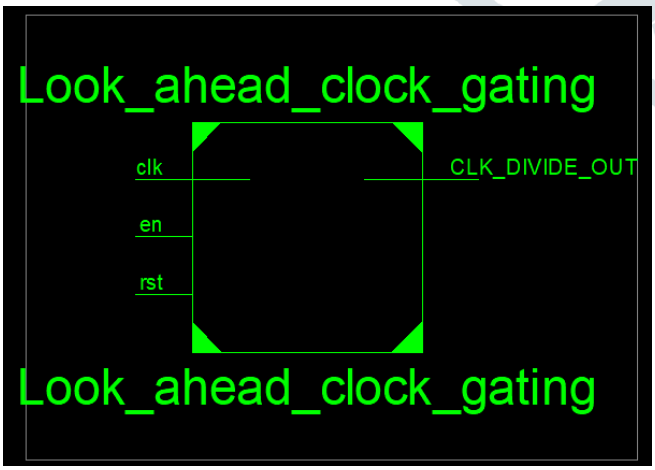

Fig.19: RTL Schematic of LACGD

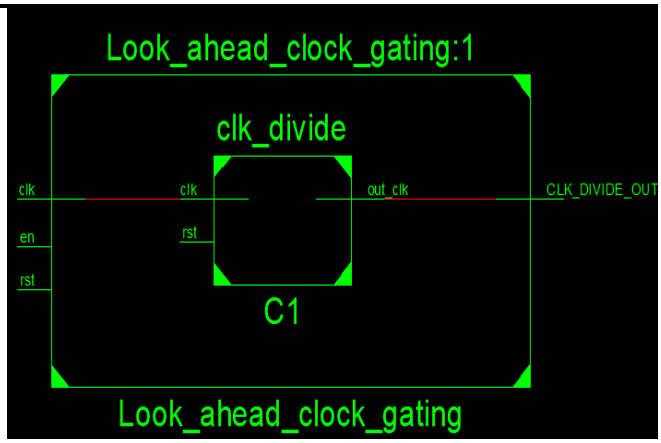

Fig.20: Technology Schematic of LACGD

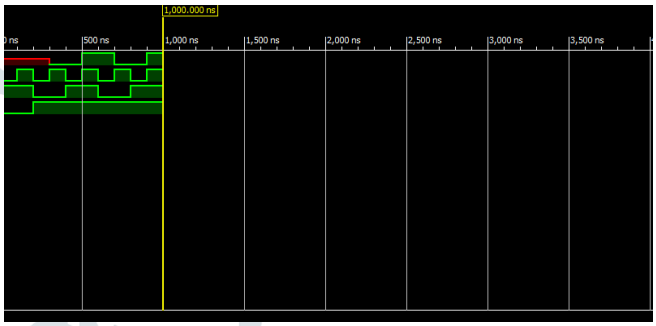

Fig.21: Simulation output for LACGD

5. CONCLUSION

In this paper, a low power look ahead clock gating is introduced and compared it with the previously clock gating technique i.e. Flip-Flop clock gating,gate clock gating,automated clock gating. The result shows that the proposed low power look ahead clock gating is having the less power consumption than the previous data driven clock gating. This look ahead clock gating has been shown to be very useful in reducing the power. One of the major sources responsible for power consumption in digital circuits is the systems clock signal. It contributes towards a large amount of power consumption. Look ahead clock gating has been shown to be very useful in reducing the power consumed by digital systems. As this look ahead clock gating computing the clock enabling signals of each flip flop one cycle ahead of time, based on the present cycle data of the flip flop on which it depends, the drawbacks of the previously three gating methods have been overcome. The tight timing constraints existing in the auto gated flip flop and data driven clock gating methods has been avoided using this look ahead clock gating

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