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EFFICIENT WALLACE TREE MULTIPLIER USING PARALLEL PREFIX ADDER

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ABSTRACT— The Wallace tree multiplier is an effective implementation of a digital circuit that multiplies two numbers and is thought to be faster than a straightforward array multiplier. A Wallace tree multiplier is a parallel multiplier that lowers latency by using the carry save addition technique. The development of multipliers with increasing levels of efficiency has been the focus of numerous researchers. They seek to increase speed and decrease power consumption while utilising less silicon surface. Essentially multiplying two unsigned numbers, the Wallace tree. The commonly used WTM performs faster thanks to the redesigned architecture. The Cadence Genus tool does the synthesis. A parallel multiplier known as a Wallace tree multiplier uses the carry save addition method to cut down on latency. The development of multipliers with increasing levels of efficiency has been the focus of numerous researchers. While utilising a less amount of silicon, they seek to increase speed and reduce power consumption. Essentially multiplying two unsigned numbers, the Wallace tree. The widely recognised WTM performs more quickly thanks to the improved architecture. The Cadence Genus tool does the synthesis.

INTRODUCTION

The majority of digital and high-performance systems, including FIR filters, digital signal processors, microprocessors, etc., include multipliers as essential hardware components. With technological advancements, numerous researchers have worked to create multipliers that offer either of the following: high speed, low power consumption, or reduced area combined with them in multipliers, making them compatible for various high speed, low power, and compact VLSI implementations. Area and speed, however, are two competing restrictions. Thus, increasing speed always leads to a wider area. Depending on the throughput demands of the application, different multiplier structures will yield different levels of efficiency. The best

circuit structure is chosen as the initial step in the design process. From straightforward serial multipliers to intricate parallel multipliers, there are many different structures available to carry out the multiplication function. By optimising circuit sizes and the voltage supply, any multiplier speed increase will increase the operational frequency of the digital signal processors or can be exchanged for energy. The widely used Wallace tree multiplier performs faster because to the redesigned architecture. The structural optimization of the traditional Wallace multiplier results in a significant decrease in the latency of the entire circuit. Essentially multiplying two unsigned numbers, the Wallace tree. An AND array for computing the partial products, a carry save adder for adding the resulting partial products, and a carry save multiplier make up the traditional Wallace tree multiplier architecture. By optimising circuit sizes and the voltage supply, any multiplier speed increase will increase the operational frequency of the digital signal processors or can be exchanged for energy. The widely used Wallace tree multiplier performs faster because to the redesigned architecture. The structural optimization of the traditional Wallace multiplier results in a significant decrease in the latency of the entire circuit. Essentially multiplying two unsigned numbers, the Wallace tree. The carry save adder adds the partially computed products, the carry propagate adder completes the addition process, and the typical Wallace tree multiplier architecture uses an AND array to compute the partial products.

WALLACE TREE MULTIPLIER

The multiplier determines the system's overall performance and is the main component of the electrical gadget. A tremendous amount of power and delay are produced when creating a multiplier. Compressors and adders are employed to lessen these drawbacks. Therefore, one of the key goals of improving the performance of digital systems like DSP processors has been to reduce multiplier delay. Therefore, multipliers are the subject of numerous attempts to accelerate it. It is a Wallace tree that multiplies two numbers and reduces the number of partial products; it is an efficient hardware implementation of a digital system. Multiple multiplications are carried out in vector processors to achieve data or loop level parallelism. The main benefits of this multiplier are its quick processing and low power requirements. Compressors and adders are employed to lessen these drawbacks. Therefore, one of the key goals of improving the performance of digital systems like DSP processors has been to reduce multiplier delay. Therefore, multipliers are the subject of numerous attempts to accelerate it. It is a Wallace tree that multiplies two numbers and reduces the number of partial products; it is an efficient hardware implementation of a digital system. Multiple multiplications are carried out in vector processors to achieve data or loop level parallelism. The main benefits of this multiplier are its quick processing and low power requirements. These limitations are lessened by the use of compressors and adders. Reducing multiplier delay has thus been one of the main objectives of enhancing the performance of digital systems like DSP processors. Consequently, multipliers are the focus of several initiatives to speed it up. It is an effective hardware implementation of a digital system that uses a Wallace tree to multiply two values while lowering the number of partial products. In order to achieve data or loop level parallelism, vector processors do multiple multiplications. This multiplier's rapid processing speed and minimal power requirements are its key advantages.

KOGGE STONE ADDER

The kogge-stone adder was a notion for an effective and high-performance adder that was introduced in 1973 by Peter M. Kogge and Harold S. Stone. Essentially, it is a parallel prefix adder. Based on design time, this type of adder excels at providing the quickest addition. The propagate signals "Pi" and produce signals "Gi" are calculated using the I th bit of the input. Similar to how they generate signals, they also produce and carry signals. Consequently, by reducing the computation delay. It functions basically as a parallel prefix adder. This kind of adder excels in providing the quickest addition based on design time. Using the I th bit of the input, the propagate signals "Pi" and generate signals "Gi" are calculated. They produce and carry signals in a manner similar to how they generate signals. Thus, by shortening the computation delay.

Three categories are used to classify prefix adders.

A. Pre-processing

B. Carry Generation

C. Final Processing

PARALLEL PREFIX ADDER

Parallel Prefix adder: "The Parallel prefix adder employs the three-stage structure of the CLA adder". The improvement is in the carry generation stage, which is most intensive.

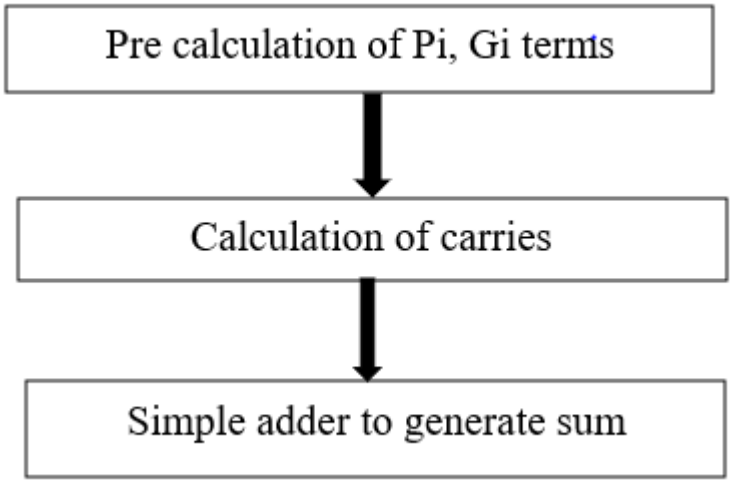

Fig.1: Parallel prefix adder

The three phases are listed below.
Stage 1: Precalculation of the terms for propagation (pi) and generation (gi)
Stage 2: Carry terms calculations. Time-saving parallel processing
Stage 3: an adder to produce the total

Stage 1: Propagation, generation terms, and partial sum are included in Stage 1.
$p(i) = a(i) + b(i)$ $g(i) = a(i) \cdot g(i)$ $psum(i) = a(i) \oplus b(i)$

Stage 2: Carry terms calculations. Time-saving parallel processing (Carry generation stage):
$P[i:j] = P[i:k] \cdot P[k-1:j]$, if $n \geq i > j \geq 1$
$G[i:j] = G[i:k] + (P[i:k] \cdot G[k-1:j])$, if $n \geq i > j \geq 1$
Where n = no. of bits

Stag 3: an adder to produce the total the final stage
$c(i) = G[i:1]$ $Sum(i) = psum(i) \oplus c(i-1)$

IMPLEMENTATION

Utilizing Xilinx ISE 14.1 software and the VHDL programming language, the approach took Spartan -6 devices into consideration. Xilinx ISE 14.1 software and the VHDL programming language were used for the implementation, which took Spartan -6 devices into consideration.

The multipliers used are:
1) Wallace multiplier – 4bit, 8bit, 16bit
2) Wallace multiplier with Sklansky adder – 8bit, 16bit
3) Wallace multiplier with Kogge-Stone adder – 8bit, 16bit
4) Reduced Complexity Wallace multiplier with Sklansky adder – 8bit, 16bit
5) Reduced Complexity Wallace multiplier – 4bit, 8bit, 16bit
6) Reduced Complexity Wallace multiplier with Kogge-Stone adder – 8bit, 16bit.

EXPERIMENTAL RESULTS

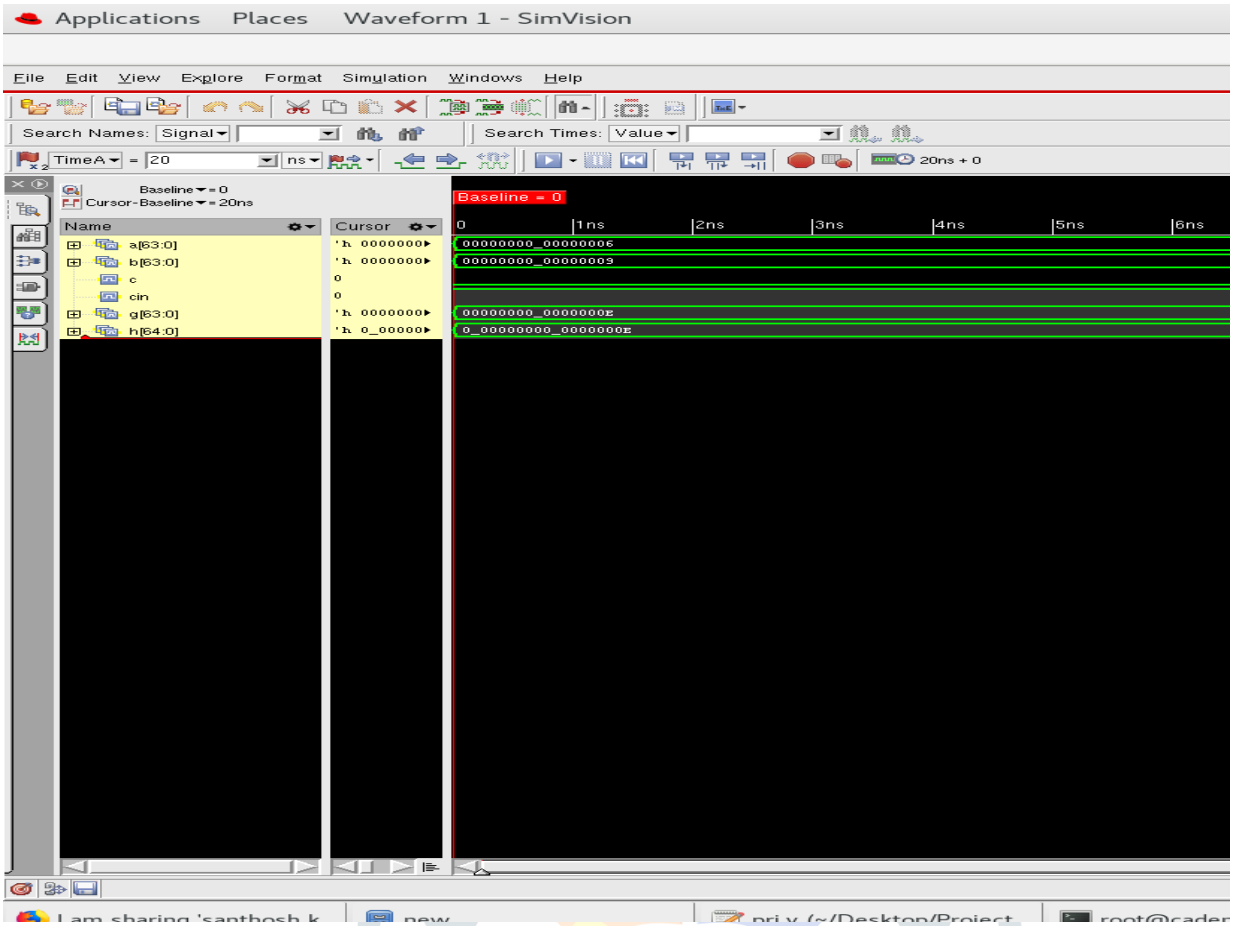

Fig.1.Waveform

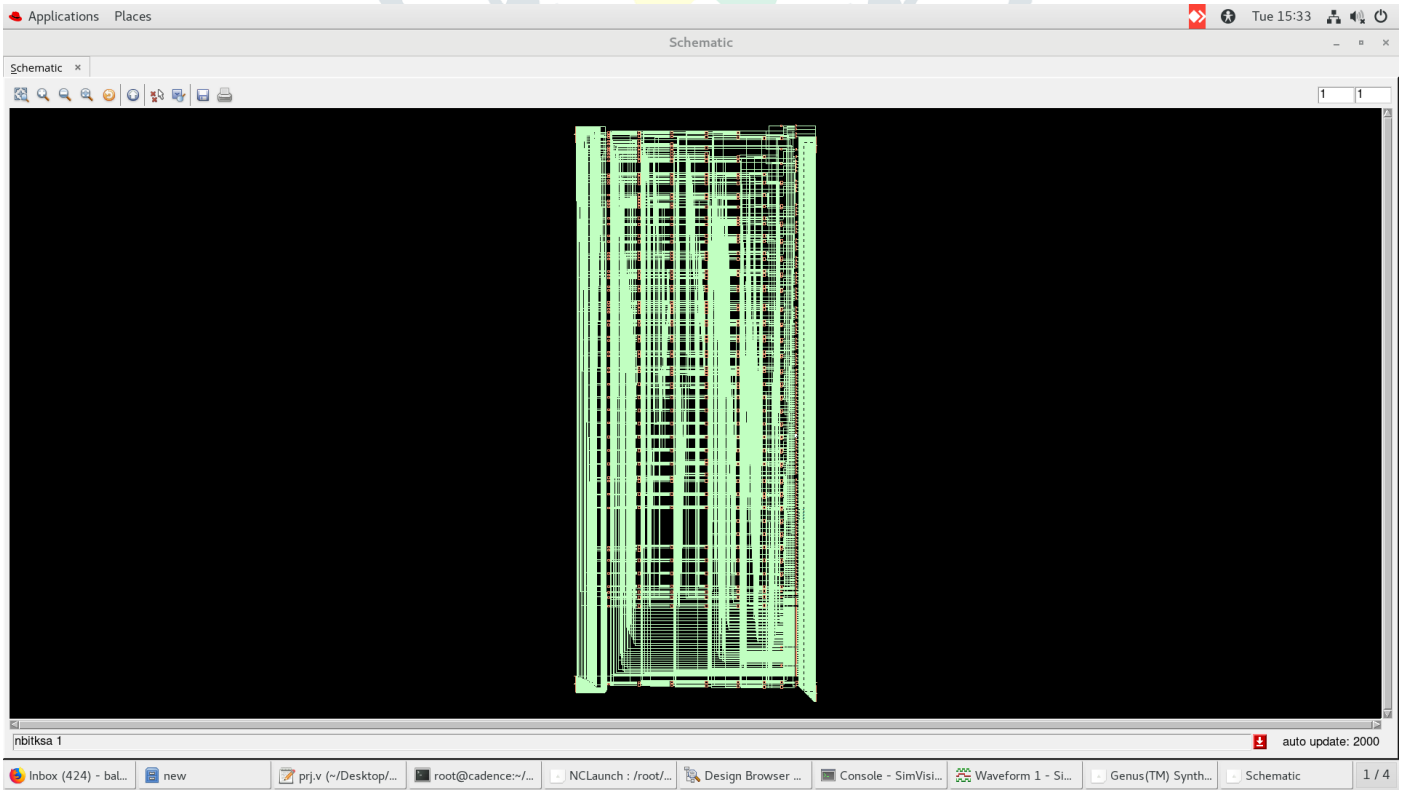

Fig.2.RTL Schematic

APPLICATIONS

The suggested Wallace tree structure offers reductions in power dissipation of around 70%, power delay product of about 86 percent, and area of about 60%. The suggested multiplier can be used in a variety of high-speed, low-power arithmetic applications, including DSP structures and ALUs. Power dissipation, power delay product, and area can all be reduced by roughly 70%, 86 percent, and 60%, respectively, using the Wallace tree topology that has been presented. The suggested multiplier can be used in a variety of low power and high-speed arithmetic applications, including DSP structures, ALUs, and several more.

ADVANTAGES

• Wallace multiplication has a very short delay compared to standard multiplication.

• The Wallace multiplier uses very little power.

• Speed is extremely rapid; hence, delay and power are inversely related.

DISADVANTAGES

Wallace tree multipliers consume a significant number of gates due to their high memory occupancy. A Wallace tree is an effective implementation of a digital circuit Wallace, an Australian computer scientist, developed to multiply two numbers. Wallace tree multipliers use a significant amount of gates because memory usage is very high. A digital circuit for multiplying two integers, developed by an Australian computer scientist, is efficiently implemented using a Wallace tree.

CONCLUSION

In this work, an effective Wallace tree multiplier design was used. With a total power dissipation of 155.532mW, the entire device operates at a frequency of 215MHz s. Since 32-bit multiplication has a shorter delay, it can be employed in systems that demand high processing performance for operations requiring several bits. XILINX ISE 12.3i is used to verify the Multiplication's functioning, and XILINX synthesiser is used to create it. We used the design of an effective Wallace tree multiplier. The entire unit operates at a frequency of 215MHz, dissipating a total of 155.532mW of electricity. Due to the reduced delay of 32-bit multiplication, this design can be employed in systems that demand excellent processor performance for operations requiring several bits. Utilizing XILINX ISE 12.3i and XILINX synthesiser, the Multiplication's functionality is tested.

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