JETIR.ORG ISSN: 2349-5162 | ESTD Year : 2014 | Monthly Issue
JOURNAL OF EMERGING TECHNOLOGIES AND INNOVATIVE RESEARCH (JETIR)
An International Scholarly Open Access, Peer-reviewed, Refereed Journal

DESIGN OF IMPRECISE MULTIPLIER USING DUAL STAGE COMPRESSOR WITH REVERSIBLE LOGIC

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Abstract– This paper proposes the Imprecise multiplier using Dual stage Compressor with reversable logic. The proposed dual stage compressor has universal gates which helps in reducing the area and power. An 8×8 multiplier is implemented in this paper. This multiplier is designed using Dual stage 4:2 Compressors in the Partial product accumulation stage and Parallel Prefix Adder in the final partial product addition stage. Using reversable logic gates helps in increasing the performance of the multiplier. The Dual stage 4:2 compressors have universal gates which decrease the area and power. Parallel prefix Adder decreases the delay in the final partial product addition. The proposed multiplier is measured in terms of area, delay and power. The effectiveness of the proposed method is synthesized and simulated using Xilinx Vivado 2018.3.

Index terms: **Wallace multiplier, Dual stage compressor, Parallel prefix adder, Reversable logic.**

1. INTRODUCTION

In majority of signal processing applications use convolutional units as their computationally expensive and performance-determining operational units. Multipliers greatly contribute to the size, delay, and power of convolutional units, where adders and multipliers are primarily used. The operation of multiplication is divided into three stages

1) Partial products generation

2) Accumulation of Partial products

3) Addition of final partial product

Wallace [1] has made a significant contribution toward accumulation stage delay-optimized architectures. By using compressors rather than full adders and half adders, accumulation phase delay is further decreased. The 4:2 compressor is the most popular compressor topology because, in contrast to topologies like the 5:3, 7:2, and others, it can create regularly structured designs. In recent years, in order to realise area and power optimised designs for error tolerant applications like multimedia processing, neural networks, and signal processing, multipliers are extensively studied in the context of approximation. Such optimizations are currently being studied for CMOS, FPGA, and pass transistor-based multiplier realisations.

1.1 REVERSABLE LOGIC

A n × n gate is referred to as reversible if there is a bijective mapping between the n input and n output combinations. The reversible logic gates NOT, Toffoli, Feynman, Fredkin, Peres, and BJN are employed in this work. Below is a basic explanation of the gates.

NOT gate -a one-bit gate symbolised by NOT. The output negates the input. Its QC is one.

Feynman gate [2]- a two-bit gate represented by FYG. The Feynman gate's output is (A, A B) when input (A, B) is present. QC for FYG is 1.

Toffoli gate [3]- a three-bit gate represented by TG. The Toffoli gate's output is (A, B, AB ⊕ C) when input is (A, B, C). QC for TG is 5.

Fredkin gate [4]- a three-bit gate represented by FRG. The Fredkin gate's output is (A, AB ⊕ AC, AB ⊕ AC), when input is (A, B, C). QC for FRG is 5.

BJN gate [5] - a three-bit gate in which an output (A, B, (A+B) ⊕ C) is produced for combination (A, B, C) s the input and QC of BJN is 5.

Peres gate [6] - a three-bit gate represented as PG. The Peres gate's output is (A, A ⊕ B, AB ⊕ C), when input is (A, B, C). QC for PG is 4.

An optimal reversible circuit synthesis should make use of the fewest possible ancilla inputs, garbage outputs, gates count, and quantum costs. Below is a presentation of the basic computational unit's reversible logic realisation.

Half Adder

Half adders, which have two inputs (HAIN1 and HAIN2) and two outputs (HASUM and HACARRY), which is used to calculate the sum of two bits. Below is a list of the expressions for HASUM and HACARRY.

$$HASUM = HAIN1 \oplus HAIN2$$

$$HACARRY = HAIN1 \cdot HAIN2$$

As seen in Figure 1, a half adder is implemented using reversible logic gates. One ancilla input and one garbage output are employed in a Peres gate.

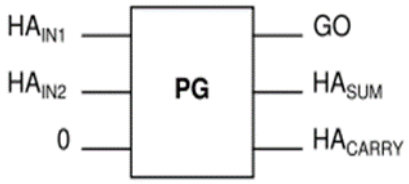

Figure 1: Half adder using Reversible Logic

Full Adder

A full adder is employed to determine the sum of three bits in Figure 2. FAIN1, FAIN2, and FACIN are the three inputs and two outputs of the full adder are FASUM and FACARRY. FASUM and FACARRY can be expressed below

$$FASUM = FAIN1 \oplus FAIN2 \oplus FACIN$$

$$FACARRY = (FAIN1 \oplus FAIN2) \cdot FACIN + FAIN1 \cdot FAIN2$$

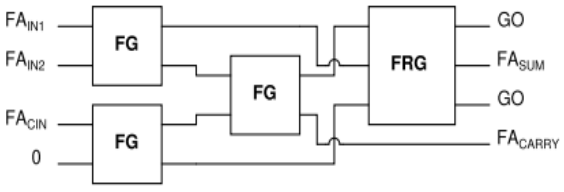

Figure 2: Full adder using Reversible Logic

2. LITERATURE SURVEY

H. Thapliyal et al. [7] discussed the primary design's emphasis on minimising the amount of garbage outputs and reversible gates. New reversible sequential circuit designs that are optimised for quantum cost, delay, and garbage outputs. Selecting a reversible gate carefully to implement a specific logic function is part of the design process for reversible gates. These reversible sequential latches perform better than other designs in terms of garbage outputs, delay, and quantum cost.

A. Momeni et al. [8] discussed how approximate computing is an appropriate paradigm for digital processing at nanometric scales. In this essay, the analysis and design of two brand-new, approximate 4-to-2 compressors for use in a multiplier are discussed. A Dadda multiplier is presented and examined using four alternative utilisation techniques for the proposed approximation compressors. In comparison to an exact design, the results demonstrate that the designs significantly reduce power dissipation, delay, and transistor count. A new paradigm for computation at the nanoscale is approximate computing.

P. J. Edavoor et al. [9] discussed about the high-speed multimedia and have opened up a completely new field for high-speed error-tolerant circuits with approximation computation. High performance is provided by these applications, but accuracy is sacrificed. Additionally, such approaches reduce power consumption, latency, and system architectural complexity. This study investigates the design and analysis of two approximation compressors that, when compared to current architectures, have reduced area, latency, and power while maintaining comparable accuracy.

J. Pujar et al. [10] discussed about the typical digital systems lose information because bits are erased during logic operations, which results in a significant amount of energy/power loss. Reversible calculations preserve bits at the output, balancing out any information loss. In this paper, a Feynman gate and a Fredkin gate-based energy-efficient low power reversible complete adder is developed. The study and calculation of energy dissipation in reversible circuits are proposed in this paper. By cascading three Feynman gates and one Fredkin gate, the construction of a reversible complete adder is suggested in this paper.

A. G. M. Strollo et al. [11] discussed the approximate multipliers, in the scientific literature that suggests numerous circuits built with about 4-2 compressors. The thorough analysis and comparison of the approximately 4–2 compressors that have been suggested in the literature. In order to investigate a total of twelve different approximate 4-2 compressors, we also propose a novel approximate compressor. This research presents a thorough analysis and comparison of previously proposed approximate 4-2 compressors. This allows us to deduce the key feature of the previously proposed approximate 4-2 compressors, and we have created a new approximate 4-2 compressor.

Sithara Raveendran et al. [12] discussed about the 8×8 Wallace multiplier using exact and inexact compressors using reversable logic gates. By maximising the reversible logic realisation parameters GC, QC, GO, and AI, a novel design for an inexact 4:2 compressor that can be implemented using reversible logic is created. The effectiveness of the presented inexact compressor-based Baugh-Wooley Wallace tree multiplier in image processing and CNN-based applications is verified. The more details of this paper is discussed in below existing method.

3. EXISTING METHOD

In this method, eight exact 4:2 compressors, eight inexact 4:2 compressors, five full adders and twenty three half adders are used. The details of the reversable Exact 4:2 compressor and the Inexact 4:2 compressor is show below

Exact 4:2 Compressor

The reversible logic realization of an exact compressor is presented in Figure 3 and has four Feynman gates, one NOT gate, two BJN gates and four Peres gates with eight AI and nine GO.

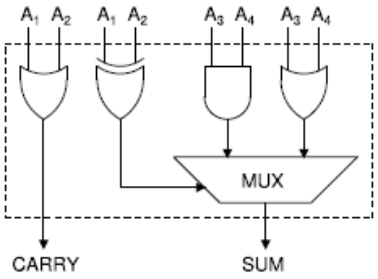

Figure 3: Exact 4: 2 compressor

Inexact 4: 2 Compressor [12]

Using reversible logic gates, Figure 4 illustrates the circuit realisation of the proposed inexact 4:2 compressor. With three BJN gates, three Peres gates, six AI gates, and eight GO gates, the proposed 4:2 inexact compressor has twelve gates in total. An 8x8 multiplier is created below utilising these adders and compressors with reversible logic.

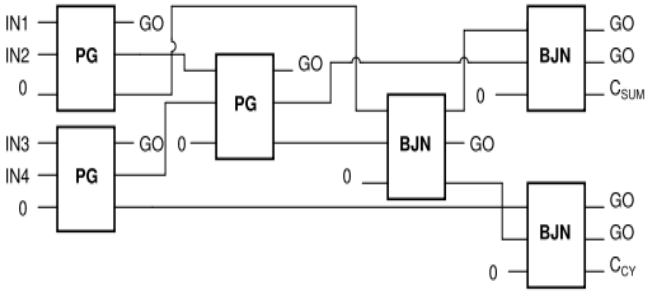

Figure 4: Inexact 4: 2 compressor

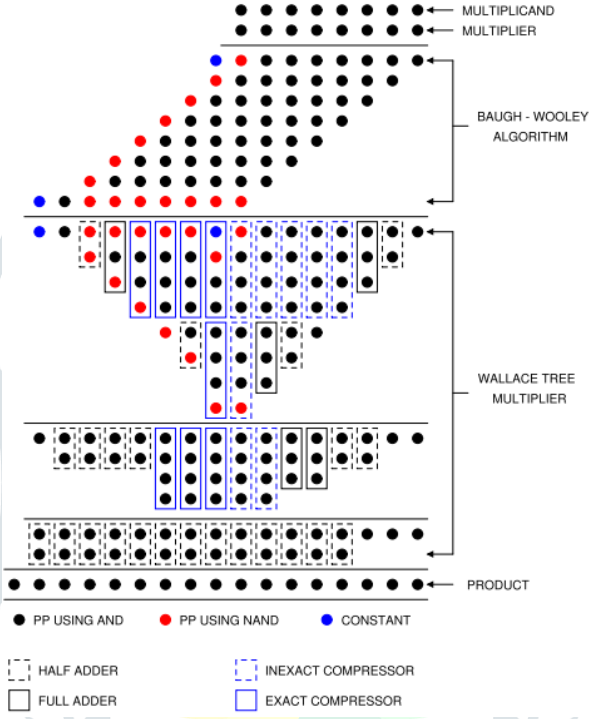

Figure 5: Inexact 8×8 multiplier using Inexact 4:2 compressor

In the existing method, the area, delay and power are more compared to the proposed method. The implementation and details of the proposed method is discussed below.

4. PROPOSED METHOD

In the proposed method the Inexact 4:2 compressors are replaced with the Dual stage 4:2 compressor. Using half adders, full adders and the Dual stage 4:2 compressors the 8×8 multiplier is designed. The details of the Dual stage 4:2 compressors are as shown below

Dual stage 4:2 Compressor [13]

In the Dual stage 4:2 compressor the universal gates are used which helps in reducing the area of the circuit. The schematic of Dual stage 4:2 multiplier is shown in fig 6. The reversable logic Dual stage 4:2 compressor is shown in the fig 7. Multiplier designed using this Dual stage compressor reduced the area compared to the multiplier designed using Inexact compressor.

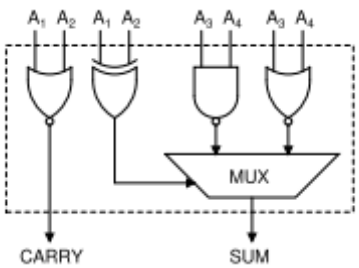

Figure 6: Dual stage 4: 2 compressor

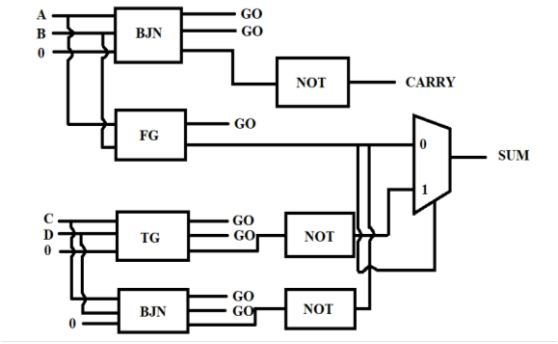

Figure 7: Reversable logic Dual stage 4: 2 compressor.

The Dual stage 4:2 compressors consist of two BJN gates, two FG gates, three NOT gates and a multiplexer. The structure of 8×8 multiplier using Dual stage 4:2 compressor is shown in the fig 8. In the multiplication for the reduction of 2 partial products half adder is used, for the reduction of 3 partial products full adder is used and for the reduction of 4 partial products Dual stage 4:2 compressor is used in the design. In the final partial product parallel prefix adder is used which reduces the delay of the partial product reduction.

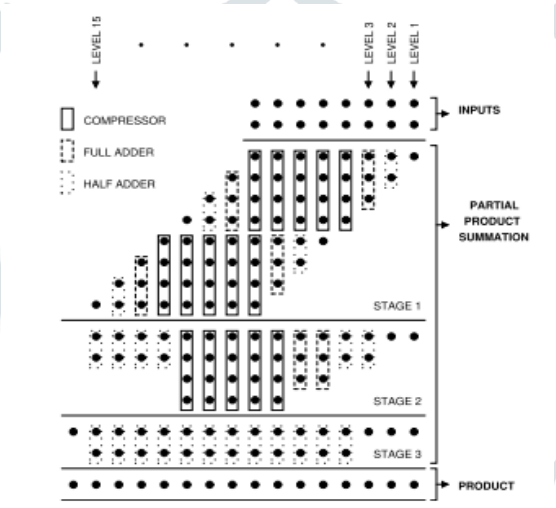

Figure 8: 8×8 multiplier using Dual stage 4:2 compressor

The design of the multiplier is done in the proposed method. The area and power is reduced by replacing with the dual stage compressor, delay is reduced by replacing the carry propagating adder with the parallel prefix adder. The results of the proposed multiplier is shown below.

RESULTS

The simulation and synthesis results of the proposed multiplier are as below. The simulation of the proposed multiplier is shown in Figure 9. The area utilization of the proposed multiplier is shown in Figure 10. The delay of the multiplier is shown in Figure 11 and the Power of the proposed multiplier is shown in Figure 12.

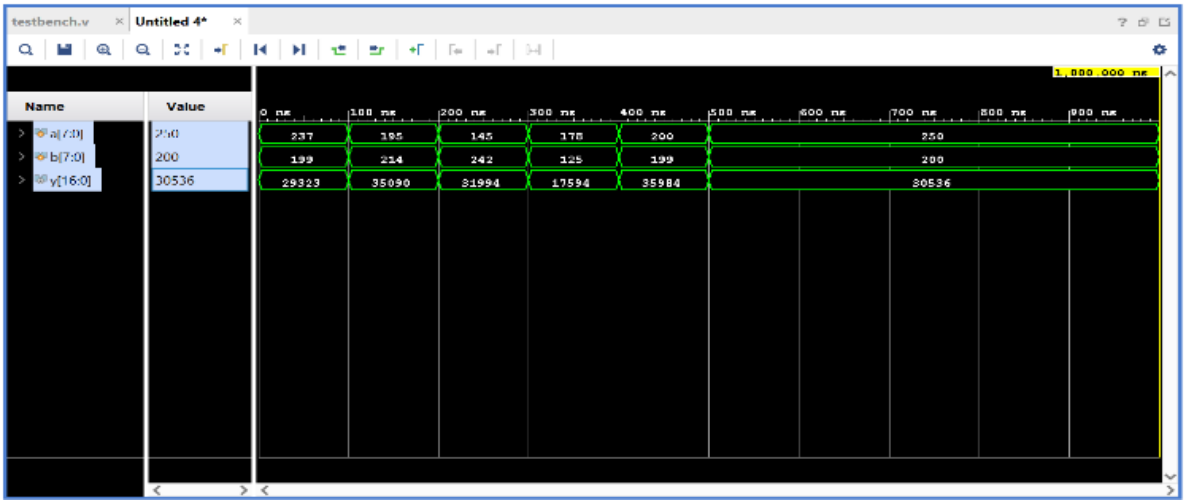

Figure 9: Simulation result of Proposed 8×8 multiplier using Dual stage 4:2 compressor

Resource	Utilization	Available	Utilization %
LUT	82	20800	0.39
IO	33	106	31.13

Figure 10: Area Utilization of Proposed 8×8 multiplier

```
Max Delay Paths
--------------------------------------------------------------------------------
Slack:                  inf
  Source:               b[6]
                          (input port)
  Destination:          y[12]
                          (output port)
  Path Group:           (none)
  Path Type:            Max at Slow Process Corner
  Data Path Delay:      9.490ns  (logic 4.252ns (44.803%)  route 5.238ns (55.197%))
  Logic Levels:         8  (IBUF=1 LUT2=2 LUT5=1 LUT6=3 OBUF=1)
```

Figure 11: Delay of Proposed 8×8 multiplier

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**13.876 W (Junction temp exceeded!)**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**94.4°C**
Thermal Margin:	-9.4°C (-1.8 W)
Effective ϑJA:	5.0°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Figure 12: Power of Proposed 8×8 multiplier

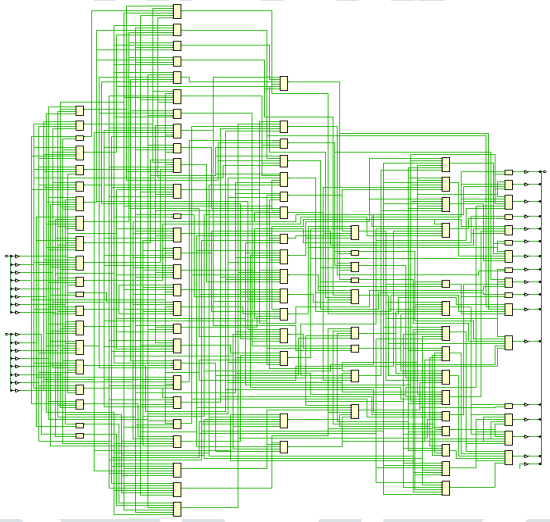

Figure 13: Technology Schematic

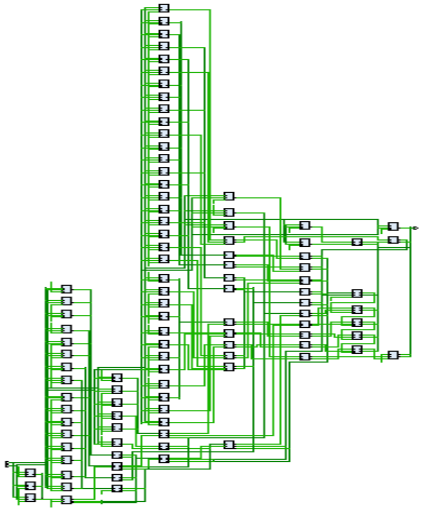

Figure 14: RTL Schematic

TYPE	AREA	DELAY	POWER
EXISTING SYSTEM [12]	LUT - 84/20080	10.502ns	14.893W
PROPOSED SYSTEM	LUT - 82/20080	9.490ns	13.876W

Figure 15: Comparison table of existing and Proposed 8×8 multiplier

From the comparison table of the existing and the proposed system, the area of the proposed multiplier is less. The delay of the proposed multiplier is less and the power of the proposed multiplier is less.

CONCLUSION

In this paper, the multiplier designed using inexact 4:2 compressor is modified by replacing inexact 4:2 compressor with Dual stage 4:2 compressor which consists of universal gates. By using parallel prefix adder at the final partial product addition, we can reduce the delay and by using universal gate-based compressor we can reduce hardware complexity. The reversable logic gates increase the performance of the multiplier. From the experimental analysis, it can be concluded that the proposed design is able to achieve the best optimization in scales area, delay and power.

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