JETIR.ORG ISSN: 2349-5162 | ESTD Year : 2014 | Monthly Issue
JOURNAL OF EMERGING TECHNOLOGIES AND INNOVATIVE RESEARCH (JETIR)
An International Scholarly Open Access, Peer-reviewed, Refereed Journal

THD MITIGATION IN THE PV SYSTEM BY USING A CASCADED MULTILEVEL INVERTER BY THE ANN TECHNIQUE

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Abstract: ***The presence of harmonics in solar Photo Voltaic (PV) energy conversion systems results in the deterioration of power quality. To address such an issue, this paper aims to investigate the elimination of harmonics in a solar-fed cascaded Multilevel inverter with aid of Proportional Integral (PI), Artificial Neural Network (ANN) based controllers. The inverter can have a significant impact on the overall performance of the CMLI, including maximum power point (MPP) tracking, total harmonic distortion (THD), and efficiency. Multilevel inverters are one of the most promising classes of converters that offer a low THD. In this paper, we propose a new multilevel inverter topology with the motivation to improve all three aforementioned aspects of performance. The proposed topology is controlled through ANN, which is state-of-the-art in control techniques. We compare the performance of the proposed topology with the topologies reported in the literature. The proposed topology offers one of the best efficiency, MPP tracking, and voltage THD. At full load, the standalone system successfully delivers 97.21% of the theoretical maximum power. Additionally, CC is incorporated to mitigate voltage spikes at the output when supplying power to inductive loads. It successfully eliminates the spikes and also reduces the total harmonic distortion (THD) of output current and voltage from more than 10% to less than 5%, as recommended in IEEE 519 standard.***

Index Terms: Multi-level inverter, photovoltaic (PV) system, maximum power point, voltage regulator, capacitor compensator (CC).

I. INTRODUCTION

Renewable energy sources receive increased attention due to the initiatives towards increasing the capacity of renewable energy production [1], and reducing the dependency on fossil fuels that will cause the ennmental pollution and climate change in the long run [2]. Since photovoltaic (PV) energy is clean, environmentally friendly, readily available and free to harvest, it has become one of the most common types of renewable energy source in both residential and industrial areas [3]. It is used in a variety of applications such as water pumping system, battery charging station, solar vehicles and standalone system for off-grid applications [4]-[7]. The real-time application of an off-grid PV energy system consists of PV panels, DC-DC converter, DC-AC inverter and load [8]. However, the output of a PV panel is not constant since it depends significantly on solar irradiation and temperature [9]. Maximum power point tracking (MPPT) algorithm can be implemented to harvest peak energy from PV panels [10]. The DC-DC converter is a necessary element when MPPT is to be considered since it works by continuous duty cycle adjustment [11], [12]. Considering the necessity of employing DC-AC inverter in a PV system, multi-level inverter (MLI) is preferable nowadays compared to the conventional voltage source inverter (VSI) due to its capability to produce power quality with minimal error [13]. Traditional MLIs such as neutral point clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB) possess one common drawback, which is the massive amount of components required [14]. The number of devices is also directly related to the number of MLI level, which in turn causes the overall system to be costly, bulky and complex [15]. Researchers have been working to reduce the number of required devices. Several reduced switch MLIs have been proposed in the literature with their own merits and demerits [16], [17]. MLI can be divided into isolated or non-isolated DC source. Isolated MLI implements separate DC sources, while non-isolated MLI requires only a single source [15]. Isolated MLI is further categorized into symmetrical or asymmetrical source configuration. Symmetrical configuration uses equal voltage for each DC source, while asymmetrical configuration uses different values for the DC sources either by the binary or trinary methods [14]. Some MLI topologies proposed in [18] can work in both ways. Asymmetrical source configuration is a better choice in a PV system, especially in a low- to medium-voltage application since the number of PV modules Npv required can be optimized. For instance, most binary sources based asymmetrical MLI can produce up to 2 Npv + 1 –1 output levels compared to only 2Npv + 1 output levels when using symmetrical sources. A lot of emerging MLIs use H-bridge as a polarity generator. Such topologies are not suitable for high-voltage applications since the voltage stress at the H-bridge can be very high [19]. Isolated MLI is ideal for PV integration since separate PV panels can be directly used as independent sources. In non-isolated MLI

such as NPC and FC, voltage balancing of capacitors might be a challenge [20]. Multi-level DC-link (MLDCL) inverter is one of the most commonly-used reduced switch MLI [21]. It uses a significantly lower number of switches than traditional MLI. Further reduction in the switch can be realized by removing one switch from each stage and replacing it with diodes. This configuration is suitable for low-voltage applications [17]. However, voltage spikes will be introduced by the replacement at the output under inductive loads [22]. The presence of these voltage spikes will cause several power quality problems such as over-voltage, distorted current waveform and a significant increase in total harmonic distortion (THD). Some literature limits the operation of such configuration based on an acceptable power factor range at which the voltage spikes produced on the output are minimal [23]. In [24], only resistive loads are used to avoid the production of voltage spike. To use PV as the input to an inverter, it is compulsory to have a voltage control technique for producing constant DC voltage. For a standalone system, the proportional-integral (PI) controller can be implemented to adjust the duty cycle of a DC-DC converter by taking the output of the converter and comparing it with the desired reference value [25]. However, the PI controller does not consider MPPT, and it is not possible to control the same DC-DC converter using both MPPT algorithm and PI controller. Several methods have been proposed to tackle this issue in a standalone PV system. One of them is implementing artificial intelligence (AI) such as fuzzy, particle swarm optimization (PSO) and genetic algorithm (GA) to auto-tune the PI controller for voltage regulation [26], [27]. Another proposed method is cascading two DC-DC converters, one for MPPT and the other for voltage regulation [28]. In some literatures, MLDCL inverter is typically implemented with MPPT. However, the DC-link control is not considered, and the outputs are controlled by the load [24], or under constant input irradiance and temperature [29]. In this paper, the design of standalone PV system using 31-level asymmetrical switch-diode based MLDCL inverter integrated with proposed Incremental conductance (INC) based voltage regulator (INCVR) and capacitor compensator (CC) is presented. Due to the feasibility of using isolated MLI in a PV system, the MLDCL topology is an excellent choice due to its number of DC source with low ratio of voltage level. The proposed INCVR acts as the DC-link voltage controller. It does not require any PI controller and is capable of delivering maximum PV power even under varying irradiance, temperature and load conditions. Besides, it provides a wide range of voltage regulating capability and eliminates the need for different DC-DC converters under different operation conditions. From the literature review, there are little discussions on voltage control technique for the application of MLDCL in a standalone PV system. CC is also proposed to counter-measure the production of voltage spikes under inductive loads at the output, improving the THD significantly. Simulation is conducted to evaluate the proposed system under several conditions using MATLAB/Simulink.

II. MODELLING OF PROPOSED SYSTEM

A. PV Module and Boost DC-DC Converter

In this paper, a single diode model of PV module is used and modelled accurately for the simulation where shunt resistance RP and series resistance RS are taken into consideration. The boost converters are used to boost and regulate the PV voltages before feeding them to the MLDCL inverter. The diagram of a boost converter and its feedback mechanism used in each PV stage is shown in Fig. 1, where Cin and Cout are the input and output capacitors, respectively; Ipv and Vpv are the current and voltage of PV, respectively; and Verr, VDC , and Vref are the voltage error, the actual output voltage of the boost DC-DC converter, and the reference DC voltage, respectively. Cin is required to ensure continuous output from PV panel [30].

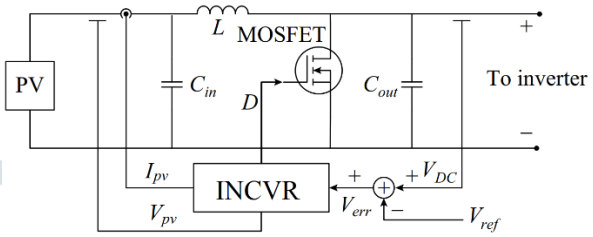


Fig. 1. Boost converter with PV source and proposed INCVR.

31-level Asymmetrical Switch-diode MLDCL Inverter

MLDCL inverter is a type of hybrid MLI inverter which consists of two stages. The first stage is the level generation part, where positive and zero voltage levels are generated to synthesize the waveform of stair-case output voltage. The second stage is the polarity generator part used to reproduce the second half-cycle of the generated waveform into negative levels. Figure 2 shows the circuit diagram of the 31-level asymmetric switch-diode based MLDCL inverter. For the asymmetrical operation of the MLDCL topology, it is more appropriate to use the binary source configuration where the voltage levels are determined by geometric progression (GP) with a factor of 2 [14]. Thus, in this paper, the voltage sources for the 31-level MLDCL are VDC, 2VDC, 4VDC, and 8VDC. The relationship can be given as:

$$\frac{V_{DC2}}{V_{DC1}} = \frac{V_{DC3}}{V_{DC2}} = \frac{V_{DC(n)}}{V_{DC(n-1)}} = 2$$

It is important to analyse the voltage across the switches and the peak inverse voltage VPIV of the diodes in order to select the most suitable components to be used. Selected devices for the implementation should have the maximum blocking voltage VB and VPIV rating higher than the blocking voltage and VPIV measured. The blocking voltages of all the switches and PIV of all the diodes in this topology are given by:

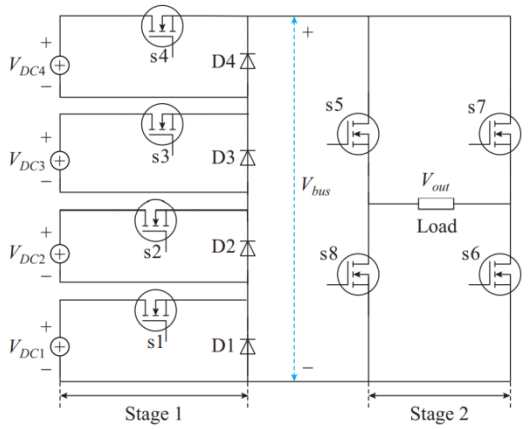


Fig. 2. Topology of 31-level switch-diode based MLDCL inverter.

$$V_{B,s1} = V_{PIV,D1} = V_{DC}$$

$$V_{B,s2} = V_{PIV,D2} = 2V_{DC}$$

$$V_{B,s3} = V_{PIV,D3} = 4V_{DC}$$

$$V_{B,s4} = V_{PIV,D4} = 8V_{DC}$$

$$V_{B,s5} = V_{B,s6} = V_{B,s7} = V_{B,s8} = 15V_{DC}$$

where VB,sn is the blocking voltage of switch; and VPIV,Dn is the PIV of each diode. On the other hand, the maximum current Im flowing through each switch or diode is the same as the load current ILoad, and it is zero when they are not conducting [31]. It can be given as:

$$I_{m,s1} = I_{m,D1} = \ldots = I_{m,sn} = I_{m,Dn} = I_{Load}$$

where Im,sn is the maximum current through the switch; and Im,Dn is the maximum current through the diode. Table I presents the switching states of the generation stage for the 31- level asymmetrical switch-diode MLDCL inverter. The switching states are the same for both half-cycles. The switching states at the polarity generation stage are given in Table II. The overview of the proposed standalone PV system is shown in Fig. 3, where PWM stands for pulse width modulation.

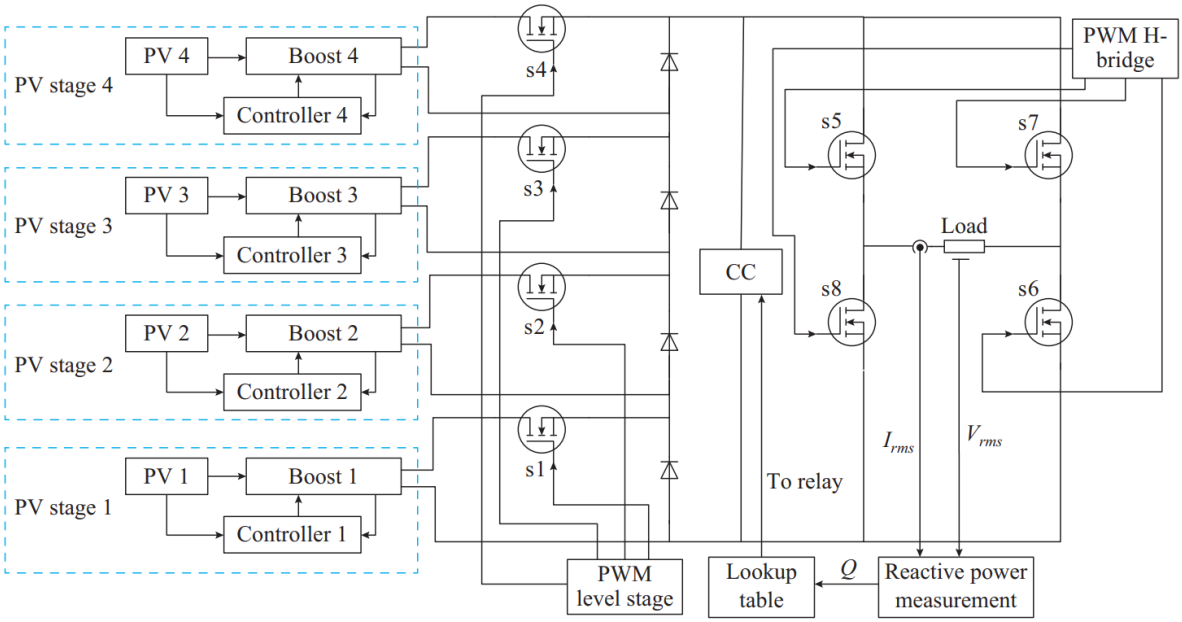


Fig. 3. Overview of proposed system and controller scheme.

Circuit of CC

At the inductive load, the output current of an inverter lags the output voltage by an angle α. During the time between 0 and α, the output power is negative. This phenomenon causes the voltage spikes in the output voltage waveform for the application of switch-diode based MLDCL topology as shown in Fig. 4. It can be observed that the voltage spikes are produced at the beginning of both positive and negative cycles of the voltage waveform during which the power is negative. If the power factor is lower, the value of α will be higher. Thus, wider voltage spikes will occur and further increase the THD of the AC output voltage.

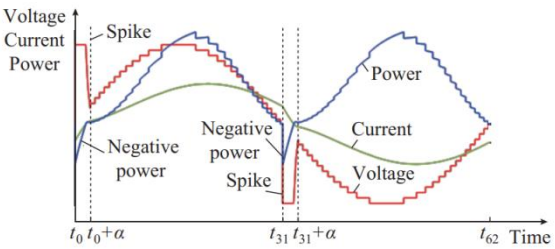


Fig. 4. Inductive load effect on MLDCL inverter.

To tackle this issue, a CC circuit is introduced as shown in Fig. 5. CC is placed between the first and second stage of the MLDCL inverter as depicted in Fig. 3. It operates by providing leading power factor components to compensate the lagging power factor components from the inductive loads.

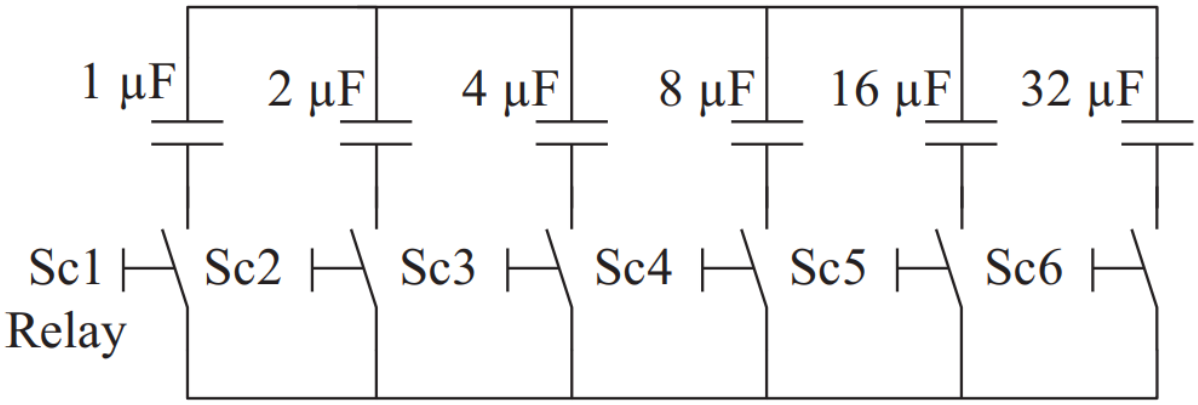


Fig. 5. Diagram of proposed CC circuit.

In this paper, CC consists of six capacitors connected in series by means of relays. Relays are used instead of switches to avoid additional power switches into the existing topology and it is suitable for the low-voltage application of the system. The value of compensating capacitors C can be chosen using the following equation:

$$C = \frac{Q_C}{2\pi f V^2}$$

where QC is the reactive output power; f is the output frequency; and V is the root mean square (RMS) value of output voltage.

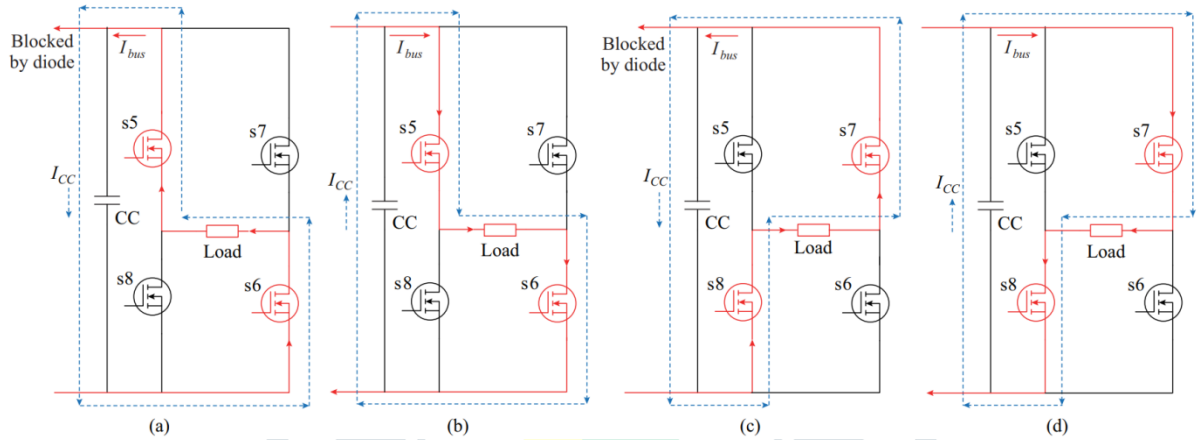


Fig. 6. Scheme of CC circuit operation. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4.

Control of CC Circuit

The proposed CC generally operates upon the value of reactive power for the inverter output. The RMS values of output voltage and current are measured to calculate the reactive power Q. The value of Q can be obtained as follows:

$$S = V_{rms} I_{rms}$$

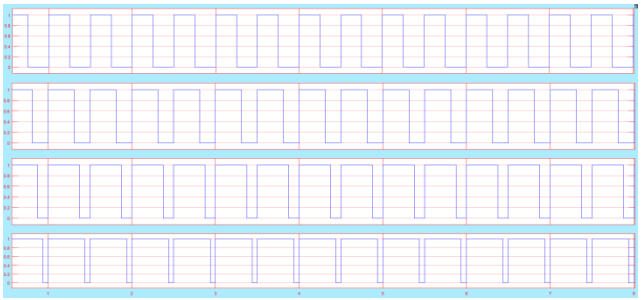
$$P = V_{rms} I_{rms} \cos\alpha = V_{rms} I_{rms} \cdot pf$$

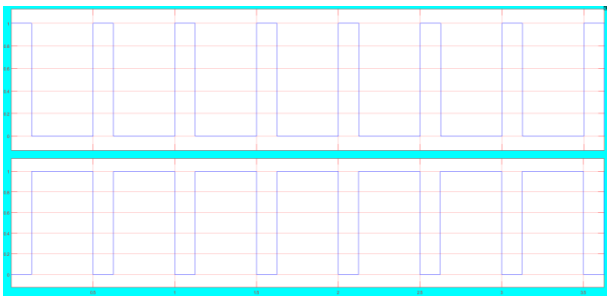
$$Q = \sqrt{S^2 - P^2}$$

where Vrms is the RMS value of output voltage; Irms is the RMS value of output current; and S is the apparent power. Next, from the obtained value of reactive power, a lookup table is used to control an appropriate combination of capacitors to be injected into the circuit by switching on/off the relay operation based on (8). All the control actions explained for CC operation can be implemented by using voltage sensor, current sensor and microcontrollers. For the purpose of simulation, a MATLAB/Simulink function block is used to control the relay action based on the lookup table. Digital signal processing (DSP) unit or similar controllers can be used if the control scheme is to be implemented experimentally.

PWM Technique

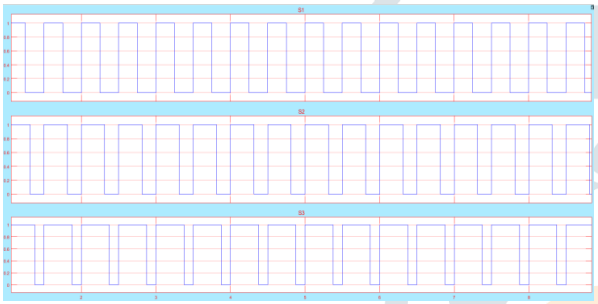
Similarly, like other MLI topologies, several PWM techniques can be implemented for the operation of reduced switch MLDCL inverter. The most popular PWM strategy is the carrier-based sinusoidal PWM. The only difference is the combination of the signals to be compared using relational operators in generating gate pulses. The combination can be determined from the switching states given in Table I and Table II. Besides, pre-determined switching angles or selective harmonic elimination (SHE) technique can also be used if the operation is to be implemented using a controller. Figure 9 demonstrates the generated switching signals for all the switches. the peak voltage of 325.27 V and the RMS value of output voltage of 230 V. The same switching frequency of 20 kHz is used in all boost converters.

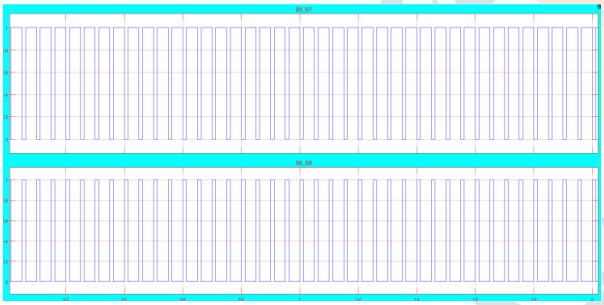




For 31 level PWM pulses

Fifteen level





III. ANN CONTROLLER

The brain learns essentially from experience[3]. It goes without saying that small energy-efficient packages will actually solve them outside the reach of existing computers. This brain modelling promises to also create computer solutions in a less technical way. The ANN consists of artificial neurons that interconnect. It is essentially a class of well-connected, very simple nonlinear elements which have the ability to learn[15]. ANN takes data samples to find solutions that saves time and resources instead of full data sets. Mathematical models for developing current data analytics technology are considered fairly simple ANNs.

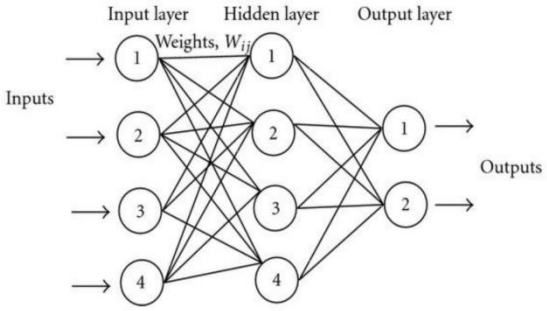


Figure 6. ANN structure

In the experiment, source voltage $vs(k)$ is first measured and compared with an estimated voltage $vfund_{est(k)}$. Note that k refers to the digital implementation sampling rate. E(k) is processed with an algorithm to change weight W or amplitude(coefficient) W_{11} and W_{21} of $\sin(k\omega\Delta t)$ and $\mathrm{Cos}(k\omega\Delta t)$) vectors as shown in equation (7).

The source voltage $vs(k)$ is calculated and compared with an approximate $vfund\_est(k)$ voltage (k). Notice that the constant k refers to the digital sampling rate. Here, e(k) error results in an algorithm that updates the sine sin (k ft) or cosine cos(k ft) vector by weight, as shown in the Equ (7) for weight W updates or amplitude W_{11} and W_{21}.

$$\mathrm{W(k+1)} = \mathrm{W(k)} + \left(\frac{\alpha e(k) Y(k)}{Y(k)^T Y(k)}\right)$$

Where, $W = \begin{bmatrix} W_{11} \\ W_{21} \end{bmatrix}$ is weight-factor, $Y = \begin{bmatrix} \sin(k\omega\Delta t) \\ Cos(k\omega\Delta t) \end{bmatrix}$ is fundamental sine and cosine components, $e(k) = vs(k) - vfund\_est(k)$ is the error among estimated and measured voltage signal, and α is learning rate.

At same time, W_{11} & W_{21} will be utilized to compute sudden magnitude $vfund\_est(k)$ of $vs(k)$ according to following approach.

$$vfund_{mag(k)} = \sqrt{W_{11}^2 + W_{21}^2}$$

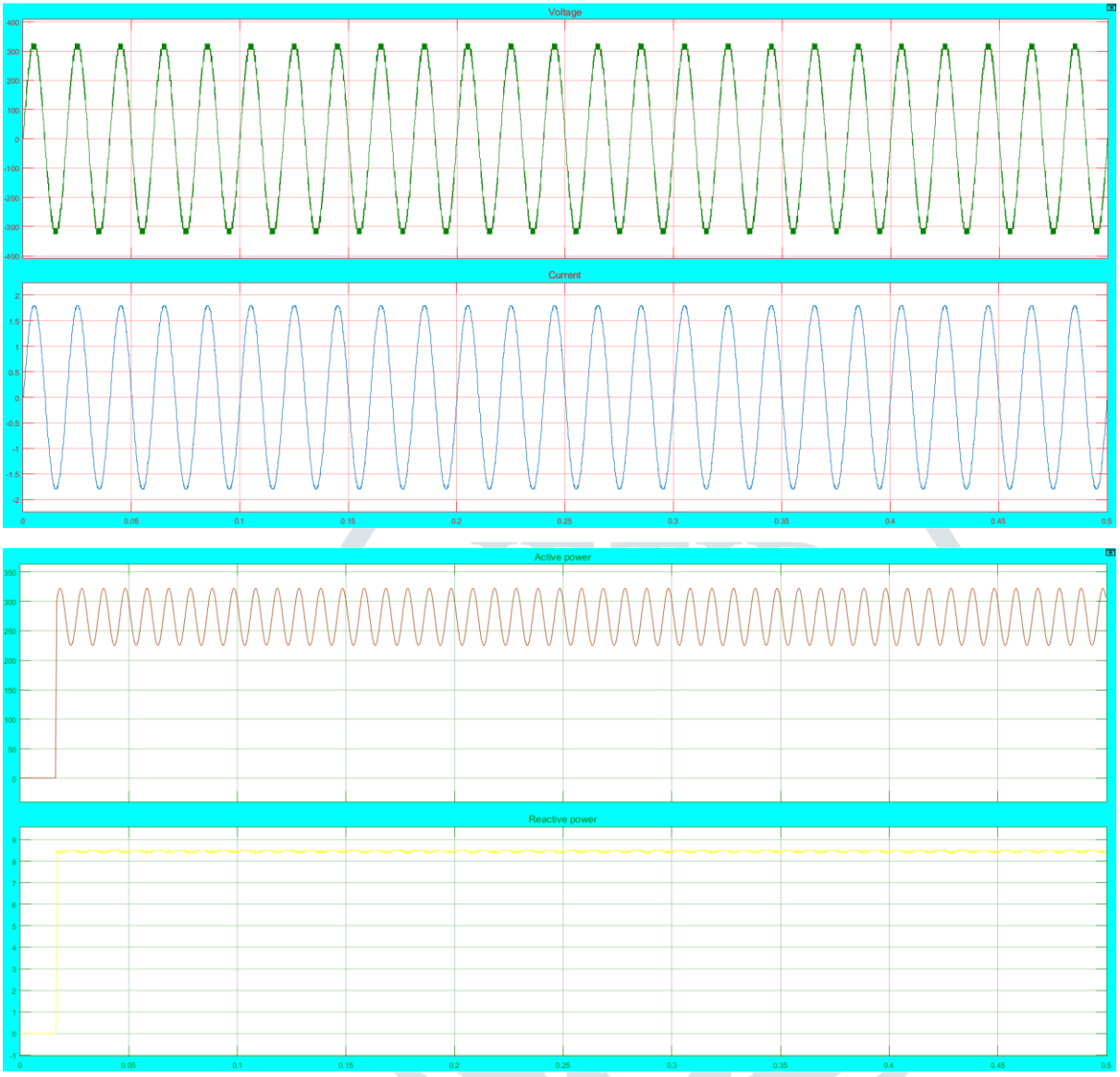
The iteration continues until $vfund_{est(k)} = vs(k)$ actual magnitude of the $vs(k)$ is twisted at this moment and finally divided between $vs(k)$ calculated to generate the desired synchronisation signal $\sin(k\omega\Delta t + \theta)$ please note that a unit representation of instant source voltage is the desired synchronisation signal generated in this way.

IV. RESULTS AND DISCUSSION

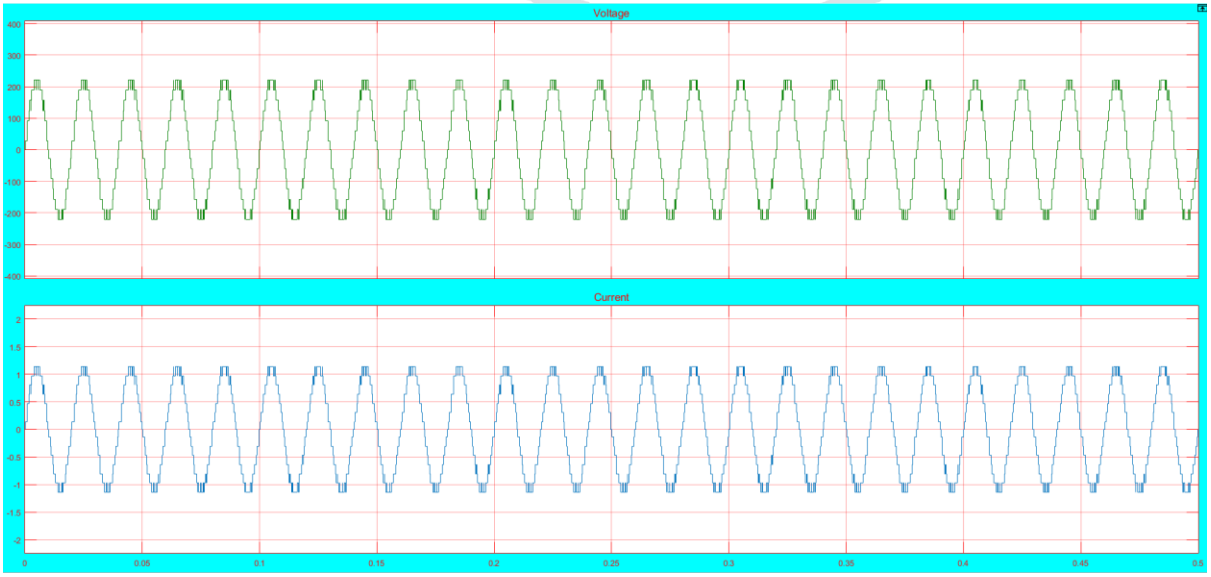
Resistive-inductive (RL) Load and CC Test The irradiance value of 800 W/m2 at the temperature of 31 o C is selected as the test condition. Several combinations of RL loads are chosen to produce different values of reactive power at the inverter output with power factor ranging above 0.6. The simulation results under inductive loads are given in Table V. The table includes the combined capacitance values when CC operates and the percentage contribution of active power towards the apparent power indicated as (P/S) 2 .

Figure 11 shows the startup operation of the system using RL load of 125 Ω, 243 mH. At 0.36 s, the system has reached the target- ed RMS value of output voltage of 230 V with the final CC capacitance value of 11 µF at the reactive power of 186.20 var

31 level



15 level



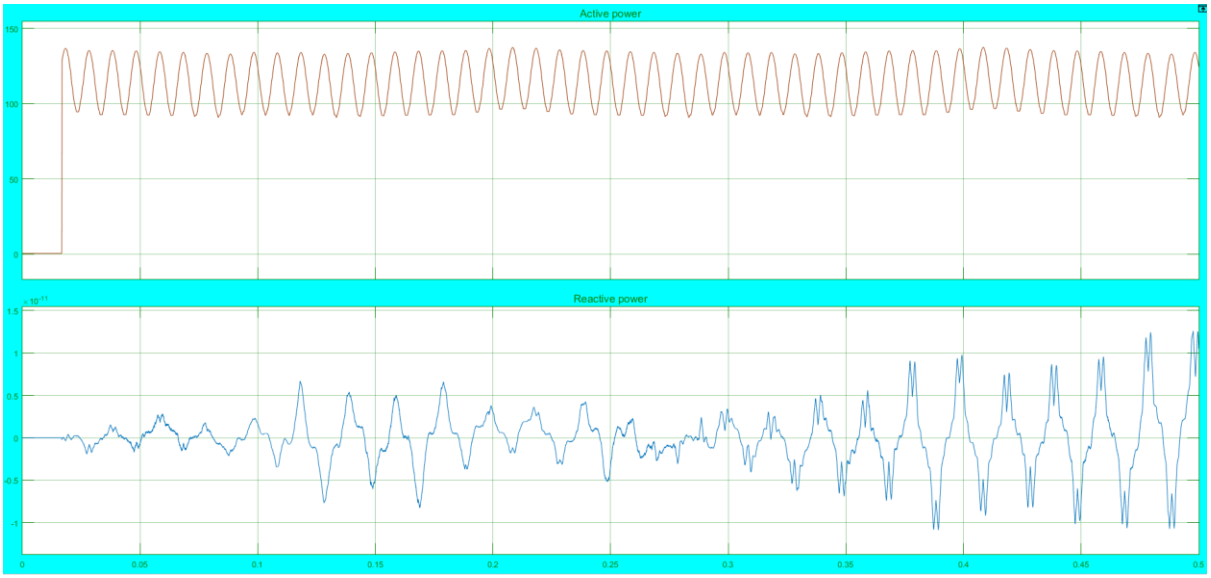
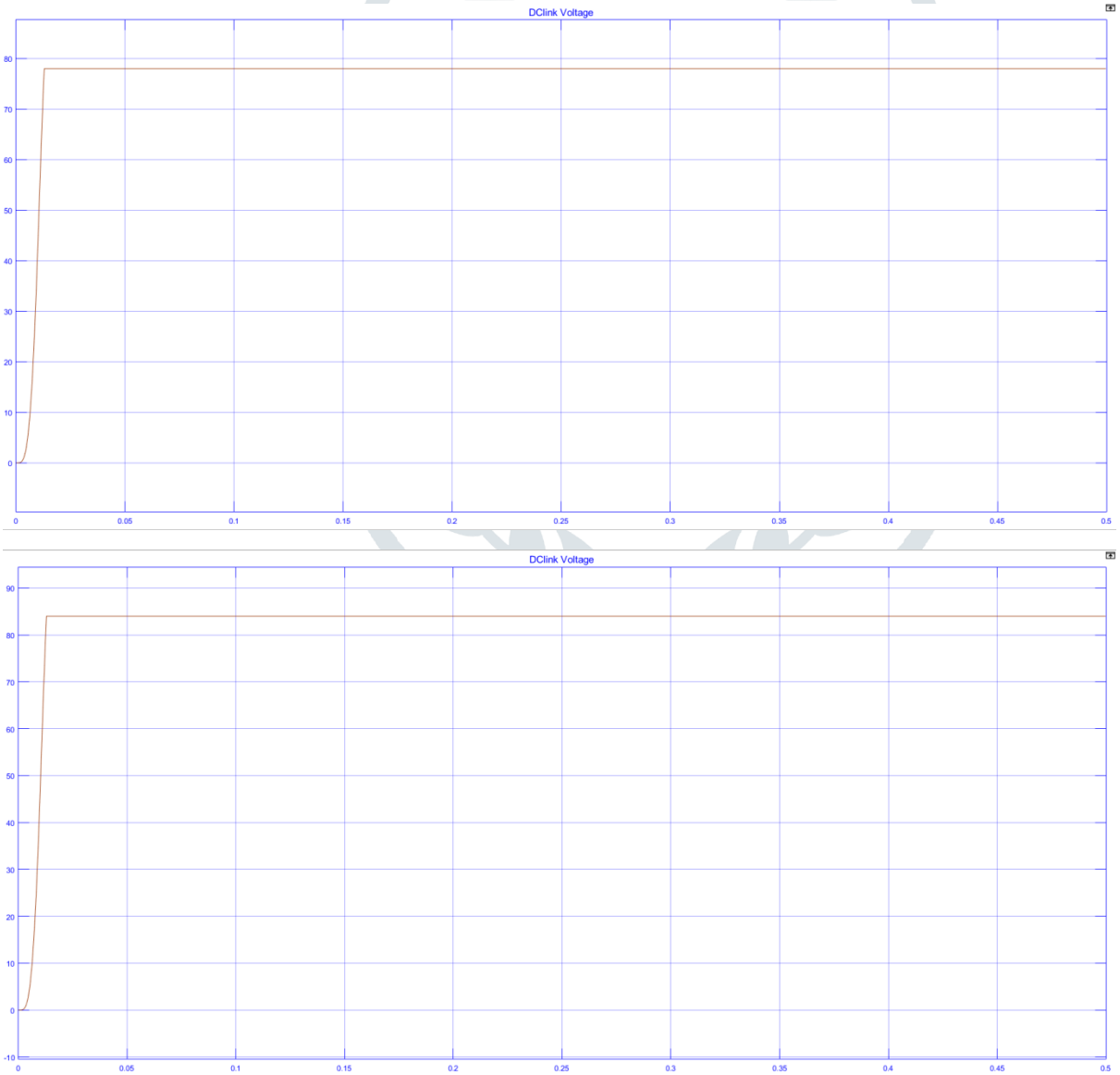


Fig. 11. Start-up behaviour. (a) Output voltage and current. (b) Measured reactive power and CC capacitance

31 level



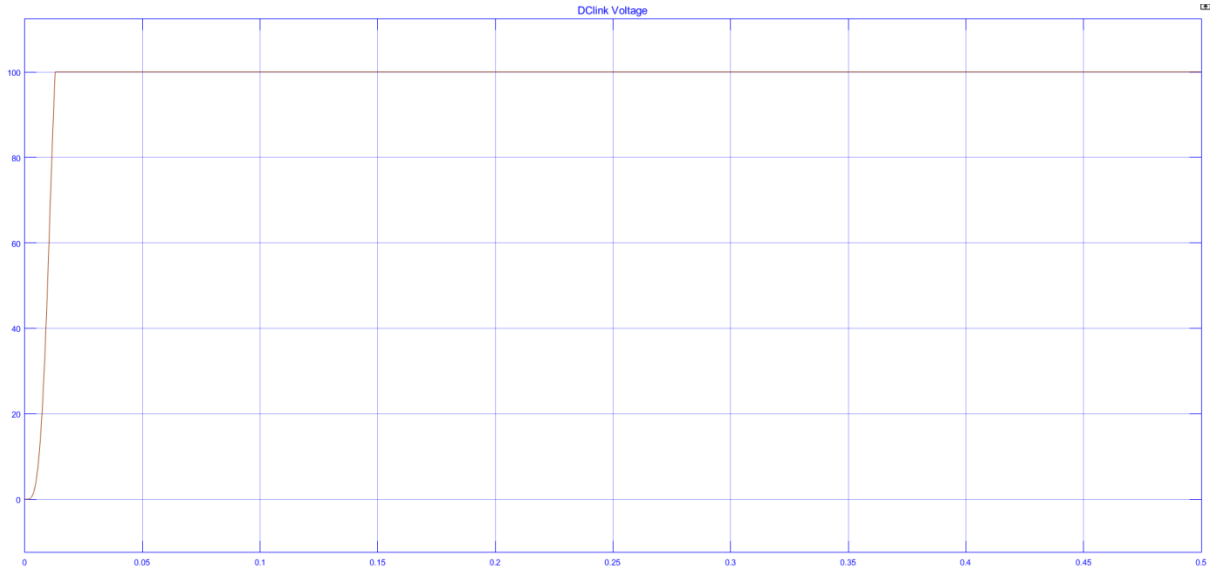
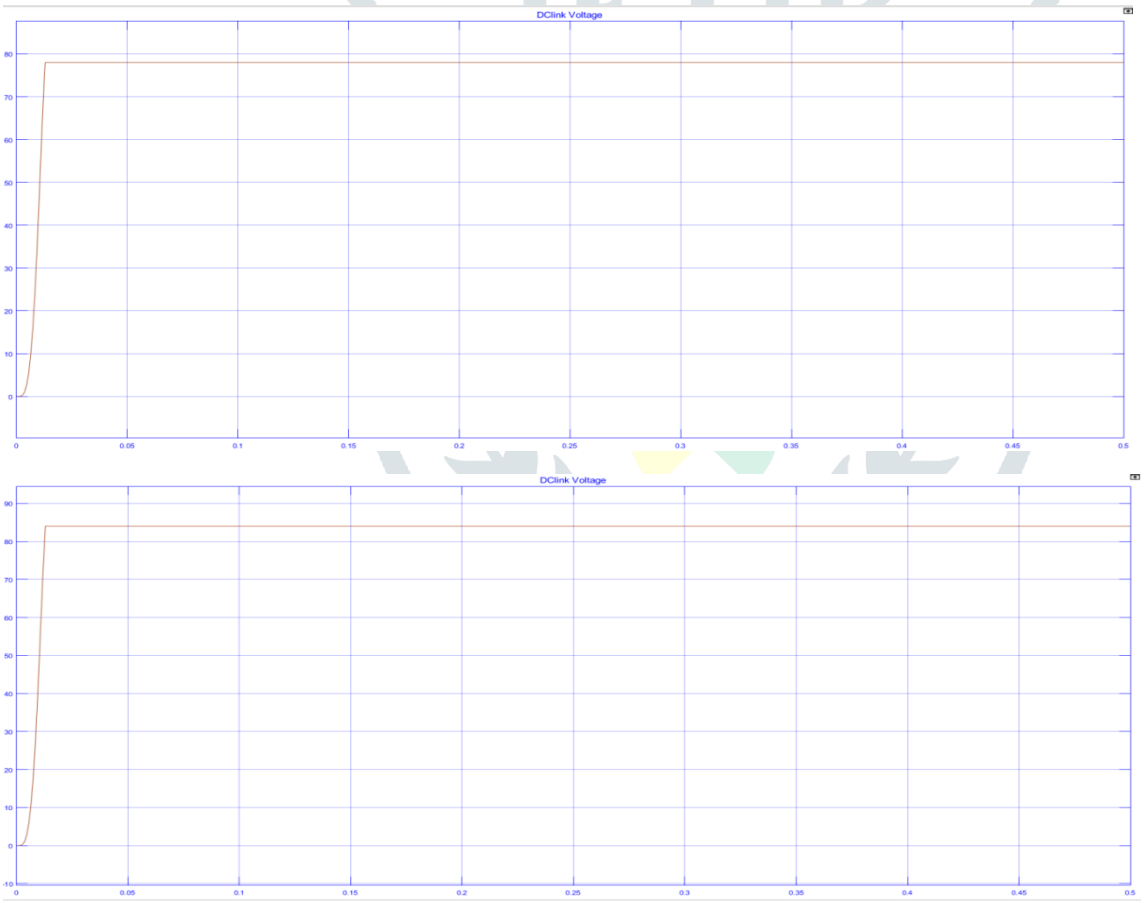
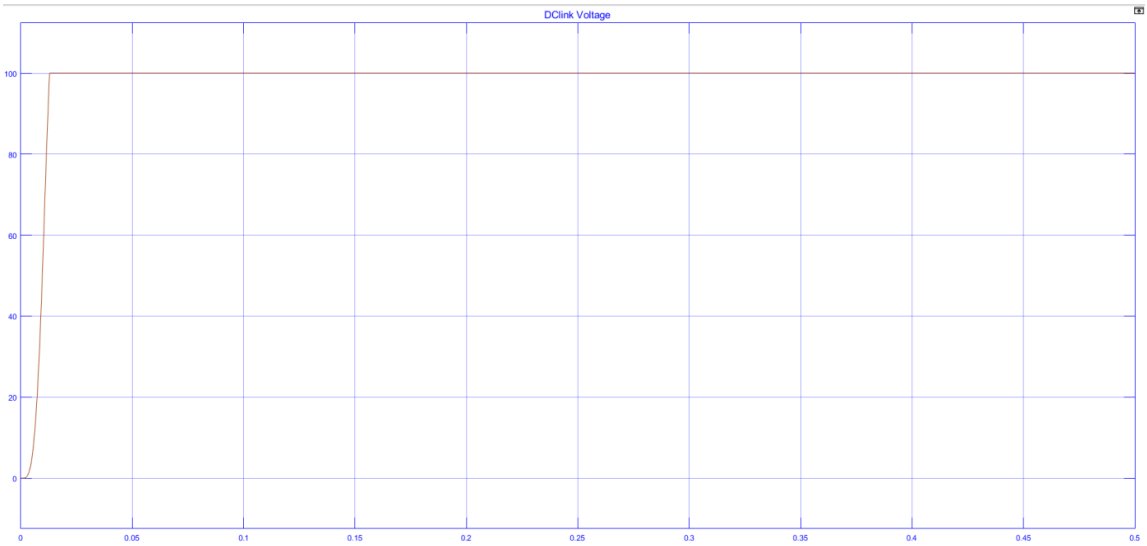


Fig. 13. DC-link voltage. (a) Under varying irradiance. (b) Using different reference values. (c) Using different load ratings. (d) Using different loads with the maximum value

15 level





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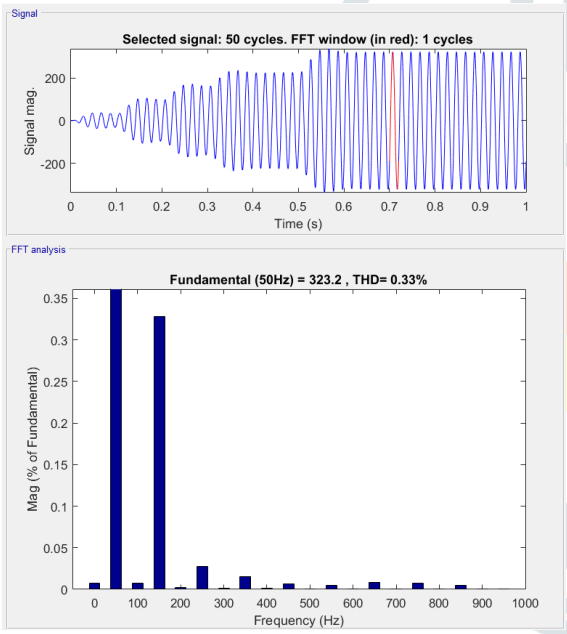

Fig. THD % of the 31 level Voltage with ANN

Proposed INCVR Test In order to validate the performance of the algorithm in maintaining the desired DC-link voltage, the INCVR is tested with a constant load under varying solar irradiance and voltage reference. The output from a boost converter is observed in this test. The third stage is selected which con- sists of four PV panels connected in series to produce the reference DC voltage of 86.74 V. The obtained DC-link volt- age under sudden changes in irradiation at a fixed tempera- ture of 31 o C is shown in Fig. 13(a). It can be observed that the proposed regulation technique has a faster initial re- sponse time without overshoot to achieve the desired output in comparison to the classic ANN controller. It also takes mini- mal time to re-track for the desired voltage at the point of ir- radiance change. The initial overshoot from ANN controller can be minimized with careful tuning. However, different tuning might be required when there is a change in load, environ- mental condition and reference value

CONCLUSION

The operation of a 31-level asymmetrical switch-diode based MLDCL inverter has been presented in this paper. A INCVR for a standalone system is proposed to maintain the desired voltage level at the output of each DC-DC boost converter while maintaining the ability of delivering the maxi- mum power under full-load operation even under varying environmental conditions. In the full-load test, the power obtained at the output of the system is found to be at 97.21% of the theoretical maximum power of the PV panels by the ANN. This proves the tracking ability of the proposed algorithm for the maximum power. It is also observed that the regulation technique is able to re-track the desired DC-link voltage under a rapid change in irradiance, reference value and load with very minimal response time. In addition, a CC circuit is also proposed to mitigate voltage spikes at inductive loads. A further test at dynamic loads is carried out to prove the robustness of the whole system. The system takes one electrical cycle of response time at most to reproduce the desired inverter output when the load is suddenly changed from purely resistive to inductive load, and from inductive load to another inductive load at different power factor levels are controlled by the ANN efficiently.

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