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DESIGN OF A 13-STAGE MODIFIED H-BRIDGE HYBRID MULTILEVEL SOLAR INVERTER

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Abstract : A 13-stage modified H-bridge solar inverter was designed with less numbers of solar photovoltaic modules, switches and diodes. A multilevel inverter is a device which converts DC to AC with more sinusoidal output. The proposed model is efficient in terms of output, redundancy and also costing. This inverter is capable to generate AC current directly from the solar photovoltaic modules. The proposed model used only 3 solar modules, 8 IGBTs, 8 clamping diodes and 3 DC bus capacitors. PWM signals were used to trigger the Gates of IGBTs. The THD in voltage and current wave has been administered at a significant low value and as reported by is nearly 2.68% and 2.58% respectively which is quite impressive.

Index Terms **- Multilevel inverter, Solar photovoltaic, H-bridge, THD.**

1. INTRODUCTION

With the increasing demand of the power, when the traditional resources are being exhausted rapidly, renewable power sources are getting attention more wisely. Due to the features of green and clean energy, solar photovoltaics are preferred most over others. A multilevel inverter (MLI) is an electronic control system, capable of supplying desired alternating voltage at the output using several lower level DC voltages as an input [1-4]. To utilize the solar power in terms of on and off grid conditions the MLIs play a major role. [5-8]. The MLIs are used in various practical high power [9-10], high voltage [11] and low current applications [12] because of a huge number of benefits starting from generating almost a pure sinusoidal output to reduced THD[13-14]. On another hand, they use a greater number of IGBTs and sources, more switches, and hence more connection and switching losses are encountered. This increases the size of the circuit and also hits the economic stability [15]. A traditional 13 level cascaded H-bridge MLI would use 24 IGBTs, 6 solar photovoltaic modules and 24 gate triggering pulses are required [16]. This increases the circuit redundancy and also the energy loss and space for installation are higher. In the proposed model, we have successfully attained the 13-level output with a lesser loss and distortion than encountered in the orthodox circuit. The new topology uses 8 IGBTs & 3 solar photovoltaic modules thus making it more economic, compact, faster and efficient.

2. MULTILEVEL INVERTER: DEMARCATION

The waveform for the three, five and seven level inverters is shown in the figures below (Fig.1) where we clearly see that as the levels are increasing, waveform becoming smoother. The Multilevel inverters can be exhaustively stemmed down to these types [17]. Amongst all the types that are listed here, our proposed model roughly falls under the Hybrid MLI demarcation of Modified H-Bridge bifurcation [18-21].

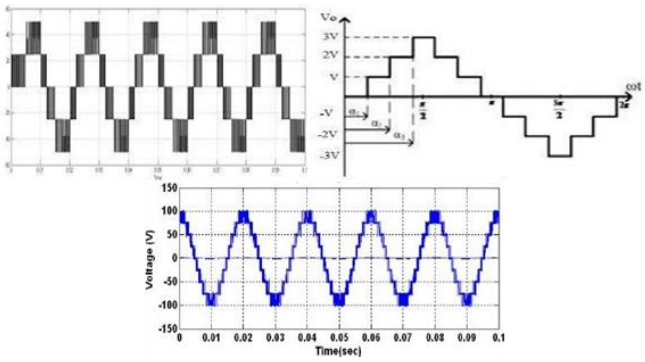

Fig. 1. A 5-level inverter output, A 7-level inverter output, A 9-level inverter output

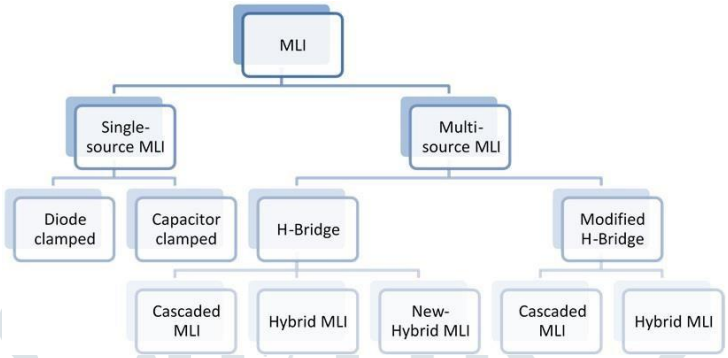

Fig. 2. MLI Family Tree

2. 1. Bi-Level Vs Multi-Level Inverter: Advertising Advantages

This section speaks about the various advantages of MLIs over the conventional Bi-level inverters.

Table 1. Advantages of Multilevel Inverters

Bi-Level Inverter	Multi-Level Inverter
• Only two inverting (IGBT) levels are present.	• Many such inverting levels are present and connected in suitable fashion to allow required output.
• The output is alternating in nature but doesn't correspond a pure sinusoidal wave.	• The output of such multi staged inverters corresponds to almost a pure sinusoid, owing to a greater number of levels.
• The absence of common mode voltages increases stress on the motor driven by the device.	• They produce common mode voltage, reducing the stress of the motor and hence avoiding damage.
• Input current is drawn with a higher distortion.	
• The operation of such inverter is taken at fundamental frequency. This accounts higher switching losses and lower efficiency.	• They can draw input current with low distortion.
	• They can work both at higher and lower switching frequency. A lower switching frequency implies lower switching loss & hence higher efficiency is achieved.
• The output of such inverters has harmonic distortions which can only be removed using a filter circuit. This adds to the cost of such circuit.	• Selective Harmonic Elimination used with MLI topology results in low harmonic distortion in the output without the use of filters.

2.2. CONTRASTING MLIS

2.2.1. APPLICATIONS

Multilevel Inverters since their advent have been very popular in the industry. Various applications of different orthodox Multi Level Inverter topologies are listed in the section below [22-25].

Table 2. Applications of various MLIs

Diode Clamped MLI	Capacitor Clamped MLI	Cascaded H-Bridge (CHB) MLI
• Static VAR compensation.	• Induction motor control using Direct Torque Control (DTC) circuit.	• Motor drives
• Variable speed motor drives. • High voltage system interconnections. • High voltage DC and AC transmission lines.	• Static VAR generation • Both DC-AC and AC- DC conversion applications. • Converters with harmonic distortion capability. • Sinusoidal current rectifiers.	• Active filters • Electric vehicle drives • DC power source utilization. • Power factor compensators. • Back to back frequency link systems. • Interfacing with Renewable energy sources.

2.2.2. ADVANTAGES &DISADVANTAGES

Every coin has both the faces and so has every field. Nothing lacks losses or demerits. But the advantages they have rendered in service outnumber their cons. Few of the disadvantages are mentioned in the section below. Also, they are well contrasted with each other's disadvantages. The sectional so contrasts and compares the various advantages among the pre-existing topologies.

Table 3. Comparison of Advantages and Disadvantages

	Diode Clamped	Capacitor Clamped	Cascaded H-Bridge
Advantages	• Same switching frequency for all the switches. • Modular structure is easy to analyze.	• Low cost and less components due to lesser number of capacitors. • Can be operated on SDCS.	• Each branch can be analyzed independently.
Disadvantages	• Separate DC sources are required.	• For more than 3 levels the charge balance gets disturbed. • Output voltage gets limited.	• Pre-charging capacitors are difficult.

2.2.3. COMPARISON OF POWER COMPONENT REQUIREMENT PER PHASE LEG

This section compares and contrasts the quantity of components required per leg in the pre-existing MLIs and hence shows a clear edge that our proposed prototype has over other.

Table 4. Component Comparison per leg

Components per phase	Diode Clamped MLI	Capacitor Clamped MLI	CHB MLI
Main switching devices	2(n-1)	2(n-1)	2(n-1)
Main diodes	2(n-1)	2(n-1)	2(n-1)
Clamping diodes	(n-1)(n-2)	0	0
DC bus capacitors	(n-1)	(n-1)	(n-1)/2
Balancing capacitors	0	(n-1) (n-2)/2	0

Table 5. Voltage level and switch number comparison

Topology	Voltage level of each stage	Number of output levels	Number of switches used
Diode clamped MLI	Vs- on each C	N_c+1 (N_c is number of C)	N_c
Flying capacitor MLI	SV_{dc}/(n-1)	S	S-1
CHB MLI	SV_{dc}	S	4S

Where 'n' is the number of output levels, 'N_c' is the number of capacitors and 'S' is the number of photovoltaic sources.

3. VARIOUS CLAMPING TOPOLOGIES FOR DIFFERENT PHASES IN MLIS: DISCUSSING THD

3.1. BUS CLAMP TECHNIQUE

In this technique every phase gets clamped for certain duration over fundamental cycle [26-27]. The clamped phase is not switched over the clamped period. A reference vector is generated by switching other two phases. As a result, switching loss is less in BCPWM as compare to that of CSVPWM, at same carrier frequency. Depending on the position of clamping zone in the space vector plane, there exist different type of BCPWMs. 300 and 600 BCPWMs are more popular. Over the fundamental cycle, normal clamping duration is 1200. For 300 BCPWM each phase gets clamped for duration of 300for each quarter of fundamental cycle. So, it's also called as split phase BCPWM. On the other hand for 600BCPWM, the particular phase gets clamped for duration of 600 at the middle of each half cycle. This PWM technique is called continual clamping, as the clamping zone is continuous for each half zone. In three level inverters BCPWM can also be applicable. There are four types of BCPWM techniques i.e. Type-1, Type-2, Type-3 and Type-4. The hexagon and the zone of clamping for above type of BCPWM have been shown in Fig 3. In type-1 positive R-ph is clamped from $n\pi/3$ to $2n\pi/3$and negative R-ph is clamped from $4n\pi/3$ to $5n\pi/3$. For type-2 positive R-ph is clamped from $n\pi/2$ to $5n\pi/6$ and negative R-ph is clamped from$3n\pi/2$ to $11n\pi/6$. Likewise, in type- 3 positive R-ph is clamped from $n\pi/6$ to $n\pi/2$ and negative R-ph is clamped from $7n\pi/6$ to $3n\pi/2$ (Rakesh Kumar Dhal, September 12 – 13, 2015). In above type of clamping all the phases are clamped for continuous 600 in both positive as well as negative fundamental cycles, but with a phase difference of 1200. The next phase is clamped after a period of 600 and continued. In type-4 positive R-ph is clamped from $n\pi/6$ to $n\pi/3$ & $2n\pi/3$ to $5n\pi/6$ and negative R-ph is clamped from $7n\pi/6$ to $4n\pi/3$ & $5n\pi/3$ to $11n\pi/6$.

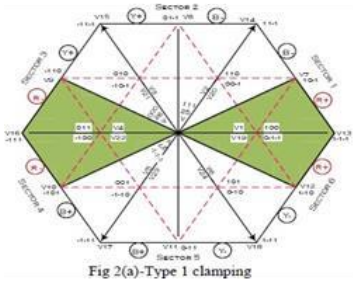
Fig 2(a)-Type 1 clamping

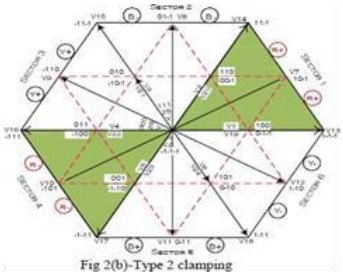
Fig 2(b)-Type 2 clamping

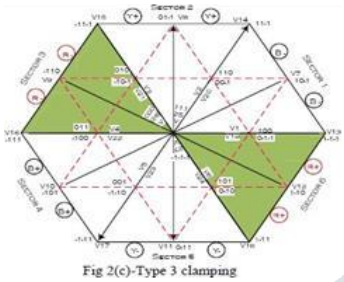
Fig 2(c)-Type 3 clamping


Fig 2(d)-Type 4 clamping

Fig. 3. T1, T2, T3 and T4 camping (clockwise)

3.2. TOTAL HARMONIC DISTORTION

This section deals with the Total harmonic distortion calculated based on the clamping technique modulationdiscussedinthesectionaloft.Thevalueslisteddownherearethengraphicallyencoded in the pages to follow. Harmonic value comparison is the main aim, this part focuses on.

Table 6. THD comparison

T1 Clamped Output THD %		T2 Clamped Output THD %		T3 Clamped Output THD %		T4 Clamped Output THD %	
V_{Pole}	47.34	V_{Pole}	53.42	V_{Pole}	53.8	V_{Pole}	59.19
V_{LL}	32.8	V_{LL}	34.8	V_{LL}	34.61	V_{LL}	31.58
V_{PH}	32.70	V_{PH}	33.77	V_{PH}	33.43	V_{PH}	31.55
I_{PH}	0.45	I_{PH}	0.48	I_{PH}	0.49	I_{PH}	0.17
V_{pole}	46.80	V_{pole}	52.84	V_{pole}	53.07	V_{pole}	58.54
V_{LL}	32.02	V_{LL}	33.81	V_{LL}	34.52	V_{LL}	31.17
V_{PH}	32.16	V_{PH}	33.3	V_{PH}	32.71	V_{PH}	31.02
I_{PH}	0.46	I_{PH}	0.48	I_{PH}	0.49	I_{PH}	0.16
V_{Pole}	47.01	V_{Pole}	53.33	V_{Pole}	53.22	V_{Pole}	58.76
V_{LL}	32.92	V_{LL}	34.4	V_{LL}	35.03	V_{LL}	31.23
V_{PH}	32.69	V_{PH}	33.66	V_{PH}	33.14	V_{PH}	31.19
I_{PH}	0.45	I_{PH}	0.49	I_{PH}	0.49	I_{PH}	0.16

4. THIRTEEN- LEVEL INVERTER: ORTHODOX VS NEW TOPOLOGY

4.1. COMPARISON

In a view to build a superior model, the superiority has to be contrasted with an existing orthodox prototype. This section aims at achieving this. Though many other parameters are left to calculate in view of declaring anything and coming out to a conclusion. However, this section deals with the component edge, the model has over the others.

Table 7. Component comparison between proposed and existing topology

Components	13-Level Orthodox CHB	13-Level New Topology
Main switching devices	24	8
Main diodes	24	8
Clamping diodes	0	0
DC bus capacitors	6	3
Balancing capacitors	0	0
Number of switches used	24	8

Added advantages of the new topology:

The added advantages of the proposed New Topology of Cascaded H-bridge Multi-Level Inverter as compared to the orthodox topology can be cited as under:

- It has 1/3rdof the switches as compared to what it had in the previously proposed model.
- The reduced number of switches account for lower switching delays and lesser switching loss.
- It has 1/3rddiodes as compared to what it had in the circuit back in records.
- Lesser diodes account for more accurate and precise output voltage owing to lesser diode voltage drops.
- It uses half as much DC sources compared to what it used in the days of yore.
- The lesser use of DC sources improves the economic liability for the circuit and enhances it compactness. It also alters the weight and hence allows in strengthening the model in physical terms.
- ThenewermodelhasanimprovedTHDandhencegivesabettergroundtoapproximatethe output waveform produced to a near sinusoidal.

The decreased number of components not only relaxes the redundancy and cost of the circuit, but also improves its efficiency.

5. SIMULATION CIRCUIT

In the simulation circuit of the new topology we are using 8 IGBT switches divided in 2 columns, each having 4 IGBT. We named the left column IGBTs as 1, 2, 3, 4 and then right column as 5, 6, 7, 8. To achieve 13 level topology we connect 3 solar photovoltaic modules of 100 V, 200 V and 300 V as follows:

- 100 V between E of IGBT 1 & C of IGBT5
- 300 V between E of IGBT 6 & C of IGBT2
- 100 V between E of IGBT 3 & C of IGBT7

Here positive terminals of the 3 modules are connected with collector and negative terminal with emitter. We get the output between terminals of the two columns. We again used NOT operation for getting/generating the gate pulses. We have taken 4 gate pulses and triggered 1,2,3,4 IGBT respectively and the same gate pulse through NOT operation for triggering 5, 6, 7, 8 respectively. We have taken R-L load but for now we have kept the value of L to be zero.

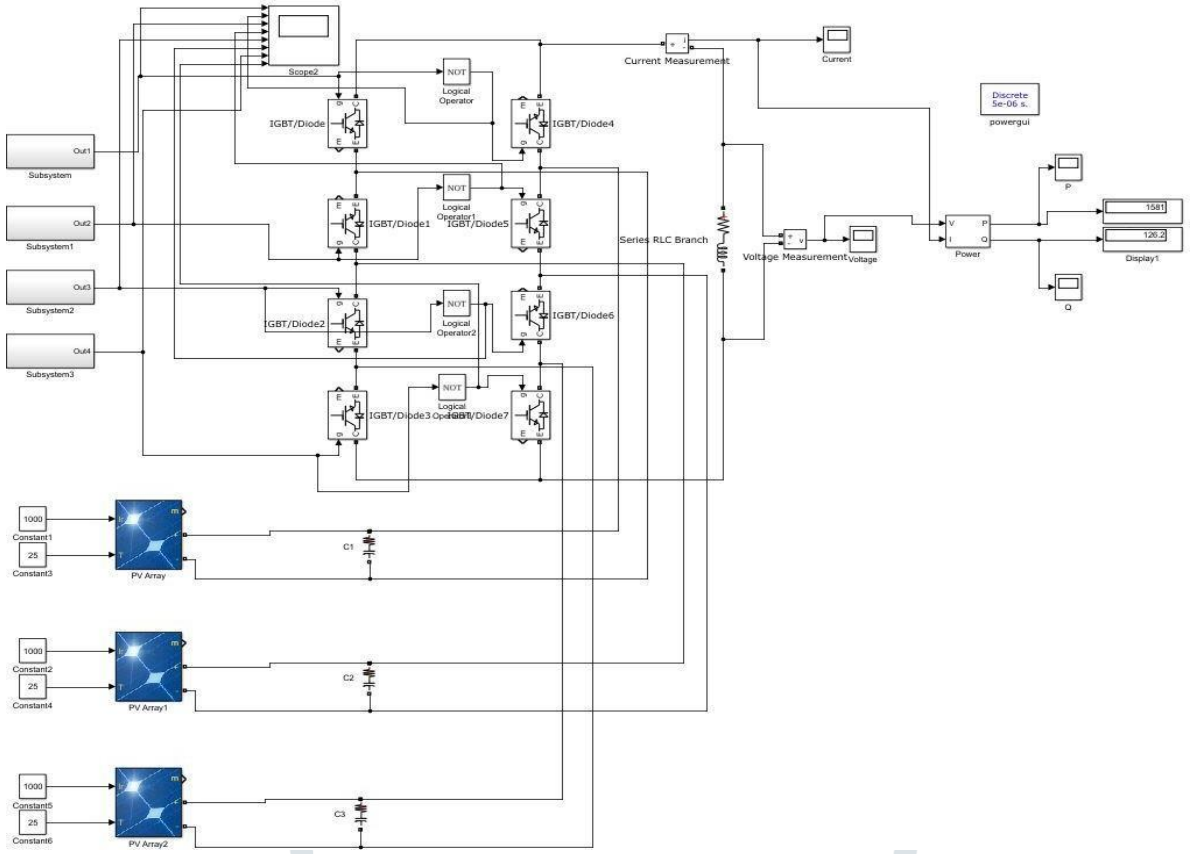

Fig. 4. Simulation Circuit of the proposed model

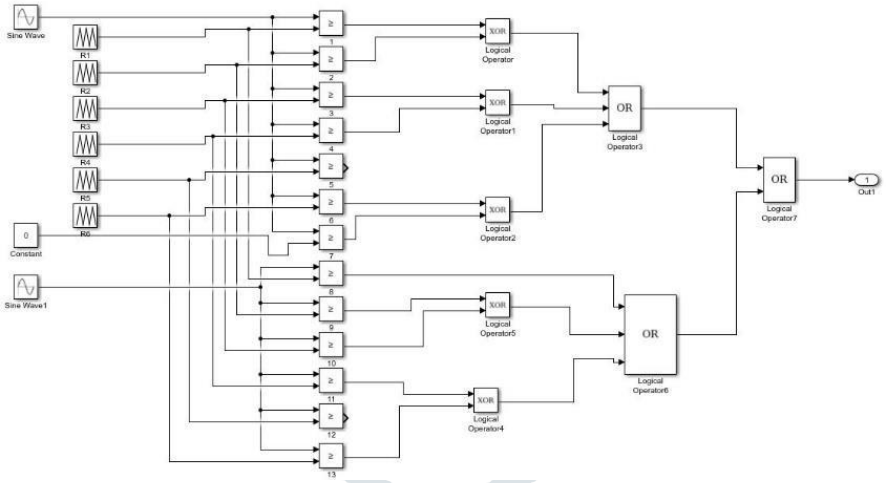

Fig. 5. Gate triggering circuit for IGBT 1&5

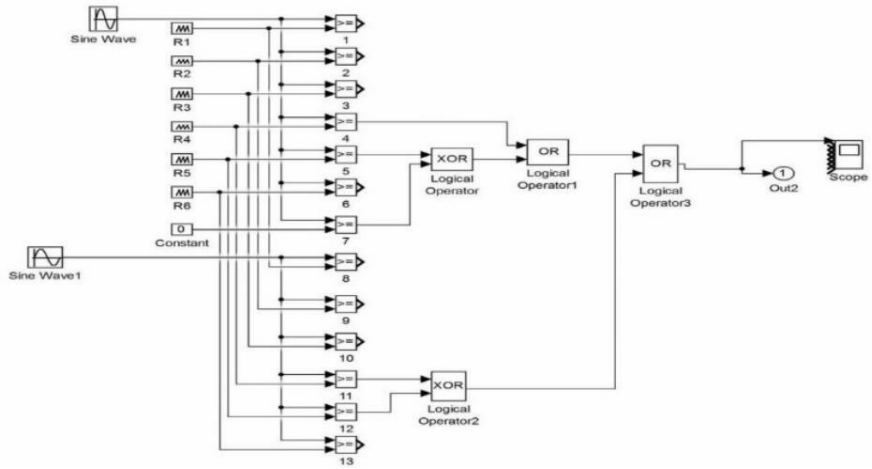

Fig. 6. Gate triggering circuit for IGBT2&6

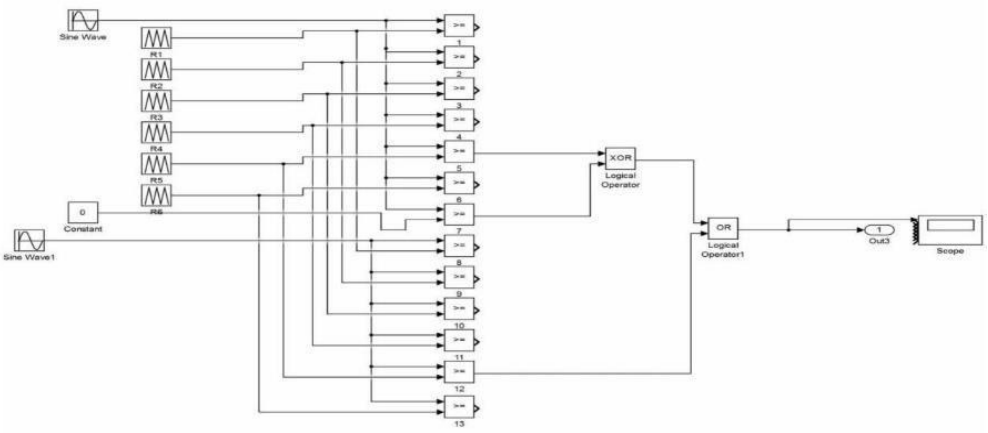

Fig. 7. Gate triggering circuit for IGBT3&7

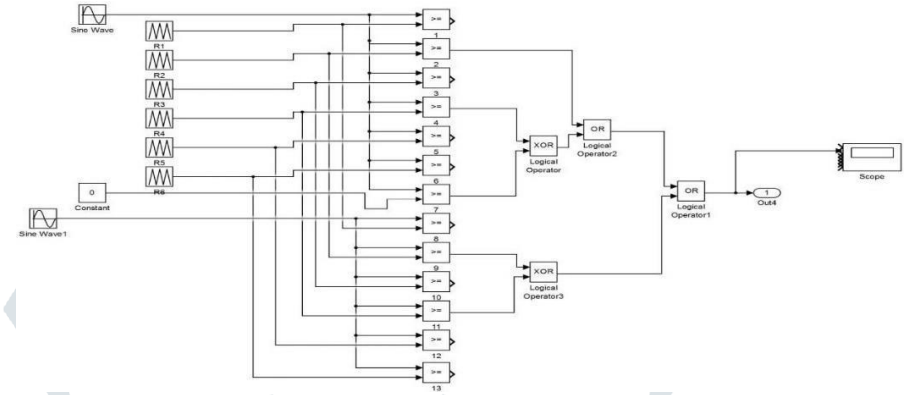

Fig. 8. Gate triggering circuit for IGBT4&8

5.1. Switching Mechanism for 13-Level MLI

Table 8. Switching sequence logic table

LEVEL / IGBT	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12	L13
G1	OFF	ON	ON	OFF	ON	OFF	ON	ON	OFF	ON	OFF	OFF	ON
G2	ON	ON	OFF	OFF	ON	ON	ON	OFF	OFF	ON	ON	OFF	OFF
G3	OFF	OFF	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	ON	ON
G4	ON	ON	ON	ON	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	OFF
G5	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	ON	ON	OFF
G6	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	ON
G7	ON	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	ON	OFF	OFF
G8	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	ON	ON	ON	ON
Level Voltage	600	500	400	300	200	100	0	-100	-200	-300	-400	-500	-600

The concept behind switching the IGBTs based on which the above table is achieved, has been discussed below, The level 600 is achieved as 100+200+300, the level 500 is achieved as 200+300, the level 400 is achieved as 100+300, the level 300 is achieved as 300, the level 200 is achieved as200, the level 100 is achieved as 100 & the 0^{th} level is achieved with all the gates of same side shorted.

6. Simulation Output: Graphs & Parameters

6.1. IGBT Gate Pulse

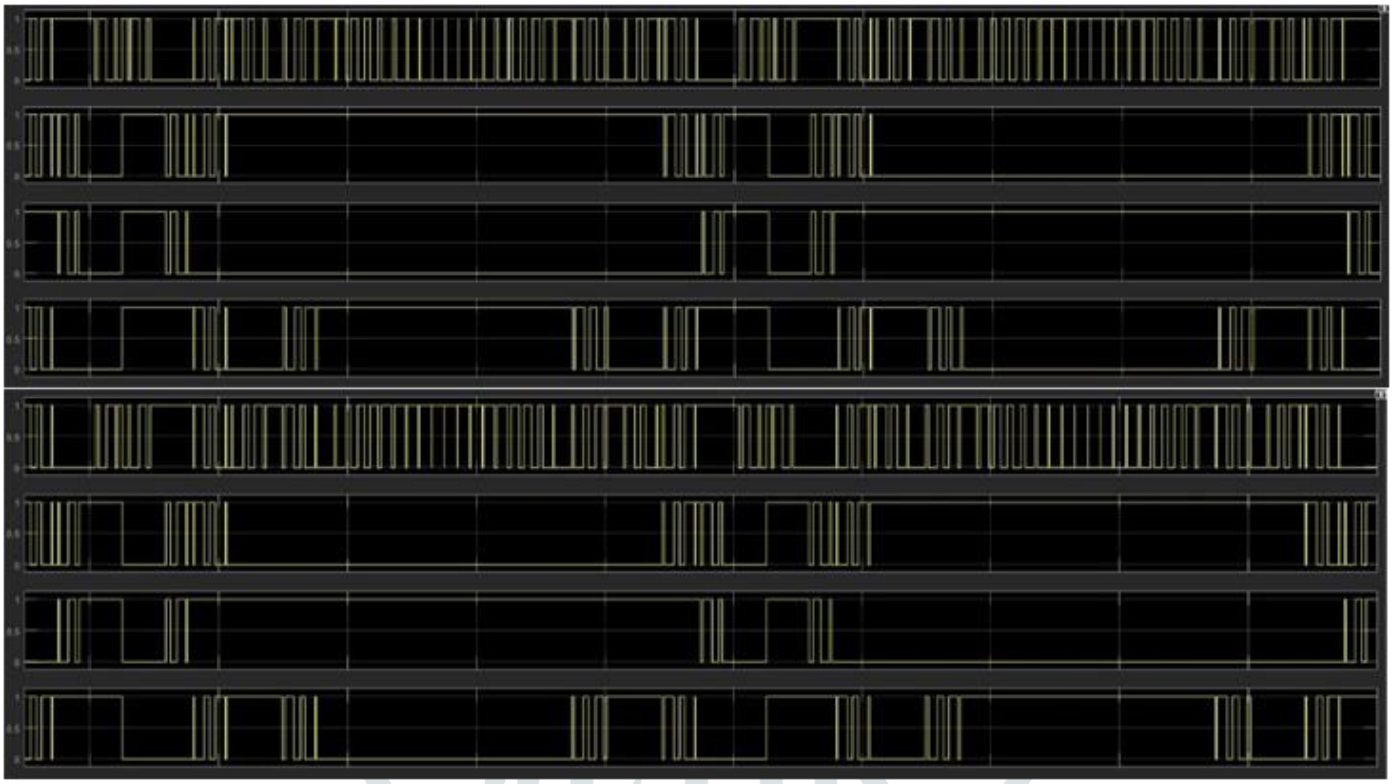

Fig. 9. Gate pulses to drive the IGBTs (in sequence 1-8)

Insulated Gate Bipolar Transistor (IGBT) which is used as switches in the project requires a proper gate triggering for its operation. Moreover, IGBT synchronous commutation is fairly important forasafeloadcharacteristic.TheIGBTtriggeringalsohasadrasticimpactontheTotalHarmonic Distortion (THD) that results in dismantling of the output from desired. A smoother output voltage and current waveform is what we desire. The gate triggering in this half of the project has been achieved through Pulse Width Modulation (PWM) technique and realized on the logic devices viz, logic gates and Comparators (harnessed by their combinations). The PWM pulses are generated by comparison of 2 signals, one of which is the reference signal, which decides output shape of PWM. In the Multilevel Inverter (MLI) prototype proposed here, a sinusoidal and non- zero crossing triangular pulse are compared for generating PWM pulses that would fetch positive half of the output wave. The other half can be graphed to reality by comparing the out phased sinusoidal with the reference non-zero crossing triangular pulses. The gates are being triggered in NOT pairs to avoid commutation issues and equivalently the output in lesser number of gate triggering. IGBT 1-5, 2-6, 3-7 and 4-8 are paired with the same vision. Hence, the pulse to gates of IGBT 5 through 8 are the pulses generated by the NOT operation on the gate pulses of IGBT 1 through 4. Also, the aim of generating such structured gate pulses can clearly been observed from the switching sequence logic table, discussed the literature before. The output waveforms for various gate triggering pulses are shown in the above figures.

6.2. COMPARATIVE STUDY OF GATE PULSES

The figure aloft makes a comparative study of the entire gate triggering pulses for the IGBT gates 1 through 4, it is quite impeccable to assume that the other 4 pulses will be NOT operation of these. It can clearly be seen in comparison to the switching sequence logic table as to how the output levels from -600 to +600 through zero are dealt. For instance, let us look at a particular instant from the comparative figure shown above. The logic sequence at the start can be seen to be 1111 for gates 1 through 4 and then 0111 for the similar combination. From the switching sequence logic table, it can be clearly referred that these correspond to an output level of 0 Volts and 100 Volts respectively, and then the same switching is repeated with a very high frequency until the next gate pulse arises. The output voltage wave thus oscillates between these 2 voltage levels as we would see in the section that leads. The continuous gating leads to the rapid oscillation of the output waveform between all consecutive levels and hence generates a better approximation of a sinusoid which is of utmost importance in practical application. For easy analysis, we have used a resistive load in this project.

6.2. RESULTS AND DISCUSSION

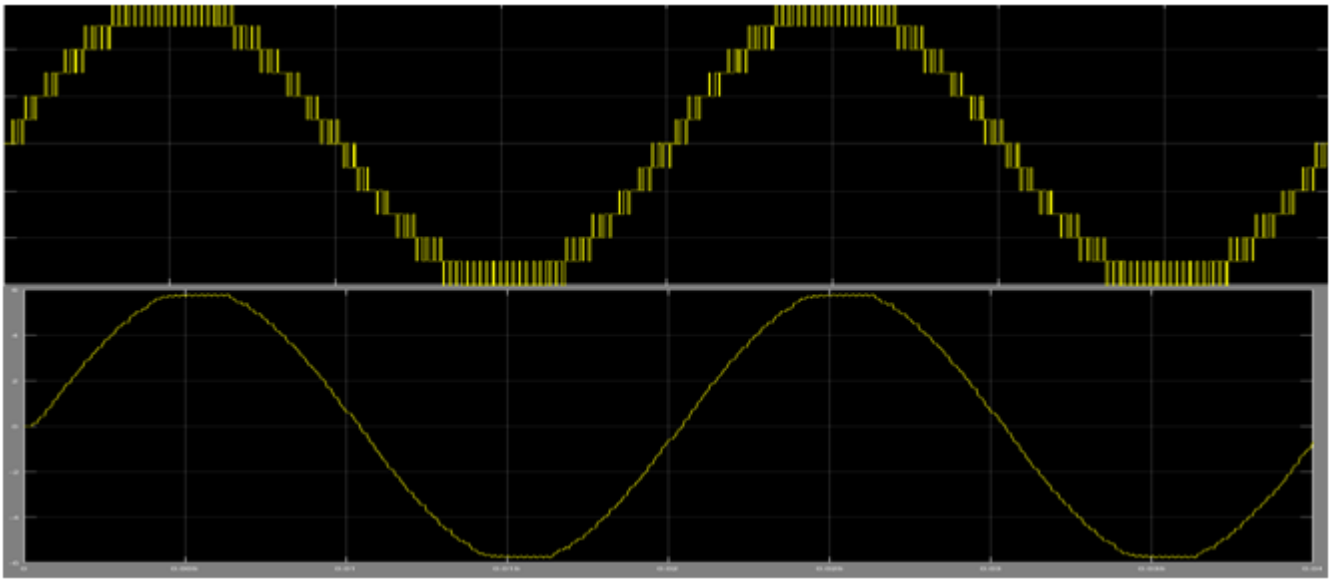

Fig. 10. Output voltage and current waveform.

The generation of output current and voltage waveform have already been put to logic and are put as a figure in the texts above. We can clearly see that the current waveform follows the voltage as ideally it should incase of a resistive load. Also, the output voltage waveform is a13-level output that has been generated through the proposed combination of the IGBTs and gate logics. The output voltage waveform is no doubt a better approximation of a sinusoidal waveform. It's quite true that with the increase in level so many orthodox multilevel topology, the waveform might even be better on such grounds, however it's noteworthy that the number of IGBTs and modules used here are considerably less. Specifically, to mention, the THD in voltage and current wave has been administered at a significant low value and as reported by MATLAB is nearly 2.68% and 2.58% respectively, which is shown in the section that follows. The main object of this project was to design a multi-level solar inverter where a proper simulation and desired output was the aim to accomplish, which we have quite well achieved with magnanimous significance. Total harmonic distortion (THD) has been briefly touched in this section. The THD is defined as the vector sum of harmonic voltages to the total assumed voltage output. The THD calculation has however not been taken manually here, as is discussed in the section above. The results from the FFT analysis command on MATLAB are shown below.

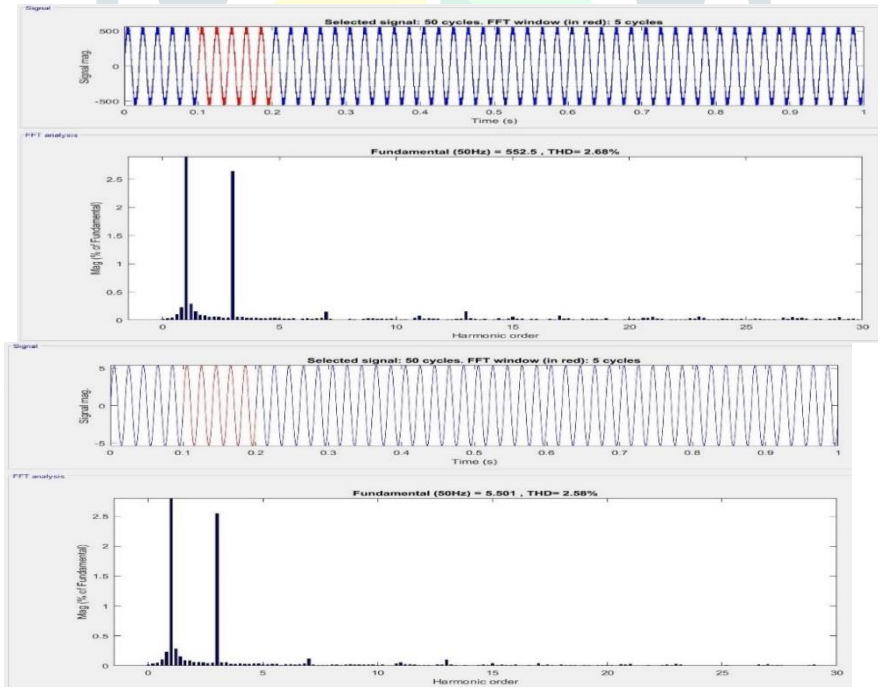

Fig. 11. Voltage and current THD analysis through MATLAB

CONCLUSION

In this paper, we have proposed an improved 13-level solar inverter model which is superior to its predecessor in various regards. The output current of the model is purely sinusoidal and the output voltage is also almost sinusoidal. The THD has been reduced and a better economic, less weight, compact and more efficient way to achieve a 13-level output waveform has

been obtained. This design is unique in terms of its design, cost and performance. A new topology to design a13level MLI is proposed in this work with only 8 numbers of IGBTs, main switches and diodes. The no. of components used here is very less in comparison to same category of other MLIs. The THD was ranging between 2.58%- 2.68% only which is quite impressive [28-29]. The reduced number of switches account for lower switching delays and lesser switching losses [30]. Lesser diodes account for more accurate and precise output voltage owing to lesser diode voltage drops. It uses half as much DC sources compared to what it used in the days of yore. The lesser use of DC sources improves the economic liability for the circuit and enhances it compactness. It also alters the weight and hence allows in strengthening the model in physical terms. The newer model has an improved THD and hence gives a better ground to approximate the output wave form produced to an ear sinusoid. The decreased number of components not only relaxes the redundancy and cost of the circuit, but also improves its efficiency.

REFERENCES

[1] Najafi, E., & Yatim, A. H. M. (2011). Design and implementation of a new multilevel inverter topology. IEEE transactions on industrial electronics, 59(11), 4148-4154.

[2] Zhang, H., Von Jouanne, A., Dai, S., Wallace, A. K., & Wang, F. (2000). Multilevel inverter modulation schemes to eliminate common-mode voltages. IEEE transactions on industry applications, 36(6), 1645-1653.

[3] Rodriguez, J., Lai, J. S., & Peng, F. Z. (2002). Multilevel inverters: a survey of topologies, controls, and applications. IEEE Transactions on industrial electronics, 49(4), 724-738.

[4] Peng, F. Z. (2001). A generalized multilevel inverter topology with self voltage balancing. IEEE Transactions on industry applications, 37(2), 611-618.

[5] Daher, S., Schmid, J., & Antunes, F. L. (2008). Multilevel inverter topologies for stand- alone PV systems. IEEE transactions on industrial electronics, 55(7), 2703-2712.

[6] Kang, F. S., Cho, S. E., Park, S. J., Kim, C. U., & Ise, T. (2005). A new control scheme of a cascaded transformer type multilevel PWM inverter for a residential photovoltaic power conditioning system. Solar Energy, 78(6), 727-738.

[7] Xiao, B., Hang, L., Mei, J., Riley, C., Tolbert, L. M., &Ozpineci, B. (2014). Modular cascaded H-bridge multilevel PV inverter with distributed MPPT for grid-connected applications. IEEE Transactions on Industry Applications, 51(2), 1722-1731.

[8] Busquets-Monge, S., Rocabert, J., Rodriguez, P., Alepuz, S., &Bordonau, J. (2008). Multilevel diode-clamped converter for photovoltaic generators with independent voltage control of each solar array. IEEE Transactions on Industrial Electronics, 55(7), 2713-2723.

[9] Gopalakrishnan,K.,SundarRaj,M.,&Saravanan,T.(1950).Multilevelinvertertopologies for high-power applications. Middle-East Journal of Scientific Research, 20(12), 2014.

[10] Manjrekar, M.D., Steimer,P.K., & Lipo,T.A.(2000). Hybrid multilevel power conversion system: A competitive solution for high-power applications. IEEE transactions on industry applications, 36(3), 834-841.

[11] Lopez, M.G., Moran, L.T., Espinoza, J.C., & Dixon, J.R. (2003, November). Performance analysis of a hybrid asymmetric multilevel inverter for high voltage active power filters applications. In IECON'03. 29th Annual Conference of the IEEE Industrial Electronics Society (IEEE Cat. No. 03CH37468) (Vol. 2, pp. 1050-1055). IEEE.

[12] Beig, A. R., & Dekka, A. (2012). Experimental verification of multilevel inverter-based standalone power supply for low-voltage and low-power applications. IET Power Electronics, 5(6), 635-643.

[13] Yousefpoor, N., Fathi, S. H., Farokhnia, N., & Abyaneh, H. A. (2011). THD minimization applied directly on the line-to-line voltage of multilevel inverters. IEEE Transactions on industrial electronics, 59(1), 373-380.

[14] Liu, Y., Hong, H., & Huang, A. Q. (2009). Real-time algorithm for minimizing THD in multilevelinverterswithunequalorvaryingvoltagestepsunderstaircasemodulation.IEEE Transactions on Industrial Electronics, 56(6), 2249-2258.

[15] Parastar,A., Kang,Y.C. ,& Seok,J.K. (2014).Multi level modular DC/DC power converter for high-voltage DC-connected offshore wind energy applications. IEEE Transactions on Industrial electronics, 62(5), 2879-2890.

[16] Sinha, A., Jana, K. C., & Das, M. K. (2018). An inclusive review on different multi-level inverter topologies, their modulation and control strategies for a grid connected photo- voltaic system. Solar Energy, 170,633-657.

[17] Murugesan, M., Pari, R., Sivakumar, R., & Sivaranjani, S. (2016). Different types of multilevel inverter topologies-A technical Review. Int J Adv Engg Tech, 7(I), 155.

[18] Sarkar, I., & Fernandes, B. G. (2014, October). Modified hybrid multi-carrier PWM technique for cascaded H-Bridge multilevel inverter. In IECON 2014-40th Annual Conference of the IEEE Industrial Electronics Society (pp. 4318-4324).IEEE.

[19] Aleenejad, M., Iman-Eini, H. & Farhangi,S. (2013). Modified space vector modulation for fault-tolerant operation of multilevel cascaded H-bridge inverters. IET Power Electronics, 6(4), 742-751.

[20] Kim, S. M., Lee, J. S., & Lee, K. B. (2016). A modified level-shifted PWM strategy for fault-tolerant cascaded multilevel inverters with improved power distribution. IEEE Transactions on Industrial Electronics, 63(11), 7264-7274.

[21] Boonmee, C., & Kumsuwan, Y. (2013, November). Control of single-phase cascaded H-

bridgemultilevelinverterwithmodifiedMPPTforgrid-connectedphotovoltaicsystems.In IECON 2013-39th Annual Conference of the IEEE Industrial Electronics Society (pp.566- 571). IEEE.

[22] Daher, S., Schmid, J., & Antunes, F. L. (2008). Multilevel inverter topologies for stand- alone PV systems. IEEE transactions on industrial electronics, 55(7), 2703-2712.

[23] Gupta, K. K., Ranjan, A., Bhatnagar, P., Sahu, L. K., & Jain, S. (2015). Multilevel inverter topologies with reduced device count: A review. IEEE transactions on Power Electronics, 31(1), 135-151.

[24] Peng, F. Z., Qian, W., & Cao, D. (2010, June). Recent advances in multilevel converter/invertertopologiesandapplications.InThe2010InternationalPowerElectronics Conference-ECCE ASIA- (pp. 492-501).IEEE.

[25] Colak, I., Kabalci, E., &Bayindir, R. (2011). Review of multilevel voltage source inverter topologies and control schemes. Energy conversion and management, 52(2), 1114-1128.

[26] Guangzhu, W. (2002). Mechanism of DC bus voltage unbalance in diode-clamped multilevel inverters. PROCEEDINGS-CHINESE SOCIETY OF ELECTRICAL ENGINEERING, 22(12), 111-117.

[27] Ozdemir,E.,Ozdemir,S.,&Tolbert,L.M.(2008).Fundamental-frequency-modulatedsix- level diode-clamped multilevel inverter for three-phase stand-alone photovoltaic system. IEEE Transactions on Industrial Electronics, 56(11), 4407-4415.

[28] Liu, Y., Hong, H., & Huang, A. Q. (2008). Real-time calculation of switching angles minimizing THD for multilevel inverters with step modulation. IEEE Transactions on Industrial Electronics, 56(2), 285-293.

[29] Farokhnia, N., Vadizadeh, H., Fathi, S. H., &Anvariasl, F. (2010). Calculating theformula of line-voltage THD in multilevel inverter with unequal DC sources. IEEE Transactions on Industrial Electronics, 58(8), 3359-3372.

[30] Schweizer, M., & Kolar, J. W. (2012). Design and implementation of a highly efficient three-level T-type converter for low-voltage applications. IEEE Transactions on Power Electronics, 28(2), 899-907.