JETIR.ORG ISSN: 2349-5162 | ESTD Year : 2014 | Monthly Issue
JOURNAL OF EMERGING TECHNOLOGIES AND INNOVATIVE RESEARCH (JETIR)
An International Scholarly Open Access, Peer-reviewed, Refereed Journal

RECENT ADVANCES IN SRAM DRAM AND FLASH MEMORY ARCHITECTURES: A COMPREHENSIVE REVIEW

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Abstract: In modern microcontroller-based electronic systems, memory design has emerged as a critical factor in determining overall system performance, reliability, and cost-effectiveness. With the rapid growth of embedded applications and the demand for compact, high-speed devices, memory technologies must address key challenges such as low power consumption, minimal leakage current, reduced latency, high storage density, and smaller device size. These requirements are especially important in portable and battery-operated systems, where energy efficiency and long-term data retention significantly influence design choices. This paper presents an in-depth discussion of three widely used memory technologies—Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), and Flash memory—focusing on their operational principles, advantages, limitations, and applicability in ultra-large-scale integration (ULSI) environments. DRAM offers high density and scalability but faces challenges of refresh cycles and power consumption. SRAM provides faster access and low latency, making it suitable for cache memory, but its high leakage current and larger cell size limit scalability. Flash memory, on the other hand, ensures non-volatility and cost-effectiveness for data storage, but suffers from slower write operations and endurance issues. The paper also explores recent innovations aimed at improving these technologies by reducing leakage currents, enhancing data expansion capabilities, and achieving higher density while maintaining power efficiency. By analyzing the trade-offs and design considerations of DRAM, SRAM, and Flash, this study provides valuable insights into selecting suitable memory solutions for modern microcontroller-based embedded systems. These advancements ultimately pave the way for the development of cost-effective, power-efficient, and scalable electronic applications.

Index Terms –**Low power memory, Leakage current reduction, High-density storage, DRAM, SRAM, Flash memory, Embedded systems**

I. INTRODUCTION

In the field of electronics and communication engineering, information processing and storage form the backbone of every modern system. Every piece of information—whether it is audio, video, image, or text—is stored in digital form, represented as binary values. Binary, consisting of the two symbols ‘0’ and ‘1,’ is the fundamental language of digital electronics. At the core of this binary representation lies the memory system, which is responsible for storing and retrieving information as needed by the processor or controller. Without efficient memory concepts, the design and functioning of electronic gadgets such as smartphones, computers, microcontrollers, and embedded systems would not be possible.

A memory device can be visualized as a collection of millions or even billions of small storage units known as memory cells. Each cell is designed to hold a single binary bit, either ‘0’ or ‘1.’ These cells are typically fabricated using semiconductor materials, most commonly silicon, due to its favorable electronic properties. In advanced designs, these cells are arranged in arrays, enabling structured access and efficient organization of data. The way data is stored, accessed, and manipulated defines the overall speed, efficiency, and cost-effectiveness of an electronic system.

For example, in the case of images, the information is represented as pixels. A pixel itself is composed of binary values, and millions of such pixels combine to form a digital image. To optimize storage, these binary values are often compressed before being written into memory. Similarly, audio and video signals are digitized, compressed, and stored in binary form. This highlights the vital role of memory technologies in enabling the storage and processing of vast amounts of multimedia data in modern applications.

The evolution of memory technologies has been driven by the increasing demand for devices that are compact, power-efficient, fast, and capable of handling large-scale data. Over the decades, researchers and industries have introduced different memory architectures, each with its own set of advantages and limitations. Among these, Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), and Flash memory are some of the most widely used technologies. These memories have been instrumental in shaping the design of embedded systems, microcontroller-based applications, and ultra-large-scale integration (ULSI) devices.

Dynamic Random Access Memory (DRAM): DRAM is well-known for its high storage density and scalability. Each memory cell in DRAM typically consists of a capacitor and a transistor, which allows for compact cell size. However, one of the major drawbacks of DRAM is that the capacitors gradually lose their charge, requiring periodic refreshing to maintain data integrity. This refresh operation leads to increased power consumption and latency, making DRAM less efficient in energy-constrained systems. Nonetheless, DRAM remains the preferred choice in main memory applications where high density is crucial.

Static Random Access Memory (SRAM): Unlike DRAM, SRAM does not require refreshing since it uses a bistable latch configuration to store each bit. This results in faster access times and lower latency, making SRAM highly suitable for cache memory and high-speed applications. However, the cell structure of SRAM typically requires six transistors, making it significantly larger than DRAM cells. Consequently, SRAM has lower density and higher leakage currents, which limit its scalability in ultra-dense memory architectures.

Flash Memory: Flash memory has become the dominant non-volatile memory technology, meaning it retains stored data even when power is removed. It is widely used in portable devices, USB drives, solid-state drives (SSDs), and embedded systems. Flash memory offers the advantage of cost-effectiveness, durability, and compactness. However, it suffers from relatively slower write and erase cycles, as well as limited endurance due to degradation of the floating-gate transistors after repeated use. Despite these limitations, flash memory continues to evolve, offering higher densities and improved performance with advancements in fabrication techniques.

The design of modern embedded systems demands memory technologies that balance multiple critical parameters: low power consumption, reduced leakage current, high storage density, radiation tolerance, scalability, and speed. The choice of memory depends on the nature of the application. For instance, battery-powered systems prioritize low power and non-volatility, while high-performance computing systems emphasize speed and density.

This paper focuses on exploring the characteristics, strengths, and weaknesses of DRAM, SRAM, and Flash memory in the context of modern electronic and microcontroller-based applications. Furthermore, the discussion highlights the latest developments and new concepts aimed at addressing the challenges of low leakage, high density, and power-efficient operation. By comparing and analyzing these technologies, this study provides valuable insights into the selection and optimization of memory systems for next-generation embedded designs.

1.DRAM:

In DRAM (Dynamic random-access memory) each memory unit is made up of two components a transistor and a capacitor. It is a type of RAM this stored information is volatile. When a bit needs to be stored in memory, the transistor is used to charge or discharge the capacitor. A charged capacitor represents a logic high, or '1', while a discharged capacitor represents a logic low, or '0'. The charging/discharging is done through the word line and bit line. During a read or write operation, the word line goes high and the transistor connects the capacitor to the bit line. Whatever value is on the bit line ('1' or '0') gets stored or retrieved from the capacitor. One thing is that charge leakage happens in capacitors, to maintain the data stored in the memory the capacitors must be refreshed periodically.

As the technology grows, the computation exponentially grows and the data transfer between the components should occur instantaneously without much delay. Along with this, one needs to keep power consumption as low as possible. Therefore, future ultra-high-density memory devices should operate at low power to process huge data. 3D-stacked DRAMs with TSVs can be used to address these kinds of issues but it suffers from a loss of refresh power, which alters the process of data.

Ho Hyun Shin et al. proposed a new scheme, EXTREME, which significantly reduces the refresh power [1]. A simple page table manager is demonstrated at the logic die of 3D-stacked DRAM devices, to retain the compatibility with OS, which reduces the refresh power by almost 98% at idle with 16 KB of SRAM and 64 KB of DRAM register overhead for a 2 GB 3D-stacked DRAM device. This method is convenient for current computing because it only modifies the OS without modification to the DRAM controller. EXTREME can reduce refresh power along with this hardware design which reduces the refresh control logic.

Flash memories are more sensitive to radiation effects due to the direct interaction of ionizing radiation with their stored charge. A new type of resistance-based storage of RAMs which is high-density, radiation tolerant non-volatile memory is introduced. M. J. Marinella et al. proposed a material and device physics, fabrication, operational principles, and commercial status of scaled 2D flash, 3D flash, and emerging technologies of different types of flash memories which leads to the way for future high-density radiation tolerant non-volatile memory. Advanced charge storage memories, such as scaled SONOS are significantly more flexible, withstanding TID (total ionizing dose) levels of 300-500 krad (Si) and upset cross sections starting at an LET of about 20 MeV·cm2 /mg [2]. Emerging resistance change memory technologies such as MRAM, ReRAM, CBRAM, and PCRAM are relatively not much affected due to ionizing radiation, single event effects, and displacement damage as there is not a direct mechanism for interaction between radiation and the storage mechanism.

In most computer systems, DRAM is used to design the main memory, and the hard disk HDD is used for secondary storage. Due to the volatile nature of DRAM, the main memory may suffer from data loss in the event of power failures or system crashes. Due to the development of new types of non-volatile memories (NVRAM) such as PCM, Memristor, and STT-RAM, maybe in the future one of these technologies will replace DRAM as main memory. In an NVRAM-based buffer cache, any updated pages can be stored longer than usual without the urgency to be copied to HDDs.Zi qi Fanet al.,propose a buffer cache policy, named I/O-Cache, using Belady’s algorithm and Least Frequently Used (LFU) algorithm that regroups and synchronizes long sets of sequential dirty pages to take advantage of HDDs' fast sequential access speed and the non-volatile-property-of NVRAM [3].A new policy can dynamically separate the whole cache into a dirty cache and a clean cache, according to the characteristics of the workload, to reduce storage writes, also this is evaluated using various traces. The experimental results show that I/O-Cache shortens I/O completion time, decreases the number of I/O requests, and there is improvement in the cache hit ratio compared with existing cache memories.

Here is a new concept of testing the DRAM characteristics with the help of SoftMC. It isFPGA based DRAM test solution.Maosong Ma et al.proposed that FPGA can test many parameters of DRAM. The flexibility and programmability of FPGA help in understanding the DRAM characteristics [4].

DRAM always has leakage current so to calculate this, Min-Hee Cho et al., proposed TF slope.DRAM memory Cell Transistor Leakage Current is calculated from the slope of the retention time-fail bit plot (defined as TF slope)[5]. A steep slope indicates a narrow cell leakage distribution, which corresponds to a narrower structural distribution and therefore a large tREF. Any Structural changes lead to an extremely high cell leakage current, which determines DRAM performance such as refresh time (tREF).This is much useful in the manufacturing process of DRAM memory

DRAM consumes more power compared to SRAM. Paramita Chowdhury et al.proposed an SD-DRAM memory cell and it is compared with all 1T, 3T, and 4T DRAM cells. 1T DRAM cell: one transistor DRAM is usually arranged in one capacitor and one MOSFET to store any binary information suchas "0" or "1" as read or write. 3T DRAM cell: it is three transistor DRAM cell, and 4T is four transistor DRAM cell. The super Diode DRAM (SD-DRAM) cellhas a gated diode which is responsible to store charge for Write/Read operation instead of any capacitor,it leads to a better performance in the area of power consumption.1T DRAM cell has fast write access compared to other designs and 4T DRAM gave fast read access response compared to other designs. For the write/read power consumption scenario SD-DRAM is the best one for reduced power [7].

To achieve high memory capacity and good radiation tolerance in DRAM memory cells, Anthony Agnesina et al.,demonstrated a radiation-tolerant stacked memory array based on state-of-the-art chip stacking and radiation mitigation technologies.In LOB technology to stack COTS memory dies, they avoid the use of proprietary TSV dies,TSVs are usedonly for interconnection between dies to achieve high memory capacity and good radiation tolerance [8].

To reduce refreshtime,capacitor-less DRAMs like MSDRAM, A2RAM, and Z2FET are compared byFrancisco Gamiz et al.,they stated that The MSDRAM (Meta-Stable DRAM) memory cell uses the double-gate action in regular FD SOI MOSFETs,namely the dynamic coupling between front and back interfaces.The Z2FET (Zero-ionization, Zero-swing FET) is a forward-biased PIN diode with the undoped channel partiallycovered by the front gate. The A2RAM memory cell was proposed in 2011 as a new device with potential application as capacitor-lessDRAM [9]. Nowadays they are found in Revolutionary Embedded Memory for Internet of Things Devices.

To deal with the area and latency overhead problem of DRAMFazal Hameed et al.,propose a block-based DRAM LLC design that decouples tag and data into two regions in DRAM. In this design,it stores the tags in a latency-optimized DRAM region as the tags are accessed more often than the data. In contrast, we optimize the data region for area efficiency and map spatially-adjacent cache blocks to the same DRAM row to exploit spatial locality.It is proposed that tag-data decoupled LLC improves system performance by 11.7% compared to a direct-mapped LLC design and by 7.2% compared to an existing associative LLC design [10].

TABLE-1 SHOWS A COMPARISON OF CERTAIN PARAMETERS OF DRAM

Radiation tolerant	**Refresh time Using EXTREME technology [1].**	**Refresh power**	**Cache hit ratio**	**System Performance (low latency) Comparison with existing LLC [10]**
2D floating gate (low)[2].	In 32 GB 16ms	In 32GB refresh power is reduced by 35% [1].	Web proxy and LRU are compared 13.2% more compared to LRU [2].	In Tag, data decoupled LLC 11.7% Improvement.
3D floating gate (low)[2].				In direct mapped LLC design 7.2% improved.
Toggle MRAM ReRAM CBRAM PC-RAM STT-MARAM (high)[2].	In 64GB 32ms	In 64 GB Refresh power is reduced by 47%[1].		

2.

SRAM:

SRAM (static random-access memory) is also a type of RAM and data stored in this is volatile. Data information is stored in the form of a binary. A memory cell is made up of flip-flops constructed using either TTL or ECL logic which consumes more power, and MOSFET (uses CMOS) logic which consumes relatively less power. Where ever battery concept is impractical there must be a requirement to design NVSRAMs such as in aerospace, medical, and networking application where the preservation of data is very important.

CNN(convolutional neural network) is one of the popular algorithms when it comes to image recognition, which is one of the most dominating applications of machine learning. Traditional SRAM can only read/write one byte at a time, this slows down the training process of CNNs. Xiaowei Chen et al.proposed a high-speed SRAM mainly designed for CNN. Here SRAM can read/write 1 byte to 4 bytes at a time in one single clock cycle and increases memory access speed up to 4 times compared to traditional memory. This SRAM has 8×32×32 bits, which is 1 KB. The SRAM is composed of 32 SRAM blocks (8 column×32 rows each) also the 1KB traditional SRAM is compared with the new architecture of SRAM using simulation and found that the proposed SRAM has a power overhead of 9.04% and an area overhead of 17.57%, which is comparatively low considering the SRAM access speed [11]. Moreover, the access speed is much more of a concern than power and area for CNN applications. The proposed SRAM reaches a very good trade-off between speed, power, and area.

Certain SRAM consumes maximum power and space area on a chip so to reduce the factors mentioned Chinmay Sharma et al., proposed a reversible design of a 4-bit 6-T SRAM array at 180nm-1.8V CMOS technology which achieves an 8% reduction in energy consumption of the circuit [12]. DNA computing, quantum computing, and ultra-low power CMOS design are the key areas of its applications.

The SRAM is used to store certain confidential contents, sosecurity issues are more, therefore, Weng-Geng Ho et al., proposed a comparative analysis of a fabricated 65nm CMOS SRAM chip and 4 commercial SRAM chips, e.g., Alliance, Lyontek, Cypress, and AMIC in terms of security vulnerability. In this, they use satellite images as the stored data and reveal the stored image, i.e., 16.1% in the 65nm CMOS SRAM, 16.2% in the Alliance SRAM, and 21% in the Lyontek SRAM [13]. The revealed images are identified in the above-mentioned SRAMs but are hidden in the Cypress and AMIC SRAMs.This is one of the techniques used to design SRAM chips to avoid security vulnerability.

In SRAM it is always necessary to reduce leakage current and power dissipation. Vishal Gupta et al., Proposed a supply voltage management technique for designing a low-power and flexible SRAM cell. They propose a FinFET-based differential 10T SRAM cell using Drowsy Cache architecture for leakage power reduction at a 45nm technology node. The said differential 10T SRAM permits bit furnished with column-wise write access control, having a differential read path, thus, improving the performance of the SRAM cell [14]. The simulation is carried out on Cadence Virtuoso at a 45nm technology node. The suggested design is therefore an attractive choice for low-power application at a 45nm technology node. It reduces the power budget of digital systems by decreasing the leakage power at 45nm technology.

Nowadays low power consumption is an important factor in designing almost all portable electronic devices. Therefore, designing SRAM with low power consumption is one of the key points so A. S V S V Prabhu Deva Kumar et al. proposed a 6T SRAM Memristor with 45nm process technology and advanced CMOS / VLSI memory [15]. This technique reduces the stored data limit without a power supply and also the leakage current.

Advanced CMOS SRAM memory chips are proposed by Surbhi Bhart et al., who used FGMOS and include it in 6T SRAM in 90 NM Technology employing under gpdk 090 (generic process design kit) using Cadence virtuoso simulation [16]. It has been evaluated for comparative analysis and is used in high-speed, low-power appliances.

The Internet of Things is one of the popular technologies in the current era. It allows the connection of various sensors, devices, and everyday objects to interact with each other. Today, many devices which paved the way for the advancement of smart homes to smart cars are connected through IoT networks. Ashwija Reddy Korenda et al. proposed a proof of concept for using SRAM-based Physically Unclonable Functions (PUFs) to generate private keys for IoT devices. PUFs are utilized, as there is inadequate protection for secret keys stored in the memory of the IoT devices. We utilize a custom-made Arduino mega shield to extract the fingerprint from the SRAM chip on demand. SRAM PUFs depend on the flipflop logic and lack perfect symmetry, it is considered a weaker PUF compared to some other memory-based PUFs (e.g., ReRAM-based PUF). However, it's a common NV technology available in several IoT devices and offers an easy and accessible technology to explore [17].

SRAM and flash are the predominant memory types embedded into microcontrollers. Typically, flash memory is used to store boot and application code, device configuration parameters, and lookup tables for constants as well as storage of learning parameter personalization information. SRAM serves as the working memory space for the application data as well as processor-local storage in the form of instruction and/or data caches plus tightly coupled memories. T. Jew et al. proposed some of the aspects of the applications which drive how much embedded SRAM and flash memory are required as well as how these memories are embedded in a microcontroller [18].

During the manufacturing process, the SRAM may be affected by resistive defects, this leads to dynamic faults. G. Medeiros et al., the proposed impact of temperature on dynamic fault behaviour [19]. During manufacturing tests of SRAM cells affected by weak resistive defects [20]. The proposed analysis has been performed using SPICE simulations adopting a 20nm FinFET compact model. This is useful to get more memory capacity on a system on a chip.

TABLE -2 SHOWS A COMPARISON OF THE PARAMETERS OF DIFFERENT SRAM MEMORIES

Power consumption [12].		**Power dissipation (mV) [11].**		**Read access time (ps) [11].**	**Security vulnerability [13].**		**Leakage current is reduced by [14].**	
Traditional SRAM	1.66 mV	Conventional SRAM	1.8mW	39.99	65 nm CMOS SRAM	16.1%	FinFET based differential 10T SRAM cell	30.59%
					Alliance SRAM	16.2%		
Proposed SRAM	1.8 mV	Reversible array SRAM	1.005mW	150.4	Lyontek SRAM	21%	FinFET based conventional 10T SRAM cell	53.6%
6T SRAM CMOS [15]	48.27E-9	6T SRAM CMOS [15]	77.38E-3	-	-	-	6T SRAM CMOS [15]	5.550E-12
6T SRAM memristor [15]	15.63 E -6	6T SRAM memristor [15]	650.8E-3				6T SRAM memristor [15]	2.528E-12

3.

FLASH MEMORY:

Flash memory is an electronic non-volatile computer memory storage medium that can be electrically erased and reprogrammed. The two main types of flash memory, NOR flash and NAND flash, are named for the NOR and NAND logic gates. Both use the same cell design;they consist of floating gate MOSFETs.Flash memory evolved from erasable programmable read-only memory (EPROM) and electrically erasable programmable read-only memory (EEPROM). Flash is technically a variant of EEPROM, but the industry reserves the term *EEPROM* for byte-level erasable memory and applies the term *flash memory* to larger block-level erasable memory.Flash memory is widely used for storage and data transfer in consumer devices, enterprise systems, and industrial applications. Flash memory retains data for an extended period, regardless of whether a flash-equipped device is powered on or off.

As the cell density increases in NAND flash memories, memory cell shows the problem of increased parasitic capacitance between the cells. This problem is generated by the floating-gate interference during cell operation. To reduce the floating gate interference, it is necessary to adopt low-k dielectric material. Daewoong Kang et al. proposed an air spacer that has the lowest dielectric constant. Here they applied the air space technology on a poly-Si/Wsix stack gate of 90 nm design-rule NAND flash dynamic faults device for the first time, which improved the cell operation characteristics [21]. The 1G bit NAND flash cell using the air spacer was successfully fabricated. It could improve the on-cell current, and program speed compares to the SiN and oxide spacer.

In this Doo-Hyun Kim, proposed 1Tb 4b/cell NAND flash memory successfully developed and manufactured using 92 stacked Word Lines. 3D flash memories manufactured using 92 stacked WLs has 18 MB/s write throughput, 110us read latency and 1.2Gb/s IO speed. The program and memory read operations are increased by 33% and 24%, respectively by increasing cell characteristics along with reliability criteria. The chip achieved 7.53 Gb/mm2 of areal density reduced by about 25% compared to previous memories designed with 64 stacked Word lines [22].

In this work, Bo Wang et al., analysed a new 3D NAND flash doping structure to solve the minority carrier generation issue. The n-source/drain and p-substrate can provide electrons and holes as majority carriers, respectively. This structure shows no obvious weakness in Power efficiency and also shows a good read performance without a p-n junction in the conductive path. It gives an optimized doping strategy for vertical-channel three-dimensional (3D) NAND flash giving a faster programming and erasing speed than conventional structure [23].

The characteristics and mechanism of the TRE (Temporary read errors) in 3D NAND Flash are investigated in this work by Shiyu Xia et al., In this work during an idle phase before reading, GBTs are discharging in the poly-Si channel. The ΔGBTs occupancy difference between the first and the second read operation is responsible for the TRE, the larger the ΔGBTs occupancy between the two read operations, the worse the TRE [24]. In this work, the experiments are based on 3D vertical channel charge trapping NAND Flash and are used to calculate TRE.

With the development of 5G networks, more data in the form of machine-generated data will be accumulated and processed in the cloud. The data expansion is expected to reach 175 ZB in 2025. The data expansion will also continue. Storage class memory (SCM) is expected to fill the gap between DRAM and flash SSD Storage. In thisTatsuo Shiozawa et al.,introduced XL-FLASHTM, a cost-effective flash-based SCM, and the XL-FLASH demo drive featuring a low penalty low latency DMA control interface [25]. Here there is an evaluation result of achieving equivalent performance between the in-memory database and the proposed key-value store database using the XL-FLASH demo drive. This result demonstrates the possibility of replacing DRAM with XLFLASH in a key-value store database application, for highly concurrent read-intensive use cases.

ZNS SSDs (Zoned Namespace Solid State Drives) are a new type of SSD that provides various features such as zone concept and host-level flash management. Hojin Shin et al. proposed how these features affect the performance characteristics of ZNS SSDs [26]. Here the observations show that 1) requesting I/Os in a large unit is indispensable in ZNS SSDs to obtain parallelism, 2) workloads can be isolated more effectively compared with traditional SSDs, 3) unexpected performance drop is not monitored, and 4) performance differs based on LBAs (Logical Block Addresses). All these can be utilized when we devise a new algorithm for ZNS SSDs.

Flash memory is implemented using 3D monolithic integration, bykeeping the same operating mechanisms of 2D. Jan Van Houdt et al. proposed a new roadmap by stacking more layers on the same chip. Thistransition from 2D-3D is discussed as well as its main limitations, and some suggestions are given for further scaling of 3D memories [27].

Jihwan Lee et al. proposed a Tiered LSM-based system that is multi-layered with NVM and improves write and read performance. NVM is expected to be the next-evolution secondary storage device. LSM-tree currently has many chances of exploiting NVM, therefore, LSM-tree with NVM has been researched in many ways. First, a Hybrid LSM-based memory system that uses both DRAM and NVM has been investigated.LSM-tree is a write-friendly data structure that organizes hierarchy using log-structured write, write buffering, and merge operations. The well-known LSM-based databases are Bigtable, Apache HBase, Cassandra, Level DB, and Rocks DB.With the emergence of various and enormous data from the web, Internet-of-Things (IoT), and mobile systems, key-value stores play a major role in database systems today [28].The write andread latencies of TLSM are improved up to 34% and 57%, respectively, compared to those of LevelDBNVM. Debao Wei verifies the self-recovery effect of NAND flash by experiments and proposed the concept of relaxation time (tr) based on the self-recovery effect.NAND flash self-recovery effect for blocks with different program/erase stresses is also studied [29]. NAND flash storage data retention error is significantly reduced by increasing the tr value. Experiments show that when tr is 6h, the retention error is reduced by about 60% compared with the retention error under 0h's tr at the same retention days. In addition, as tr increases, the NAND flash self-recovery effect will reach saturation. The experimental results show that when tr is around 2h, increasing tr will not play a significant role in reducing retention error.

The 3D NAND Flash technology has become the state-of-the-art storage medium for many applications ranging from mobile computing and Solid-State Drives (SSD).Cristian Zambelli et al.,Proposed mainly the major reliability challenges in 3D NAND Flash memories by addressing some issues occurring during the manufacturing process that will result in a macroscopic variation of memory metrics like endurance, data retention capabilities, and cross-temperature control. The analysis of the variability will show that some specific topological regions are more sensitive to a reliability threat in peculiar working corners of the memory. Finally, here it is presented a cross-layer approach that causes the use of Flash Signal Processing (FSP) techniques to avoid macroscopic variations of memory with the presented challenges [30].

TABLE-3 SHOWS THE PARAMETERS OF FLASH MEMORY

Technology	**Areal density**	**Program Throughput**	**Refresh time**	**I/O speed**	**Write latency**	**Read latency**
92 stacked WL's[21]	7.53Gb/mm2	18MB/s	110μs	1.2Gb/s		
XL-flash TLSM	-	-	-	-	34% increased	57% increased

II. CONCLUSION

Memory is a fundamental building block of modern electronic and communication systems, enabling the reliable storage and retrieval of digital information. As devices become smaller, faster, and more data-driven, the requirements for memory technologies have expanded beyond simple storage capacity. Parameters such as low power consumption, minimal leakage current, high density, scalability, and efficient data expansion have become critical to meet the growing demands of embedded systems and ultra-large-scale integration.

The discussion of SRAM, DRAM, and Flash memory reveals that each technology offers unique advantages while facing specific limitations. SRAM provides speed and low latency but struggles with density and leakage issues. DRAM achieves high density but consumes more power due to its refresh cycles. Flash memory ensures non-volatility and cost-effectiveness but is constrained by endurance and slower write operations. To address these challenges, ongoing research introduces advanced techniques to lower power usage, reduce leakage, enhance data storage density, and enable flexible memory expansion.

In conclusion, the optimization of memory technologies is essential for the continued advancement of microcontroller-based systems, portable devices, and next-generation embedded applications. By integrating innovative concepts in DRAM, SRAM, and Flash, it is possible to achieve cost-effective, power-efficient, and scalable memory solutions, paving the way for reliable and high-performance electronic systems in the future.

III. ACKNOWLEDGMENT

The authors sincerely acknowledge the unwavering support and guidance of their esteemed mentor and supervisor. Their expert advice, constructive feedback, and consistent encouragement have been crucial at every stage of this research. The technical insights and thoughtful suggestions provided not only enriched the quality of the work but also helped overcome challenges during the study. The authors are deeply grateful for their valuable time, mentorship, and dedication, which played a significant role in the successful completion of this project.

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