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Design and Analysis of 15 Transistor SRAM Bit - Cell

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Abstract : Power dissipation for nano scale VLSI design is one of the most important perseverance of current. In which continuous transistor scaling with the in growing demand for low powder application for the low voltage coupled circuit. This design expose to environmental condition where vulnerable circuit are the memory, cover the large area silicon dye and storage to critical data. Radiation hardening is one of the most useful for environment condition embedded memory blocks. In various field of application for ultralow powder is of immense important in VLSI chip designing with the reference of 13Transistor SRAM. Radiation hardening of implemented memory block is simply achieved through extremely large cell of bit or redundant array and that maintaining to relatively low power and operating high voltage. In this significant power consumption first four radiation hardened a static random excess memory (SRAM) for high soft error and robust to bit cell low voltage functionality. The proposed is 15Transistor SRAM separated feedback mechanism to apply a novel dwell driven was design and fabricate in 180nm CMOS process. On the basis of the effect single event Latch Up (SEL), Single Event Upset (SEU) and Single Event Transient (SET). Transient current and voltage that arises due to current generating from charge particle are term as SET. In this paper, design simulation of and analysis of radiation harden 15Transistor SRAM is very useful for the market. The total power consumption of 15Transistor SRAM cell is 121.29pw. It is lesser than as compare to my rest paper of 13Transistor SRAM and total power dissipation reduce 33.5% of the total chip of base paper 13Transistor SRAM.

IndexTerms **– SRAM, Transistor, Bit, Cell, SEL, SEU.**

I. INTRODUCTION

SRAM bit cell is motivation from energy constraint. For low power devices, power dissipation should be as low as possible. we know that static power is negligible of the CMOS device which is possible only in static random access memory but not in dynamic random access memory because, DRAM required refresh, again and again, so static power consume more in dram such as SRAM. SRAM is a permanent memory of the computer that is also called cache memory. SRAM designed by combination of two cross-coupled inverters where access transistor of the word line, the bit line connected to input and output. Standard 6Transistor SRAM in beginning was very useful to memory and speed of operation also more as compared to other memory but that is a big problem for space application because there are limited available energy resources and radiations are also occurs, so memory operation, read and write, disturbed due to radiation, not perfectly operated to memory operation. To realize for reduce radiation effect from a different technology.

We designed a 15Transistor SRAM bit cell radiation-hardened chip for use in space application, military, where available energy resources are limited. 15Transistor SRAM designed to motivate through 13Transistor SRAM radiation hardened for space application for ultra-low power.

In 15Transistor SRAM cell, we added two NMOS transistors, when two or more transistors are in series combination then subthreshold leakage current decrease and critical node power increase, since critical node power increase then a charge will also increase. Collection charge of hit high energetic particle is less as compared to the critical charge of the critical node, then radiation effects only a particular node but bot whole circuit. So, we find that write operation affected by radiation in a particular node, that is very effective to 13Transistor cell and also reduced 33% total power consumption of 15Transistor SRAM circuit.

Chip designers must keep in there mind the power dissipation level of these handheld devices. In recent times consumer electronic market is flooded with wireless gadgets, a crucial challenge for these gadgets are need for total power consumption. A combination of a minimum of six transistors is used in designing of Static random-access memory (SRAM) cell. In present-day SoC circuit designing, SRAM is one of the most often used blocks. For the purpose of high robustness and speed in a digital circuit, SRAMs are normally integrated with CMOS. In modern-day memory implementation, SRAMs are the favourite choice.

Radiation hardening is resistant to damage or malfunctions of electronic component and system caused due to ionizing radiation (particle radiation and high energy), such type of radiation are encountered in high-altitude flight, around the nuclear reactor, outer space, and particle accelerator. Most semiconductor devices are susceptible to radiation damage; since susceptibility to radiation damage could be reduced by using some innovative design and manufacturing variations. radiation- hardened chips are lagging behind

the most recent developments because of its widespread development and testing required to produce a radiation-hardened design of an integrated chip.

Charged particle causes ionization effect. These effects are normally transient and capable of making soft error and glitches. are caused by s and usually transient, creating glitches and soft errors. x-ray and ultraviolet radiation cause photocurrent also fall under this category. These are caused in MOSFET due to the accumulation of hole in the oxide layer.

In applications such as space it is major contributor of overall leakage power. Therefore, we can conclude that by supply voltage scaling static power consumption can be reduced and SRAM can work efficiently. And second thing that we can deduce is that tackling of soft error in SRAM has became very important because SRAM bit cell has higher probability of radiation strike because of the reason that it occupies larger area.

As depicted in Fig.1, general memory cell having six transistor stores data by cross coupling the inverters in active feedback loop. SRAM design is highly sensitive to SEUs, any type of upset can lead to bit flip if the switching threshold of one inverter is crossed by data node of other inverter. During operation at low voltage, due to decreased value of switching threshold SRAM became highly susceptible to soft error. In 6Transistor SRAM bit cell failure due to SEU can be displayed by example. It is assumed that circuit holding logic 1 (Q = VDD and QB = 0 V). The state of QB due to temporarily generated charge, if M3, cut off PMOS drain is striked by some particles of high energy.

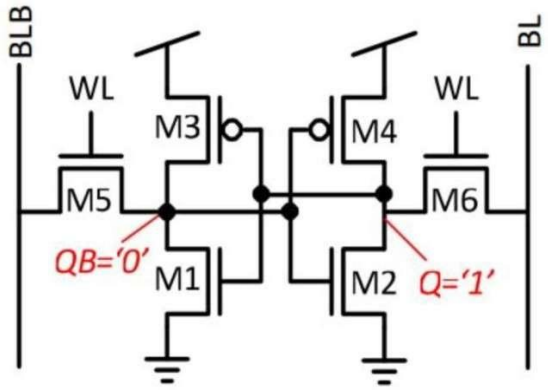

Fig.1 Conventional 6T SRAM cell

For the purpose of notation, opposite to a negative charge that is striked this type of positive chargestriked as a 0 to 1 upset at node QB. Switch of feed forward M2 and M4 switch and Q is discharged. It happen before charge deposited is desertedfrom power supply Before deposited charge can be deserted to the power supply through the conductingtransistor of the feedback inverter (M1). As a result Q.

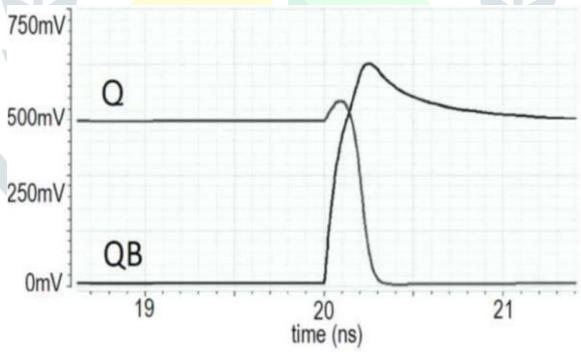

Fig.2 Due to SEU, SRAM bit flip

To exceed critical charge (Qcrit) two orders-of-magnitude smaller than that of the charge can be deposited by an energetic particle strike in space excess charge is required. As we know with scaling and voltage technology critical charge (Qcrit) is decreased. single event upset tolerance of the SRAM is damaged by above discussed trend. Hence, under low supply voltages the normal cross-coupled inverter circuit cannot gain appropriate radiation tolerance. SRAM cell stability is decided by parameter called static- noise margin (SNM). 6Transistor SRAM bit cell is simulated in 180nm CMOS process . It is operated at 500 mV and having margin of ˜ 190 mV approx. bit failure is caused to creation of this margin, a deposit charge of ~ 3. Several hundreds of Fermi to coulomb charge can be deposited in space by charge deposited. Consideration of a cell topology is required to mitigate the problem of particle striking of that amount of charge.

II. PROPOSED WORK AND RESULTS

15 Transistor RadiationHardened Bit Cell

Bit cell design: - The15Transistor SRAM bit cell isdesigned based on the 13TransistorSRAM bit cell, when two more transistors are in the stack, stack aNMOS to the inverter.

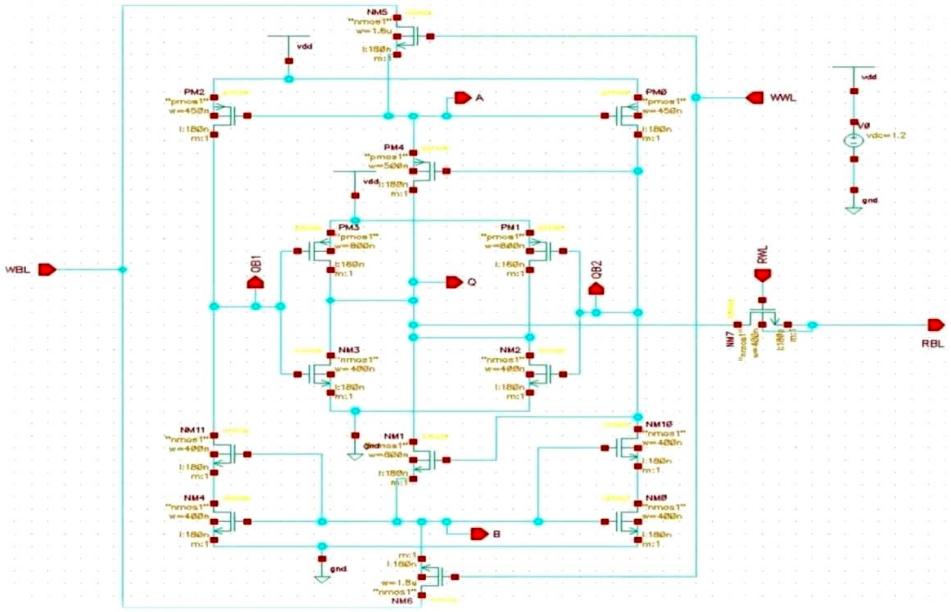

Fig.3. Schematic of 15Transistor SRAM

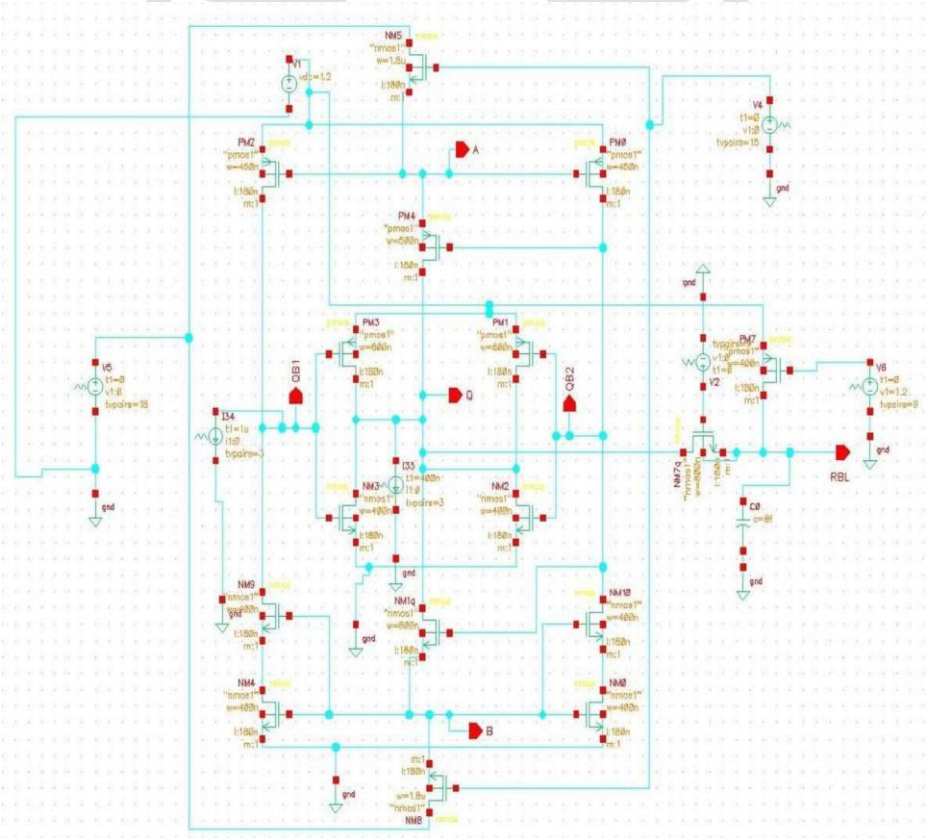

Fig.4 Design of 15Transistor SRAM, positive energetic particle (4mA) at node Qand QB1.

In this above in both figures, TransistorNM10 and transistor NM11 are added with transistor NM0 and NM4, with series, respectively. Due to transistors are NM4 and NM11 in series, and also NM10 with NM0, when any one transistor is off one of them in stack or self reverse bias, then the leakage current of the transistor reduces substantially. The proposed 15Transistor SRAM bit cell is two logs stable state, that is represented by logic 1 and logic 0, such as voltage level at critical node Q.

When a radiation strike at any node of bit cell causes a value change their node since other four internal nodes designed the change can not flip cell bit and that disrupted their recover under recovery time of the cell. For example, SEU at a critical node will readily transform the dual- driven mechanism generated by the intermediate node of the 15Transistor SRAM circuit. Soft error upsets at QB1 andQB2 will not be able to change the state at Q and will return in original state. Detailed analysis of reading operation and WRITE operation in the below section and also analysis of radiation effect on the node Q and QB1, and also their other nodes.

Write Operation

SRAM topologies of standard six transistor bit cell, write data into the storage nodes are driving direct for the new level.so needs to overcome of circuit's strong internal feedback. In this method, the proposed 15Transistor SRAM cell perform write operation by driving the weak feedback nodes A and B, hence removing much of the ratioed maintaining, essential to direct access. Write bit line (WBL) is access to the pair of transistor N5 and N6 to nodes A and B. These transistors are controlled by a write word line (WWL), such that

when WWL is raised (logic "1"), A and B are pulled as respects level driven to WBL. The pairs of NM11, PM2, and NM10, PM0 creates outer inverter of the virtual connection between A and B. Driving nodes QB1 and QB2 to the opposite level of Word Bit Line. According to the written data level, node Q connected dual driven feedback inverters, delivering the cell to a stable state.

Read Operation

In the proposed 15Transistor SRAM bitcell, In this cell contains single-ended readout by the read access transistor (NM7). This device is controlled by a read word line(RWL)and connected to a column read bit line (RBL), with pre charged to the read operation and conditionally discharged of the storage device, where the voltage stored at node Q. Due to the dual- driven feedback that drives Q to its stable value, this read operation is more robust and more speed than the read operation of standard SRAM bit cells. When the access transistor is stronger than the pull-down transistor, read operation defeats in 6Transistor SRAM cells occur due to local variations. The proposed 15Transistor SRAM cell takes advantage of a pair of pull-down transistors NM2 and NM3, which read failure probability is significantly decreased. In addition, this two transistor also contribute a lower resistance pull-down path to accomplish a faster bit line discharge. The separated Read and write ports are separated by two-ported functionality. The majority of the previous proposed 15Transistor SRAM bit cell a single-ended read. In a standard 6Transistor SRAM cell that word lines and bit lines share for both read and write operations.

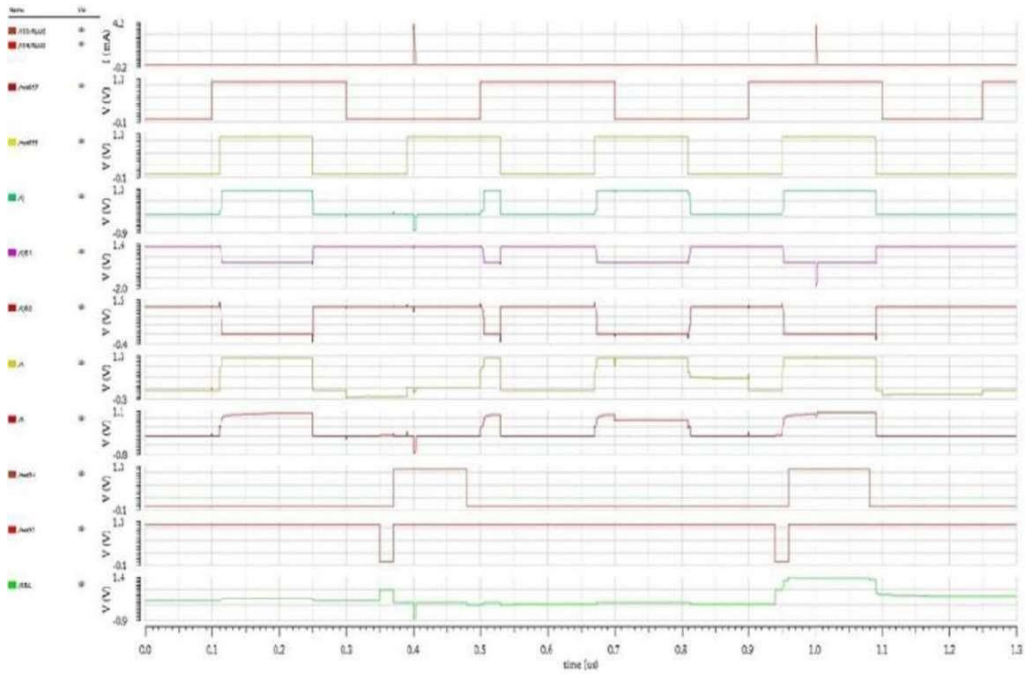

Fig.5. 15Transistor SRAM Read and Write operation due to strike high energeticparticle

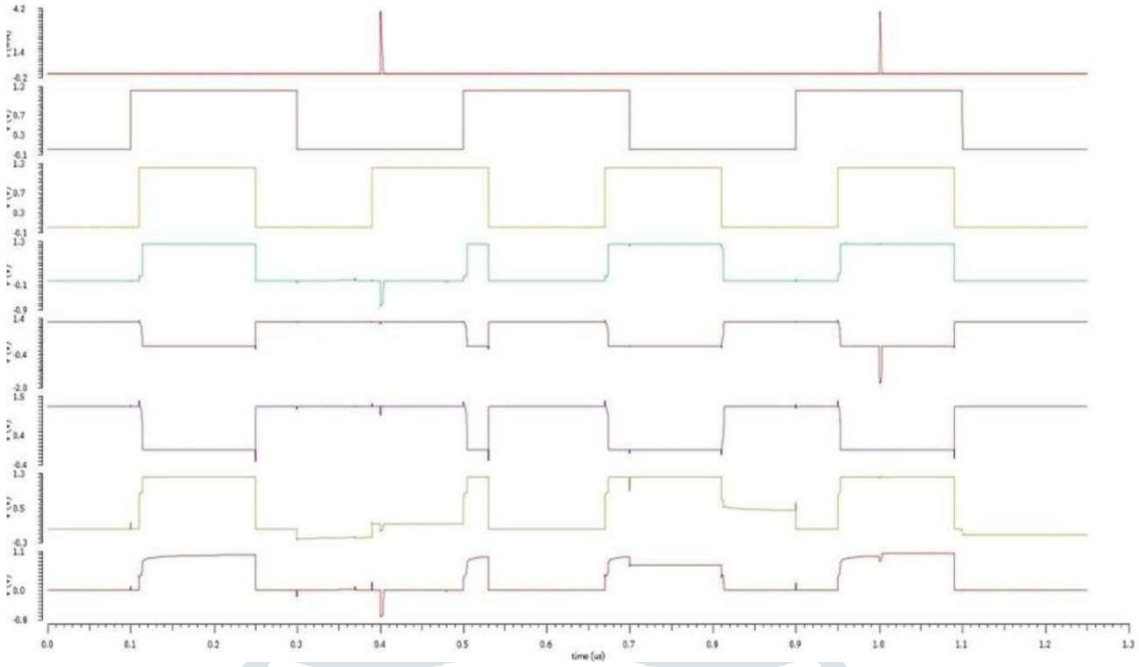

Fig.6. 15Transistor SRAM Read and Write operation, less effect of node Q andQB1 due to high energetic particle

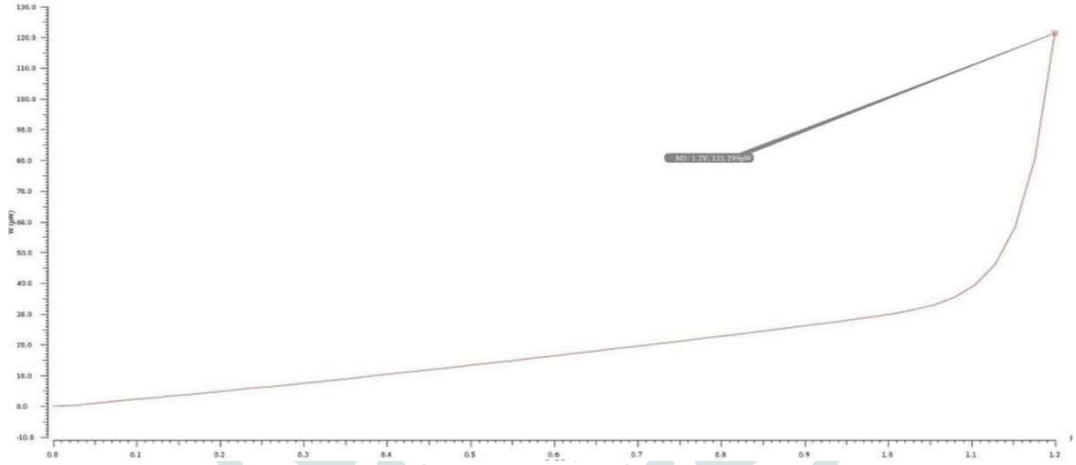

Fig.7. total power consumption in 15Transistor SRAM is 121.29 PW

However, as the read margin is often the limiting factor in supply voltage scaling, the single-ended readout is often used as an alternativeto the standard differential readout.This either leaves the cell susceptible to half-select failures or eliminates theoption of partial row writes—a real problem if bit-interleaving is desired for minimizing the probability ofmultiple-bit failures.

We find in this 15Transistor, upset strike a particle on the multiple nodes, then passes by a semiconductor material and generate in reverse biased junction lone pair ofelectron and hole. When produced electron-hole pair by hit strike particlein unbiased junction, and absence of the electric field. Transient injectedcurrent by a strike on reverse biased. By the double exponential model injected current is I(t)

$$I(t) = \frac{Q_{\text{coll}}}{t_f - t_r}\left(e^{-\frac{t}{t_f}} - e^{-\frac{t}{t_r}}\right)$$

Where Qcoll = it denotes of collectivecharge of strike particle

tr = Rise time consumption and alsopropagation delay.

if = Fall time

The dependency of ionized particlefollows Qcoll, where rise and fall time was taken 10 and 200 ps, respectively.

We find in 15Transistor SRAM reduces total power consumption and also propagation delay. In thisproposed 15Transistor, when striking high energetic particle on the nodethen that radiation tolerance effect is less as compare to 13Transistor SRAM in Write operation, that shownin fig.5, which occurs due to stacking effect because sub-threshold currentreduces in more than one transistorNMOS or PMOS in series.

III. COMPARISION

We find in 15T SRAM reducestotal power consumption and also propagation delay.

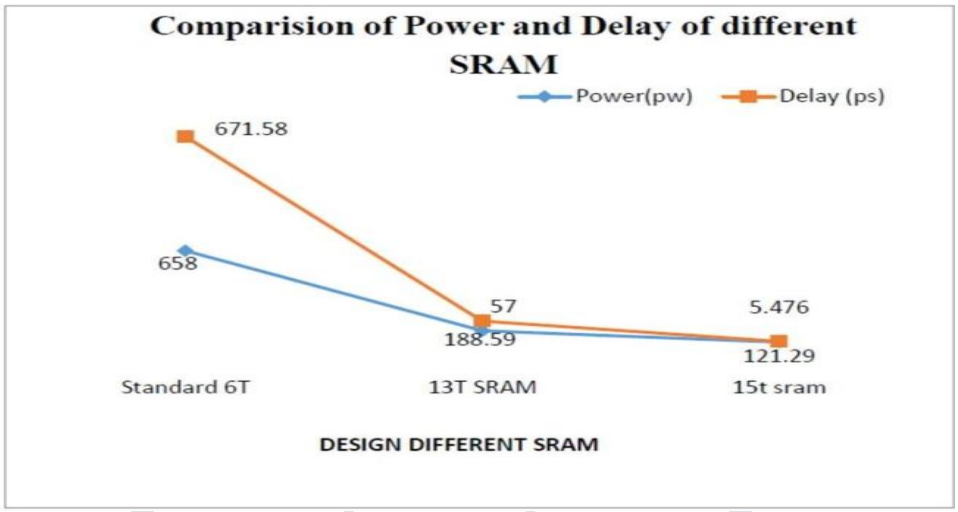

Fig 8: Comparison of different SRAM

IV. CONCLUSION

I found that 15 T transistor reduced 33 percent power compared to 13 T transistor radiation bit cell by adding two transistor in series condition. In future, we know that proposed 15 Ttransistor also design in radiation hardened and layout design by scaling of length and width of transistor, so also reduce consumed power.

REFERENCES

1. Lior Atias, Adam Teman, Robert Giterman, Pascal Meinerzhagen, and Alexander FishA Low-Voltage Radiation- Hardened 13 TRANSISTOR SRAM Bitcell for UltralowPower Space Application, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Feb.2016.
2. Teman, L. Pergament, O. Cohen, and Fish, "A 250 mV 8 kb 40 nm ultralow power 9T supply feedback SRAM (SF-SRAM)," IEEE J. Solid-State Circuits, vol. 46, no. 11, pp. 2713–2726, Nov. 2011.
3. G. R. Srinivasan, P. C. Murley, and H. K. Tang, "Accurate, predictive modeling of soft error rate due to cosmic rays and chip alpharadiation,inProc. IEEE Int. Rel. Phys. Symp., Apr. 1994, pp. 12–16.
4. N. Axelos, K. Pekmestzi, and N. Moschopoulos, "A new low-power soft- errortolerant SRAM cell," in Proc. IEEE Comput. Soc. Annu. Symp.VLSI (ISVLSI), Jul. 2010, pp.399–404.
5. J. S. Shah, D. Nairn, and M. Sachdev, "Asofterror robust 32 kbSRAM macros featuringaccess transistor-less 8T cell in 65-nm," inProc. IEEE/IFIP Int. Conf. VLSI Syst.-Chip (VLSI- SoC), Oct. 2012, pp. 275–278.
6. Y. Shiyanovskii, F.Wolff, and C. Papachristou, "SRAM cell design using tri- state devices for SINGLE EVENT UPSET protection," in Proc. IEEE Int. On-Line Test.Symp. (IOLTS), Jun.2009, pp. 114–119.
7. S. M. Jahinuzzaman, D. J. Rennie, and M. Sachdev, "A soft error tolerant10TSRAM bit-cellwith differential readcapability," IEEE Trans. Nucl.Sci., vol. 56, no. 6,pp. 3768–3773, Dec. 2009.
8. B. H. Calhoun, A. Wang, and A.Chandrakasan, "Modeling and sizing for minimum energy operation insubthreshold circuits," IEEE J. Solid- State Circuits, vol. 40, no. 9, pp. 1778– 1786, Sep. 2005.
9. E. Seevinck, F. J. List, and J. Lohstroh, "Static-noise margin analysis of MOS SRAM cells," IEEE J. Solid- State Circuits, vol. 22, no. 5, pp. 748– 754, Oct. 1987.
10. J. L. Barth, C. S. Dyer, and E. G. Stassinopoulos, "Space, atmospheric, and National Institute of Technology Patnaterrestrial radiation environments,"IEEETrans. Nucl. Sci., vol. 50, no. 3, pp. 466–482, Jun. 2003.
11. C. Peng et al., "A radiation harden enhanced Quatro (RHEQ) SRAM cell," IEICE Electron. Express, vol. 14, no. 18, p. 20170784, 2017.
12. Wang, B. H. Calhoun, and A. P. Chandrakasan, Sub-Threshold Design for Ultra- Low-Power Systems (Series on Integrated Circuits and Systems). Secaucus, NJ, USA: Springer-Verlag, 2006.
13. H.-B. Wang et al., "An area efficient stacked latch design tolerant to SINGLE EVENT UPSET in 28 nm FDSOI technology,"

IEEE Trans. Nucl. Sci., vol. 63, no. 6, pp. 3003–3009, Dec. 2016.

14. B. H. Calhoun and A. P. Chandrakasan, A 256-kb 65-nm sub-threshold SRAM design for ultra-low-voltage operation, IEEE J. Solid-state Circuits, vol. 42, no. 3, pp. 680-688, Mar.2007.
15. P. E. Dodd and F. W. Sexton, "Critical charge concepts for CMOS SRAM," IEEETrans. Nucl. Sci., vol. 42, no. 6, pp. 1764–1771,Dec. 1995.
16. B. H. Calhoun and A. P. Chandrakasan, "A 256-kb 65-nm sub-threshold SRAM design for ultra-low-voltage operation," IEEE J. Solid-stateCircuits, vol. 42, no. 3, pp. 680–688, Mar. 2007.
17. A. Wang, B. H. Calhoun, and A. P. Chandrakasan, Sub-threshold design for Ultra-Low-Power Systems (Series onIntegrated Circuits and Systems). Secaucus,NJ, USA: Springer-Verlag, 2006.