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ANALYSIS AND DESIGN OF MODULATION TECHNIQUES APPLIED TO AN ASYMMETRICAL 31-LEVEL INVERTER

[1] Abhilash Gujjar, [2] Dr. Madhusudhana J
[1] M.Tech Student, [2] Associate Professor,
[1] Department of Electrical Engineering,
UVCE , Bangalore University, Bangalore, India.

Abstract : Multilevel inverters are widely used in high power and high voltage applications. These inverters have many advantages over two-level inverters in terms of harmonic contents, voltage stress, electromagnetic interference etc. But it has some disadvantage as increased number of power electronic switches, driver circuits and voltage sources. The increase in need of power conversion technology inspirits multilevel converters emerge as a solution to overcome demerits of power ratings in conventional methods of power converters. A new cascaded multilevel inverter topology has been developed with a focus to overcome all the disadvantages mentioned. In this topology number of switches required in current path for a level in output voltage has been reduced and requirement of other parameters is also reduced.

Therefore, the overall cost and the space for installation is reduced as compared to traditional topologies like Cascaded H-bridge, Flying Capacitor, Modified H-bridge inverter and series connected inverter etc. Proposed multilevel inverter structure can generate 127 level in output voltage by using only three basic unit in cascading manner. The proposed construction is designed and simulated by MATLAB Simulink software.

The proposed 31 level inverter circuit is designed and simulated by equal phase angle and half height modulation technique

Index Terms - *multi-level inverter, equal phase angle method ,half height modulation technique, THD .*

I. INTRODUCTION

Multilevel inverters can meet the increasing demand of power rating and power quality which is associated with reduced harmonic distortion and lesser electromagnetic interference. The conventional multilevel inverter (MLI) topologies can be categorized in three chief topologies as diode clamped, flying capacitor and cascaded H-bridge multilevel inverter. Among these three topologies, cascaded H-bridge (CHB) multilevel inverter have received special attention because of simple control technique, modularity in structure and easiness in extending the number of levels in output voltage. In recent years, research in the field of multilevel inverters revolve around the minimization of number of switches, total harmonic distortion (THD), voltage stress and conduction losses. Many researchers have presented new structure with reduced number of switches and voltage sources for different applications.

In symmetrical topology, magnitudes of dc voltage sources are same whereas in asymmetrical multilevel inverter different dc voltage source has different magnitude. Asymmetric topology requires less number of switch as compared to symmetrical topology. Asymmetrical design with increased levels improves output voltage harmonic distortions which are within the percentage nominal's that are regulated by IEEE standards. This paper proposes a new asymmetrical 31-level inverter design, simulated with MATLAB Simulink. Let us discuss the proposed inverter circuit design.

II. DESIGN AND OPERATION OF THE CIRCUIT

A new MLI topology with reduced counts of switches and voltage sources has been presented in this paper. The basic unit for proposed inverter has been shown in Fig.1. This can generate seven level in output voltage waveform and comprised of two different magnitude voltage sources with six power electronics switches. Switch $S_{2,1}$, $S_{4,1}$ and $S_{5,1}$ are bidirectional switches that allow the current to flow in either direction and can block the voltage in either direction. All other three switches are unidirectional switches. By selecting the proper magnitude of the voltage sources, all the level can be obtained in output voltage waveform. For basic unit, the magnitude of dc voltage sources $V_{1,1}$ and $V_{2,1}$ should be in the proportion of 1:2.

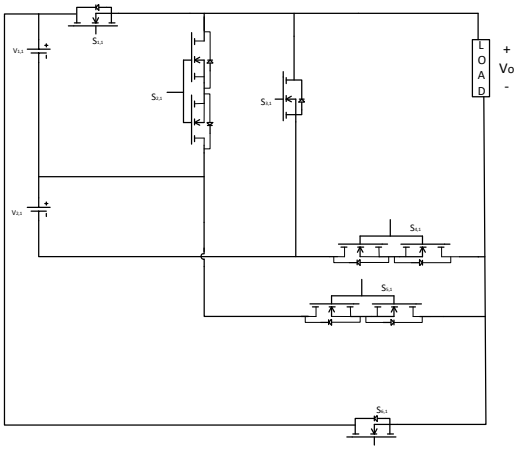

Fig 1. Basic unit

S_1	S_2	S_3	S_4	S_5	S_6	v_o
1	0	0	1	0	0	$V_{1,1}+V_{2,1}$
0	1	0	1	0	0	$V_{2,1}$
1	0	0	0	1	0	$V_{1,1}$
1	0	0	0	0	1	0
0	1	0	0	0	1	$-V_{1,1}$
0	0	1	0	1	0	$-V_{2,1}$
0	0	1	0	0	1	$-(V_{1,1}+V_{2,1})$

Table 1: Switching table for proposed basic circuit

The switches combinations for basic unit to generate all the levels in output voltage waveform are given in Table I. In this,1 indicates the conducting state of the switch and 0 indicate the non conducting state of the switch. At a time, two switches are in conducting states for obtaining the desired level in output waveform. From Table I, it can be depicted that for producing more level in output waveform magnitude of voltage source should be different. Higher number of levels can be obtained by connecting several basic units in series as shown in Fig. 2. The magnitude of the DC voltage source in n^{th} unit can be found as:

Unit-I

$$V_{1,1}=V_{dc} \quad (1)$$

$$V_{2,1}=2V_{dc} \quad (2)$$

Unit-II

$$V_{1,2}=4V_{1,1}=4V_{dc} \quad (3)$$

$$V_{2,2}=4V_{2,1}=8V_{dc} \quad (4)$$

Unit-III

$$V_{1,3}=4V_{1,2}=16V_{1,1} \quad (5)$$

$$V_{2,3}=4V_{2,2}=32V_{2,1} \quad (6)$$

Unit-n

$$V_{1,n}=4V_{1,n-1}=4^{n-1}V_{1,1} \quad (7)$$

$$V_{2,n}=4V_{2,n-1}=4^{n-1}V_{2,1} \quad (8)$$

In general, the number of voltage sources (N_{source}), number of power electronic switches (N_{switch}), number of output voltage level (N_{step}) and maximum output voltage ($V_{o,max}$) can be determined as follows:

$$N_{source}=2n \quad (9)$$

$$N_{switch}=6n \quad (10)$$

$$V_{o,max}=V_{2,n}+V_{2,n-1} \quad (11)$$

$$N_{step}=2^{2n+1}-1 \quad (12)$$

Here, *n* is the number of basic units connected in cascading manner.

Vtg level	S 1,1	S 2,1	S 3,1	S 4,1	S 5,1	S 6,1	S 1,2	S 2,2	S 3,2	S 4,2	S 5,2	S 6,2
-15	0	0	1	0	0	1	0	0	1	0	0	1
-14	0	0	1	0	1	0	0	0	1	0	0	1
-13	0	1	0	0	0	1	0	0	1	0	0	1
-12	1	0	0	0	0	1	0	0	1	0	0	1
-11	0	0	1	0	0	1	0	0	1	0	1	0
-10	0	0	1	0	1	0	0	0	1	0	1	0
-9	0	1	0	0	0	1	0	0	1	0	1	0
-8	1	0	0	0	0	1	0	0	1	0	1	0
-7	0	0	1	0	0	1	0	1	0	0	0	1
-6	0	0	1	0	1	0	0	1	0	0	0	1
-5	0	1	0	0	0	1	0	1	0	0	0	1
-4	1	0	0	0	0	1	0	0	0	0	0	1
-3	0	0	1	0	0	1	1	0	0	0	0	1
-2	0	0	1	0	1	0	1	0	0	0	0	1
-1	0	1	0	0	0	1	1	0	0	0	0	1
0	1	0	0	0	0	1	1	0	0	0	0	1
1	1	0	0	0	1	0	1	0	0	0	0	1
2	0	1	0	1	0	0	1	0	0	0	0	1
3	1	0	0	1	0	0	1	0	0	0	0	1
4	1	0	0	0	0	1	1	0	0	0	1	0
5	1	0	0	0	1	0	1	0	0	0	1	0
6	0	1	0	1	0	0	1	0	0	0	1	0
7	1	0	0	1	0	0	1	0	0	0	1	0
8	1	0	0	0	0	1	0	1	0	1	0	0
9	1	0	0	0	1	0	0	1	0	1	0	0
10	0	1	0	1	0	0	0	1	0	1	0	0
11	1	0	0	1	0	0	0	1	0	1	0	0
12	1	0	0	0	0	1	1	0	0	1	0	0
13	1	0	0	0	1	0	1	0	0	1	0	0
14	0	1	0	1	0	0	1	0	0	1	0	0
15	1	0	0	1	0	0	1	0	0	1	0	0

Table 2 : Switching table for the 31 level inverter

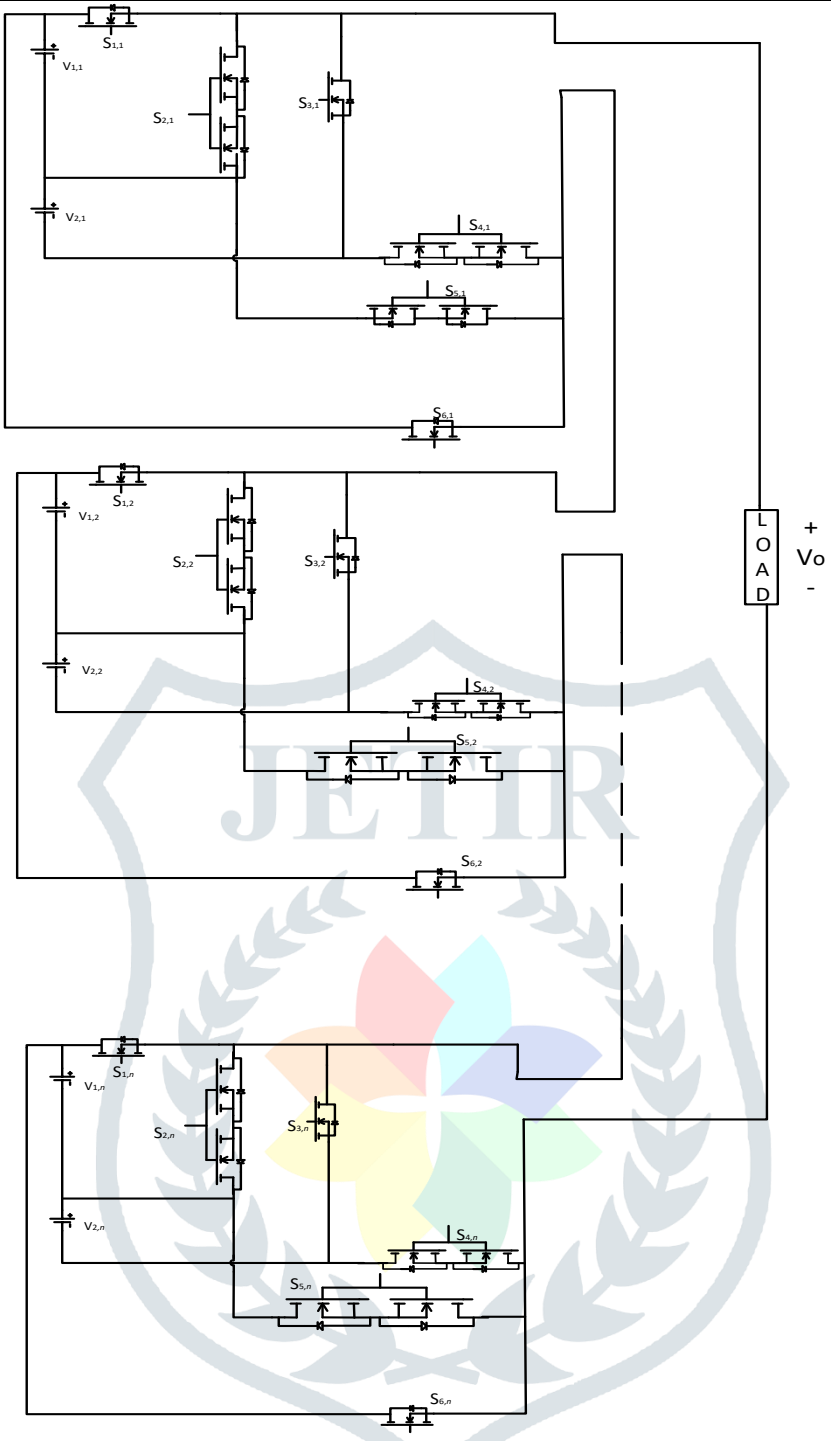

Fig. 2. Cascading of n-basic unit.

III. Modulation technique

Modulation is the process that is used to switch the power electronic device from one state to other. The purpose of the modulation technique is to generate the multilevel output waveform. Each modulation technique generates different switching pulses to achieve the desired output waveform.

Modulation technique 1 - Equa1 Phase (EP) Switching Modu1ation Technique

In this technique the switching angles are distributed average1y 0ver the full comp1ete cyc1e ranging from 0 – 360 degrees. The equation to ca1cu1ate the switching ang1es by Equal Phase (EP) method is given by

$$a_y = y * \frac{180}{N}.$$

Where y= 1, 2, 3, 4……, 2N and N = Number of output vo1tage 1eve1s

Modulation technique 2 - Half height switching modulation technique method

The half height method is employed to reduce the harmonic content at the output voltage side. For M is odd, 2(M - 1) switching angles is determined for the period of 0°- 90° Since the sine wave is symmetrical waveform, the positive half cycle is mirror

symmetrical to its negative half cycle. We define the switching angles in the first quadrant period (i.e., 0°–90°) as main switching angles. Switching angles in second quadrant (90°-180°), third quadrant (180°-270°), fourth quadrant (270°-360°) are to be calculated.

$$\alpha i = \sin^{-1}\left[\left(i - \frac{1}{2}\right) 2/N\text{-}1\right]$$

where $i = 1, 2 \ldots (N-1)/2$

N= level of switching angles

IV. MATLAB Simulink model

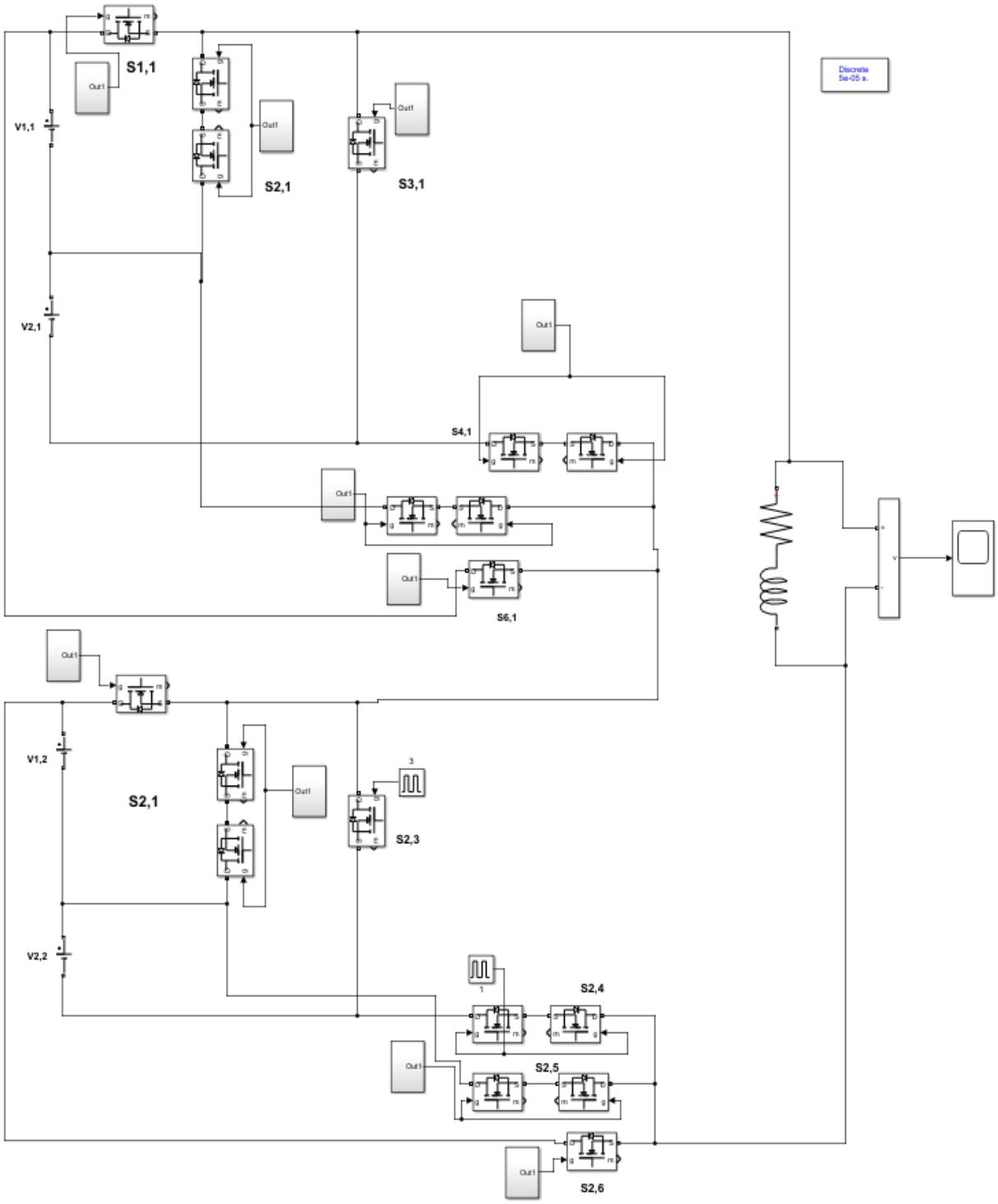

Fig 3: Simulink model of 31 level asymmetric inverter

V. RESULTS AND DISCUSSION

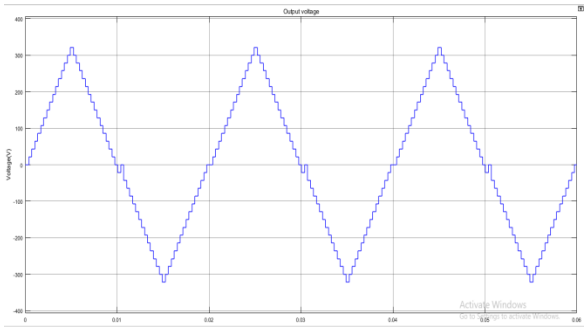

Fig 4. Output voltage waveform for 31 level asymmetric inverter using EPA method -R load

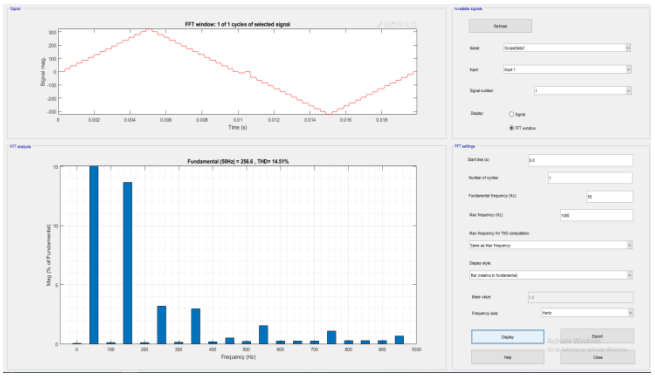

Fig 5 FFT analysis for 31 level asymmetric inverter using EPA method -L load

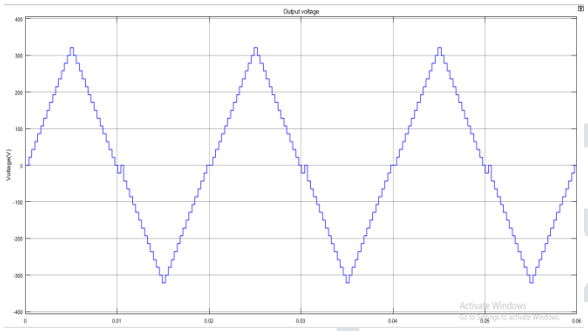

Fig 6 .Output voltage waveform for 31 level asymmetric inverter using EPA method -RL load

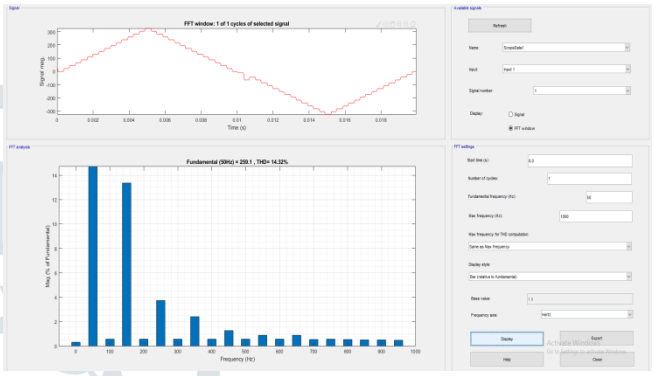

Fig 7 .FFT analysis for 31 level asymmetric inverter using EPA method -RL load

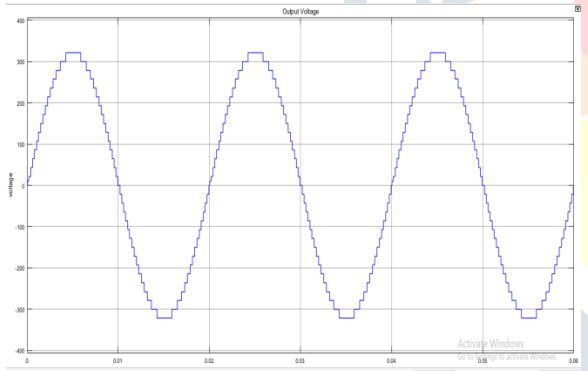

Fig .8 Output voltage waveform for 31 level asymmetric inverter using Half height method -R load

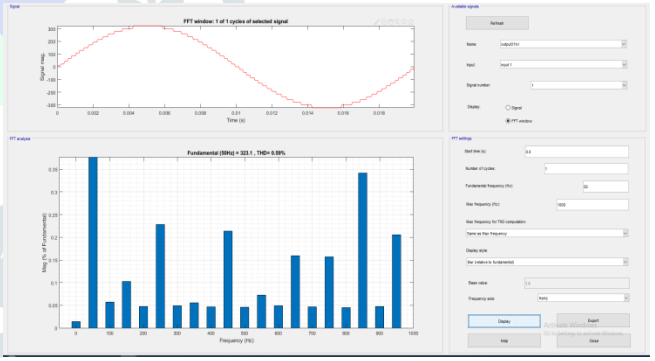

Fig 9 .FFT analysis for 31 level asymmetric inverter using Half height method -RL load

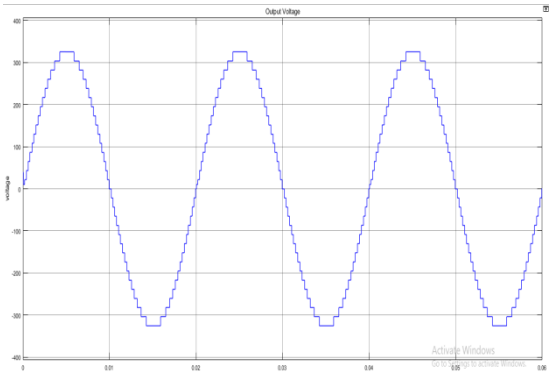

Fig 10. Output voltage waveform for 31 level asymmetric inverter using Half height method -RL load

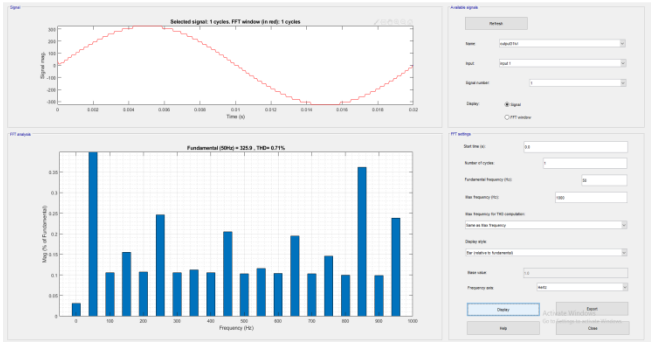

Fig 11. FFT analysis for 31 level asymmetric inverter using Half height method -RL load

Modulation technique	Type of load	THD % voltage
Equal phase angle method	R= 33.85 ohm	14.51
	R= 33.85 ohms L= 2.0523 H	14.32
Half height method	R= 33.85 ohm	0.59
	R= 33.85 ohms L= 2.0523 H	0.71

Table 3: Table of comparison results with half height and equal phase angle modulation technique.

VI. Conclusion

A new cascaded MLI structure has been presented to aid the reduction of switch count and number of sources as compared to conventional structure for a particular level in output voltage. Proposed structure requires less installation area as size has been reduced and easy in controlling the switches. The performance of the proposed structure has been verified by simulated results for 31-level in output voltage.

Equal phase angle modulation and half height modulation technique is applied with the help of pulse generators to this model based on the theory of resultant has been applied for harmonic elimination of the new topology. The switching angles are calculated by carrying out half height method, it has the advantage of finding all existed solutions, where the solution produces the lowest THD is selected. The simulation results show dramatic decrease in the in the output voltage THD. The comparison of THD with different load condition and modulation techniques is shown in Table 3.

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