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# A Low-Power and High-Speed Voltage Level Shifter Based on a Regulated Cross-Coupled Pull-Up Network

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***Abstract :*** This article introduces a voltage level shifter (LS) that is quick and extremely power-efficient. A new regulated cross-coupled (RCC) pull-up network is used to increase switching speed and the Dynamic power usage has been drastically cut. The proposed (LS) can raise nominal supply voltage levels from input signals with voltage levels significantly lower than a MOS device's threshold voltage. Due to its extremely low element count and ultra-low power consumption, the proposed LS is well suited for low-power applications including wireless sensor networks and implanted medical devices. The suggested circuit can convert up input voltage levels as low as, according to the results of the post-layout simulation in a conventional 0.18-m CMOS . The suggested circuit may convert up input voltage levels as low as 80 mV, according to the results of the post-layout simulation in a conventional 0.18-m CMOS technology. the force For an input frequency of 1 MHz and low/high supply voltages of 0.4/1.8 V, the suggested level shifter's dissipation and propagation delay are 123.1 nW and 23.7 ns, respectively.

***IndexTerms*** **- Subthreshold circuit, dual-supply, level shifter, differential cascade voltage switch, low power.**

## I. INTRODUCTION

Supply scaling is used to lower the short circuit current and dynamic power in POWER-efficient digital and mixed-mode circuits and systems. However, lowering the supply voltage decreases the efficiency and speed of analogue circuits. As a result, two or more power supply voltages are used in applications that call for distinct blocks to operate at various speeds [1][ 2]. These kinds of In medium speed systems and applications such wireless sensor networks, tiny medical devices, and environmental monitoring systems, design is more prevalent [3]. Interconnection between sub-blocks in systems using two or more distinct supply voltages. necessitates voltage level shifting of the signals. The voltage level shifters (LS) must be able to raise subthreshold voltage levels and other low logic levels to higher, acceptable voltages.blocks for the following one. Power consumption, propagation latency, and silicon area are the major considerations in the design of LSs because a system may require a significant number of LSs. Therefore, a quick and energy-efficient voltage level shifter that can transform incredibly low input voltage values to nominal supply voltage levels is suggested in this brief. The remaining information is as follows: Section II standard LS circuits, including recent high-performance ones are reviewed. Section III describes how the proposed architecture works. In Section IV, simulation results are presented.

## II. LITERATURE REVIEW

In Fig. 1 depicts two conventional level shifters, the first of which, type I, uses a basic current mirror (CM) as a pull-up network. In this kind of architecture, the interaction between the circuit's left and right branches and pulling-down and-up networks is essentially nonexistent. The result is a slow operation speed. Additionally, it has a sizable standby power, which is mostly caused by a static current that changes its direction depending on the input state and flows via one of the circuit branches. The cross-coupled pull-up network is the foundation of the differential cascode voltage switch (DCVS) architecture, which is depicted in Fig. 1(b), so that the regenerative process amplifies the Q1 and Q2 variation to switch more quickly. Mn1 and Mn2 switch on and off in response to the input rising edge. Mn1 attempts to lower Q1's voltage at this moment. As a result, Mp4 gradually starts to turn on, drawing V2 toward the high supply voltage (VDDH), which aids in turning off Mp3 and speeds up Q1's discharge. Mn1 and Mn2 switch on and off in response to the input rising edge. Mn1 attempts to lower Q1's voltage at this moment. Mp4 therefore gradually starts up. Pulling V2 in the direction of the high supply voltage (VDDH), which aids in turning off MP3, causes Q1 to discharge more quickly. Due to the fact that neither of the two circuit branches require static power, this architecture offers an extremely low standby power. Fig. 2.0 Simplified schematic of the proposed level shifter pull down transistors(MN1,MN2) are unable to easily defeat pull-up transistors when the low supply voltage (VDDL) is lower than the nominal threshold voltage of the process (Mp3, Mp4). The size of the pull-down transistors must therefore be increased in order to boost the pull-down network, which lowers the overall efficiency in terms of power and delay.

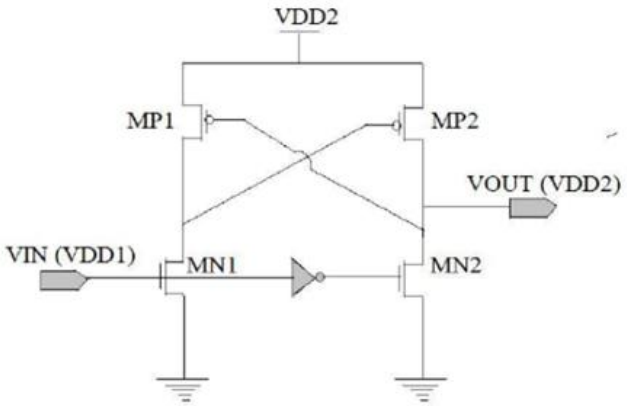


Fig 1.0: Diffrential cacade voltage switch(DCVS) architecture

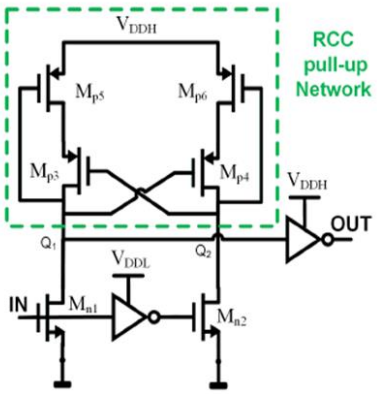


Fig. 2.0 Simplified schematic of the proposed level shifter

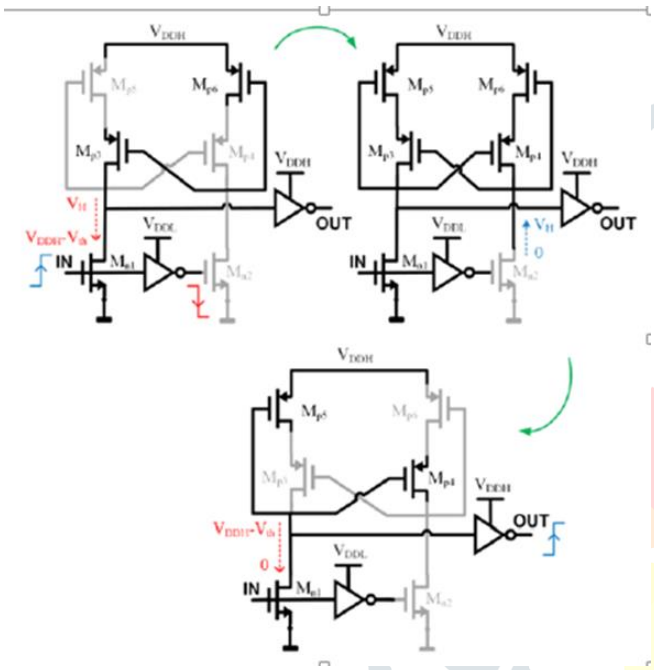

FIG 3.0 Schemetic of Proposed level shifter

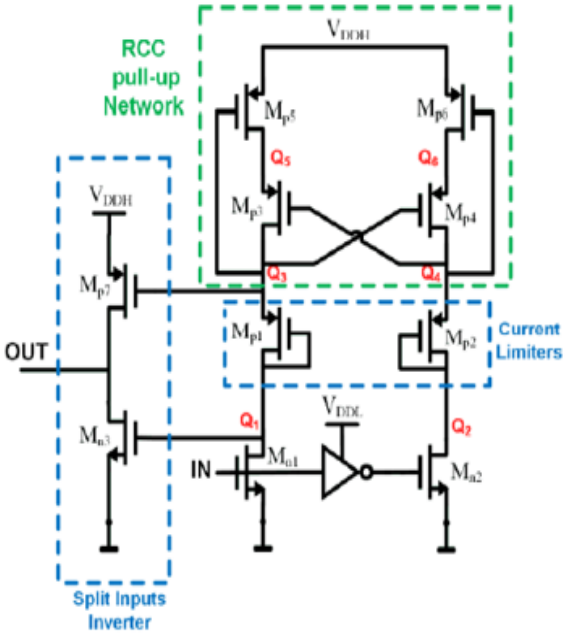


FIG 4.0 Schematic of complete proposed level shifter

## III. PROPOSED METHOD

Here Supply scaling helps power-efficient digital and mixed-mode circuits and systems by lowering the short circuit current and dynamic power of the circuit. Scaling back the supply voltage lowers the efficiency and speed of analog circuits, though. As a result, two or more power supply voltages are used in applications that call for different blocks to be processed at various speeds. More often than not, medium speed systems and applications like wireless sensor networks, tiny medical equipment, and environmental monitoring systems use this kind of design. Interconnection between sub-blocks in systems using two or more distinct supply voltages necessitates voltage level shifting of the signals. For the next block, the voltage level shifters (LS) must be able to raise low logic levels—even voltage levels below the threshold—to higher and acceptable values. Power consumption, propagation latency, and silicon area are the major considerations in the design of LSs because a system may require a significant number of LSs.The schematic of the proposed level shifter is shown in Fig. 2. Our design is a modified DCVS structure, which includes a new regulated cross-coupled (RCC) pair for pull-up part. The proposed technique regulates the strength of the pull-up network and reduces the charge or discharge time of the critical internal nodes, which consequently increases the switching speed and reduces the dynamic power dissipation. For a better understanding of the proposed LS, the operation of the circuit for a low-to-high transition is shown in Fig. 3, in three steps.In the initial state, node Q1 has a high voltage at VH (which is often less than VDDH), whereas Q2 has a low voltage. As a result, MP3 and MP6 are turned on while MP4 and MP5 are not. A low-to-high input transition causes Mn1 to turn on and Mn2 to turn off in the first step. As a result, the Q1 node's parasitic capacitors start to drain, and

because Mp3's pull-up current is fairly low by Mp5, node Q1 quickly discharges. This state lasts until Q1 nearly reaches VDDH& Vth, at which point MP4 and MP5 start to turn on.

As a result, in the second stage, Mp4 turning on causes Q2 voltage to start to rise, turning on Mp3 and Mp6. In the initial state, node Q1 has a high voltage at VH (which is often less than VDDH), whereas Q2 has a low voltage. As a result, MP3 and MP6 are turned on while MP4 and MP5 are not. A low-to-high input transition causes Mn1 to turn on and Mn2 to turn off in the first step. As a result, the Q1 node's parasitic capacitors start to drain, and because Mp3's pull-up current is fairly low by Mp5, node Q1 quickly discharges. This state lasts until Q1 nearly reaches VDDH& Vth, at which point MP4 and MP5 start to turn on. As a result, in the second stage, Mp4 turning on causes Q2 voltage to start to rise, turning on Mp3 and Mp6.When Mp3 shuts off in the third stage, Mn1 will be able to drop node Q1's voltage, even for input voltages below its threshold value. Finally, no static current flows through the left and right branches after turning off MP3 and MP6. This means that the power dissipation and transition

times are greatly decreased as a result of the RCC pull-up component in the suggested LS. Similar to this, the working states of the circuit are switched as the input signal goes from high to low. When Mp3 shuts off in the third stage, Mn1 will be able to drop node Q1's voltage, even for input voltages below its threshold value. Finally, no static current flows through the left and right branches after turning off MP3 and MP6.

This means that the power dissipation and transition times are greatly decreased as a result of the RCC pull-up component in the suggested LS. Similar to this, the working states of the circuit are switched as the input signal goes from high to low. Fig. 3. The planned LS for the L–H transition in use. Two p-MOS diodes are utilised in series with a pull-down network to further reduce power usage. Additionally, a split-inputs inverter is used to lessen short circuit current during output inverter transitions. The low voltage level in nodes Q3 and Q4 is set at a value greater than zero by the pMOS diodes MP1 and MP2. The output inverter's pull-up and pull-down transistors (Mn3 and Mp7) are prevented from going on simultaneously by the voltage difference between Q1 and Q3 nodes, thereby minimizing the short-circuit current and lowering the circuit's power consumption.

## IV. SIMULATION RESULT

The proposed structure Fig. 5 and some earlier work are simulated in a common 0.18-m CMOS technology in order to fairly verify the performance of the proposed LS. All additional structures' schematics and the dimensions of their transistors are displayed. During simulation, the W-Edit waveform viewer shows graphic results. Voltage, current, charge, and power analysis findings from T-Spice can be written to one or more files. In proposed level shifter power consumption reduces from 34uw to 19 uw. Time Delay almost remain same ie 0.44ns to .48ns. The proposed structure contains the fewest components overall. The arrangement of each level shifter is shown in Fig. 8. The area that the proposed design takes up is the smallest design, measuring 63 m2, is made possible by a relatively modest number of transistors. It should be noted that the post-layout simulation used to generate all of the data below used an inverter as the load circuit for every circuit. Each design is simulated under identical circumstances (typical corner, 27°C), with an input frequency of 1 MHz, and a VDDH of 1.8 V. The projected LS displays impressive performance in terms of energy usage When VDDL is in the subthreshold range, the suggested design has one of the lowest propagation delays. Table II summarises the proposed structure's performance and contrasts it with alternative designs. Ps stands for static power in this table, and Pt represents total power. Power delay product (PDP) can be used as a figure of merit for better comparison.

**RESULT**

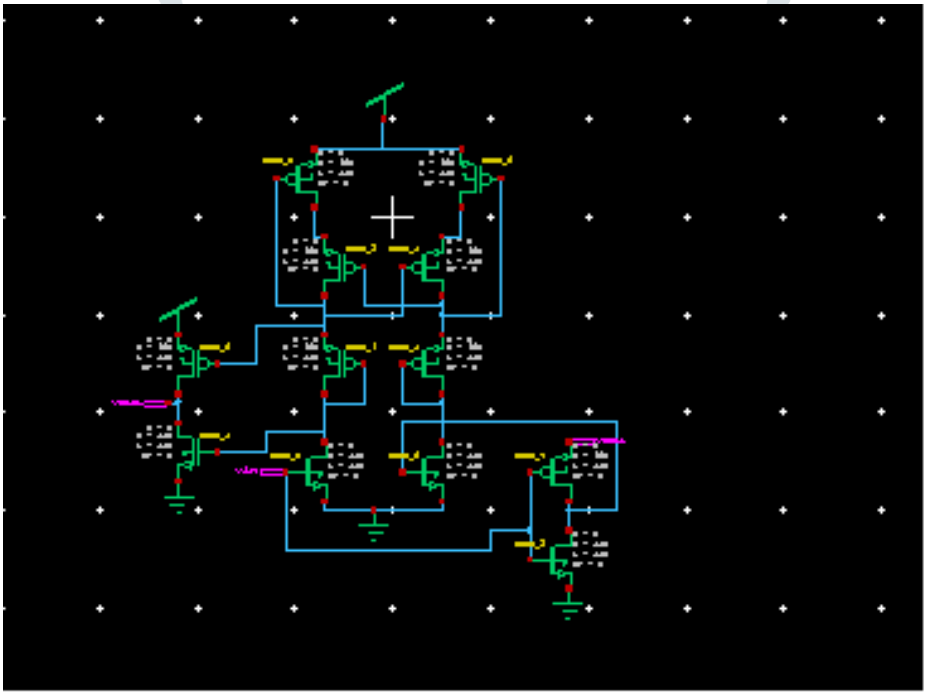

Fig 5.0 PROPOSED LEVEL SHIFTER

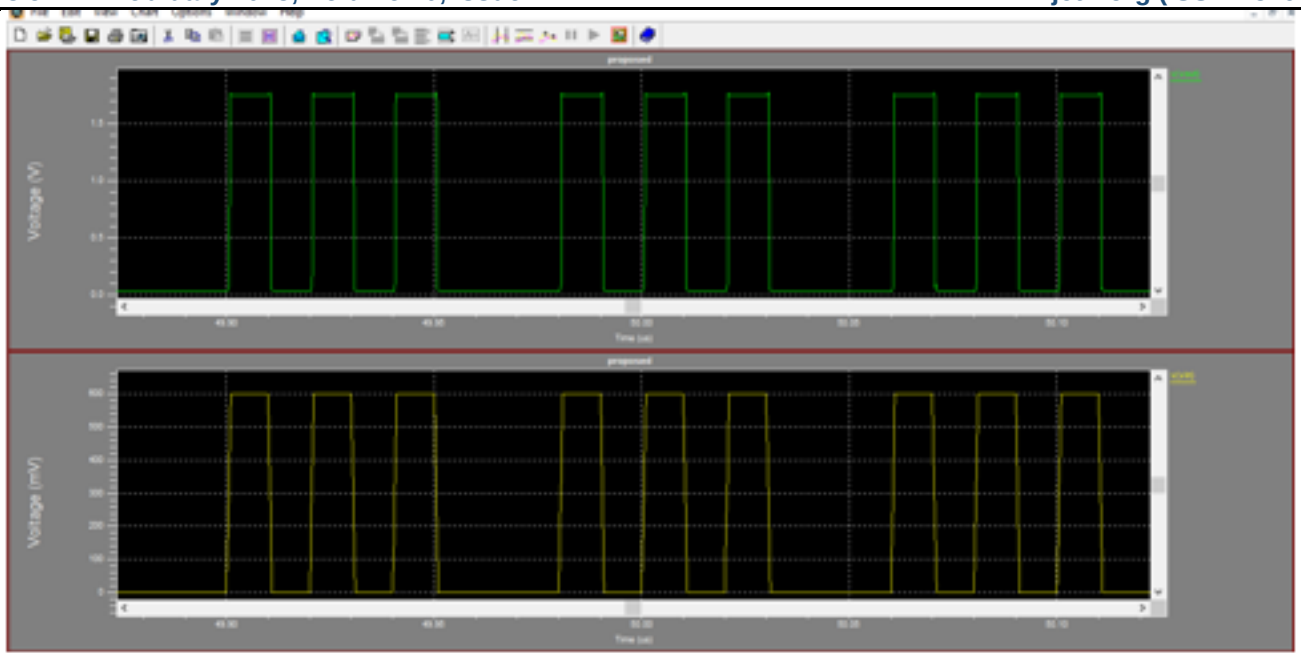

Fig 6.0 SIMULATED OUTPUT OF PROPOSED LEVEL

## Evaluation of power and delay:

| Parameter | Existing level shifter | Proposed Level shifter |
|---|---|---|
| Power (uw) | 34 | 19 |
| Delay (ns) | 0.44 | 0.48 |

Table1.0 evaluation of power and delay

- Power delay product (PDP) can be used as a figure of merit for better comparison.
- The suggested design converts up very low voltage levels while having the lowest PDP and area.

## V. CONCLUSION

In this paper in order to accomplish voltage level shifting from 0.6V to 1.8V, the suggested current mirror and current limiter based high performance voltage level shifter circuit is constructed utilising 45nm CMOS technology. The outcomes demonstrate that the suggested circuit switches smoothly and at a reasonable power cost. The large conversion range enables the suggested design to be as robust as possible.The suggested Voltage Level Shifter may be further enhanced by utilising leakage reduction approaches as leakage power is the primary issue.

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