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DESIGN OF IMPROVED HIGH PERFORMANCE VALENCY LING ADDER

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Abstract: Ling Adder is an advanced architecture of Parallel prefix adders. Parallel Prefix adders are used for efficient. VLSI implementation of binary number additions. Ling architecture offers a faster carry computation stage compared to the conventional parallel prefix adders. Ling adders help to reduce the complexity as well as the delay of the adder further. In many computers and other kinds of processors, adders are used not only in the Arithmetic Logic Unit (ALUs), but also in other parts of the processor. Thus the delay in adders has to be decreased as maximum as possible to make the system faster. In particular, valency or the number of inputs to a single node is explored as a design parameter. High -valency. Ling adders have superior area x delay characteristics over previously reported Ling-based or non-Ling based adders for the same input size. In DSP, even the multipliers require a large number of logic gates that consumes more area, power and delay. Hence ,the lookup table can be used for performing computation which requires less area. Therefore, APC and OMS are the two techniques implemented in Lookup table so as to reduce the size to one-fourth of its conventional multiplier. This proposed combination of both Lookup table Multiplier and Ling adder has better area and delay measurement

Index Terms –

1.INTRODUCTION

An adder is a digital circuit that performs addition of numbers. In many computers and other kinds of processors adders are used in the arithmetic logic units or ALU. They are also utilized in other parts of the processor, where they are used to calculate addresses, table indices, increment and decrement operators, and similar operations.

Arithmetic circuits are the ones which perform arithmetic operations like addition, subtraction, multiplication, division, parity calculation. Most of the time, designing these circuits is the same as designing multiplexers, encoders and decoders. In many computers andother kind of processors, adders are other parts of the processor, many computers and other kinds of processors, where they are used to calculate addresses, table and similar. The binary adder is the one type of element in most digital circuit designs including digital signal processors (DSP) and microprocessor data path units. Therefore fast and accurate operation of digital system depends on the performance of adders. Hence improving the performance ofadder is the main area of research in VLSI system design.

2.1 CONVENTIONAL ADDER

2.1.1 Ripple Carry Adder

Ripple Carry Adder is constructed by cascading full adder blocks in series. A RCA isa logic circuit in which the carry out of one stage fed directly to the carry in of the next stage. It is called RCA because each carry bit gets rippled into the next stage. The main drawback ofthe ripple adder is every bit being added has to propagate through each digital logic gate inthe circuit before an answer can be generated. This is known as a gate delay.

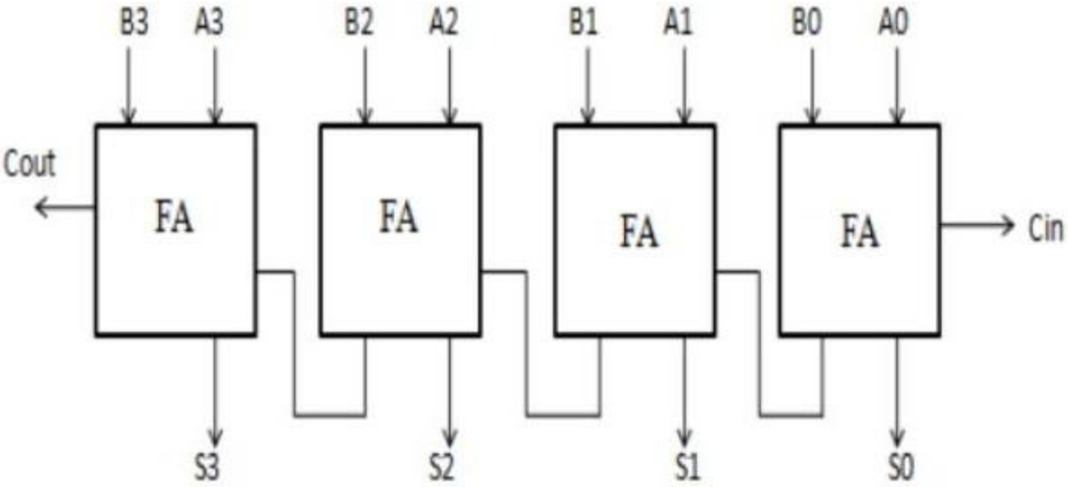

Figure 2.1: 4-bit Ripple Carry Adder

2.1.2 CARRY LOOK AHEAD ADDER

A Carry Look Ahead adder (CLA) is a type of adder used in digital circuits. A carry- look ahead adder improves speed by reducing the amount of time required to determine carry bits. It can be contrasted with the simpler, but usually slower, ripple carry adder for which the carry bit is calculated alongside the sum bit, and each bit must wait until the previous carry has been calculated to begin calculating its own result and carry bits. The carry-look ahead adder calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger value bits. The Kogge-Stone adder and Brent-Kung adder and Ladner Fischer are examples of this type of adder. To reduce the computation time, engineers devised faster ways to add two binary numbers by using carry-look ahead adders

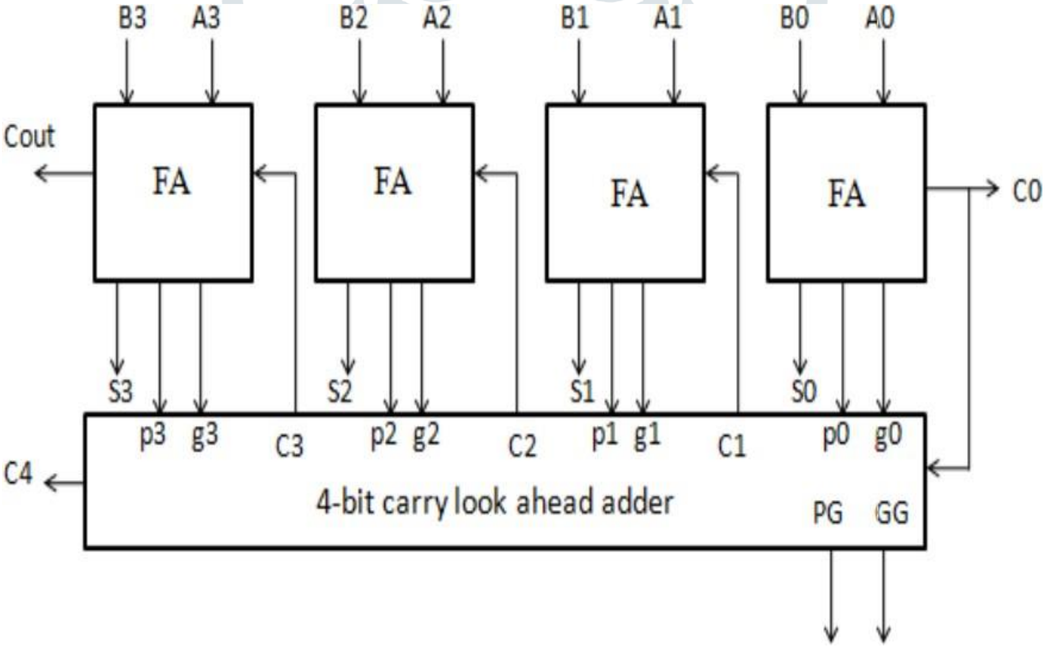

Figure 2.2: 4-bit carry look ahead adder

2.2 Proposed Adders

2.2.1 Parallel prefix adders

The PPA is like a Carry Look Ahead Adder. The production of the carriers the prefix adders can be designed in many different ways based on the different requirements. We use tree structure form to increase the speed of arithmetic operation. Parallel prefix adders are faster adders and these are faster adders and used for high performance arithmetic structuresin industries. The parallel prefix addition is done in 3 steps.

a) Pre-processing stage

b) Carry generation network

c) Post processing stage

a) Pre-processing stage

In this stage we compute, the generate and propagate signals are used to generate carry input of each adder. a and b are inputs. These signals are given by the equation (1) & (2) & (3).

d_i =a xor b .... (1)

p_i =a or b. ....(2)

g_i =a and b ....(3)

The implementation of Pre-processing stage is shown in below figure. Pre- processing stage represents the first basic cell operation of parallel prefix adders.

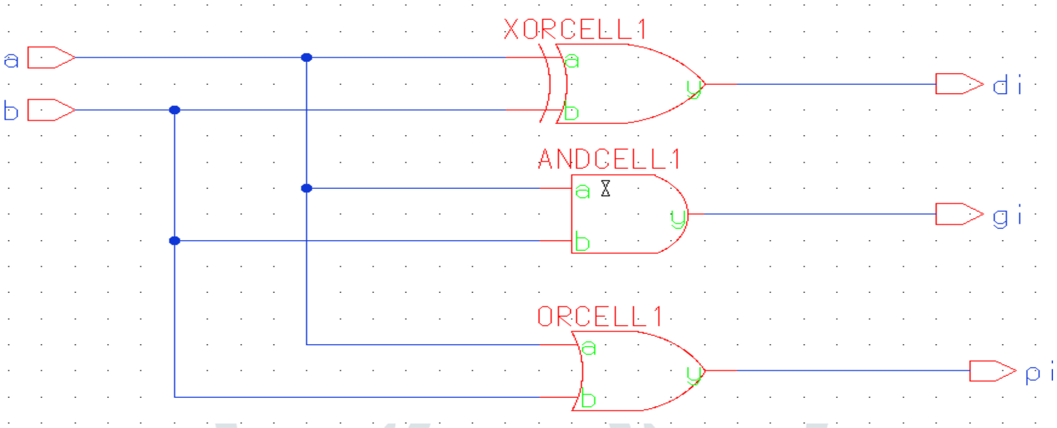

Figure 2.3: Schematic of Basic cell -1

b) Carry generation network

In this stage we compute carries corresponding to each bit. Execution is done in parallel form .After the computation of carries in parallel they are divided into smaller pieces. Carry operator contain two AND gates, one OR gate. It uses propagateand generate as intermediate signals which are given by the equations (4) & (5).

p= p and pprev.. (4)

g= (p and gprev) or g.. (5)

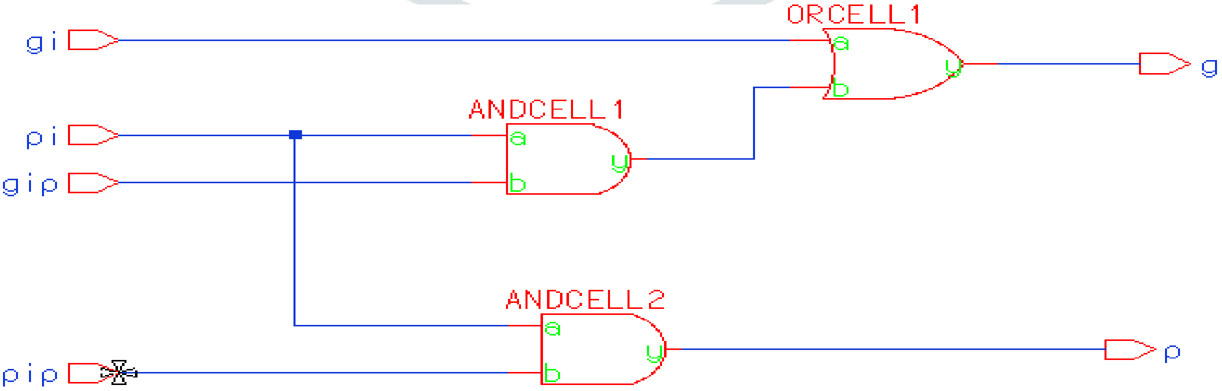

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Figure 2.4: Schematic of Basic cell -2

C) Post processing stage

This is the final stage to compute the summation of input bits it is same for alladders and sum bit equation given

y=d xor pprev ....(6)

$H_{i-1}=C_{i+1} + C_i$...(7)

$S_i= P_i C_i$ .... (8)

$C_{i+1}= (P_i .C_0) + G_i$..(9)

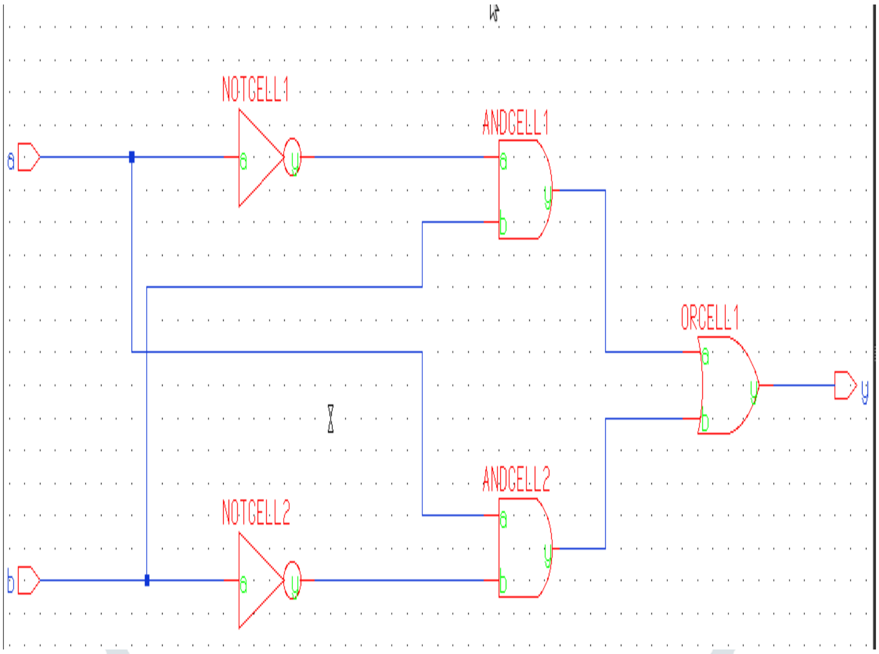


Figure 2.5: Schematic of Basic cell

METHODOLOGY

Parallel Prefix Adders are classified into

1. Kogge- Stone Adder
2. Ladner-Fischer Adder

3.1 : Kogge-Stone Adder

Kogge-Stone adder is a parallel prefix form carry look ahead adder. The Kogge-Stoneadder was developed by peter M. Kogge and Harold S. Stone which they published in 1973. Kogge-Stone prefix adder is a fast adder design. KS adder has best performance in VLSI implementations. Kogge-Stone adder has large area with minimum fan-out. The Kogge- Stone adder is widely known as a parallel prefix adder that performs fast logical addition.

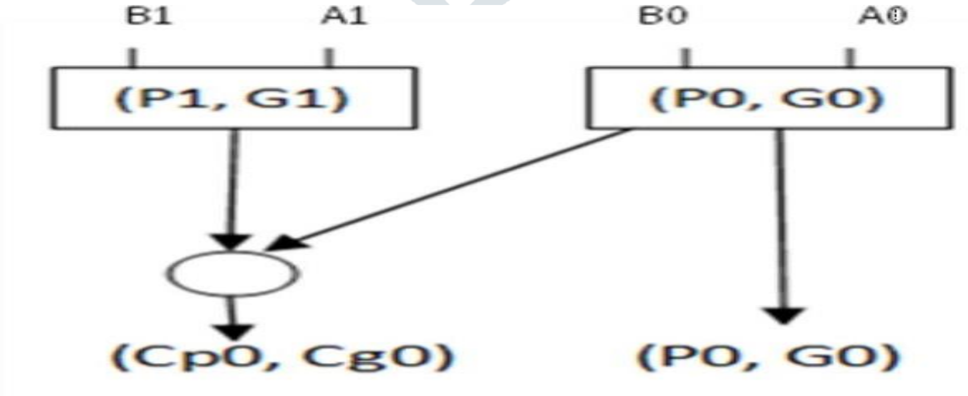


Figure 3.1: 2-bit Kogge-Stone

4-bit Kogge-Stone adder

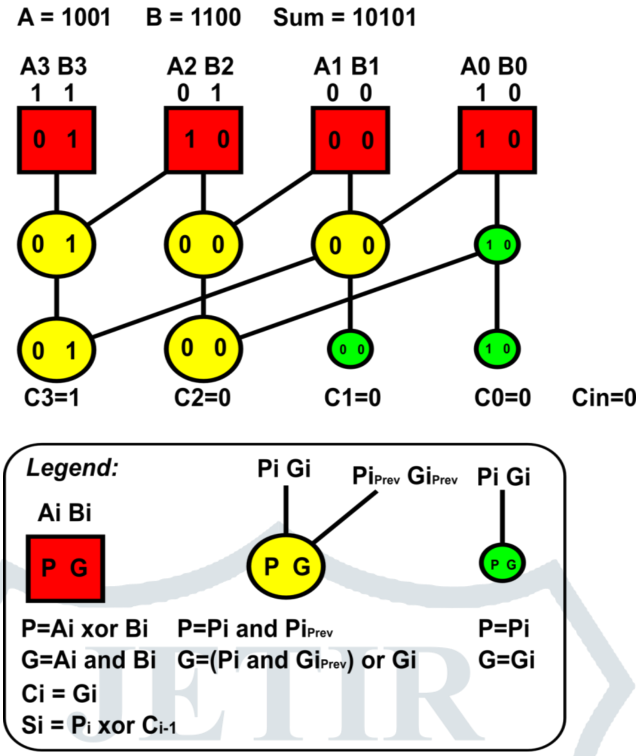


Figure 3.2: 4-bit Kogge-Sto ne Adder

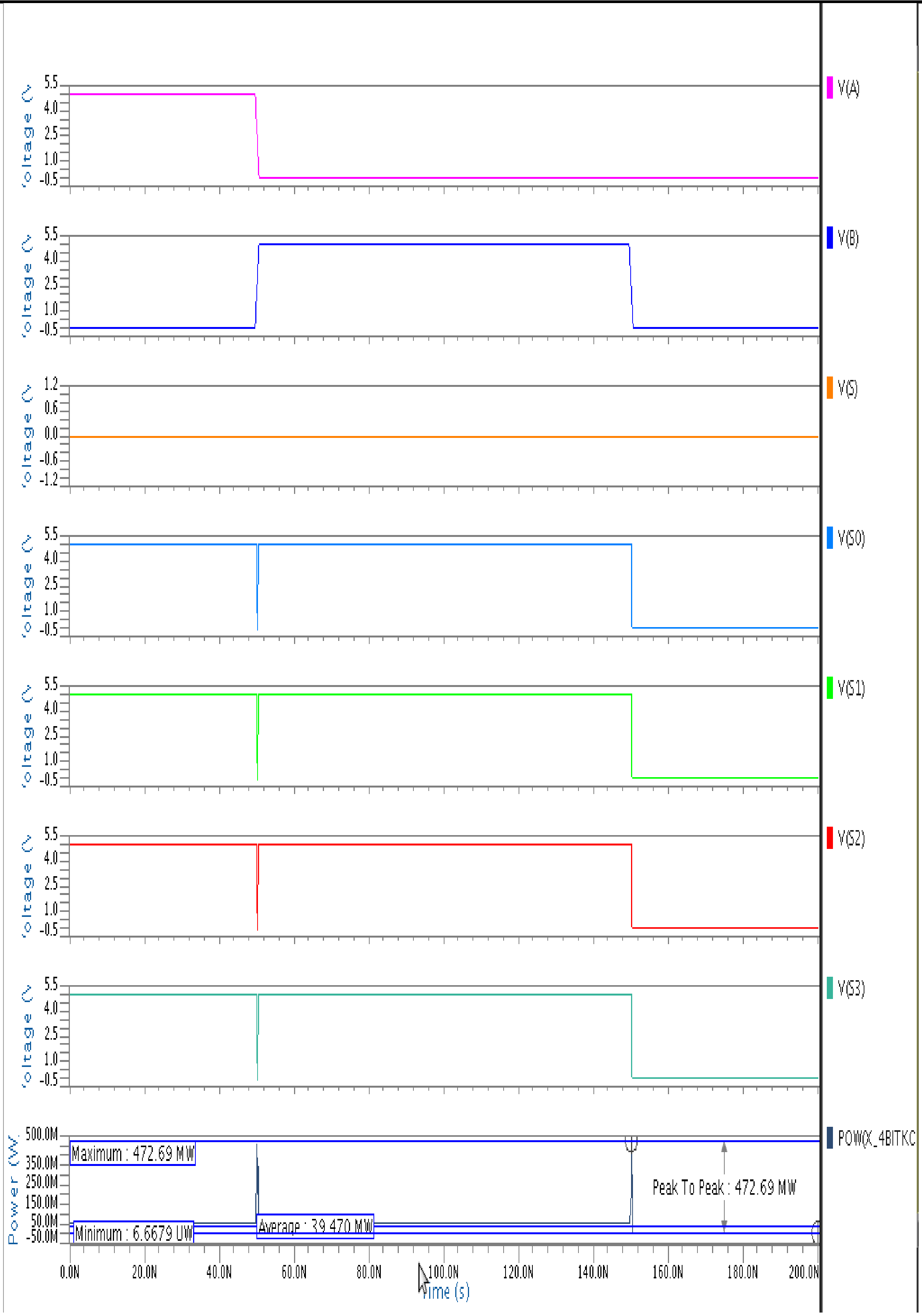


Figure 3.4: Output of 4-bit Kogge-Stone Adder

3.1 Ladner-Fischer adder:

Ladner- Fischer adder is a parallel prefix adder. This was developed by R. Ladner and M. Fischer in 1980.Ladner- Fischer adder has minimum logic depth but it has large fan-out. Ladner- Fischer adder has carry operator nodes.

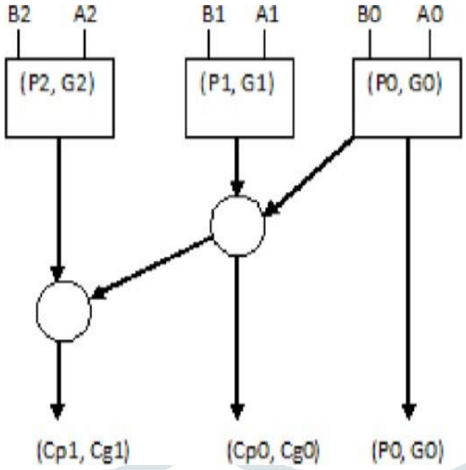
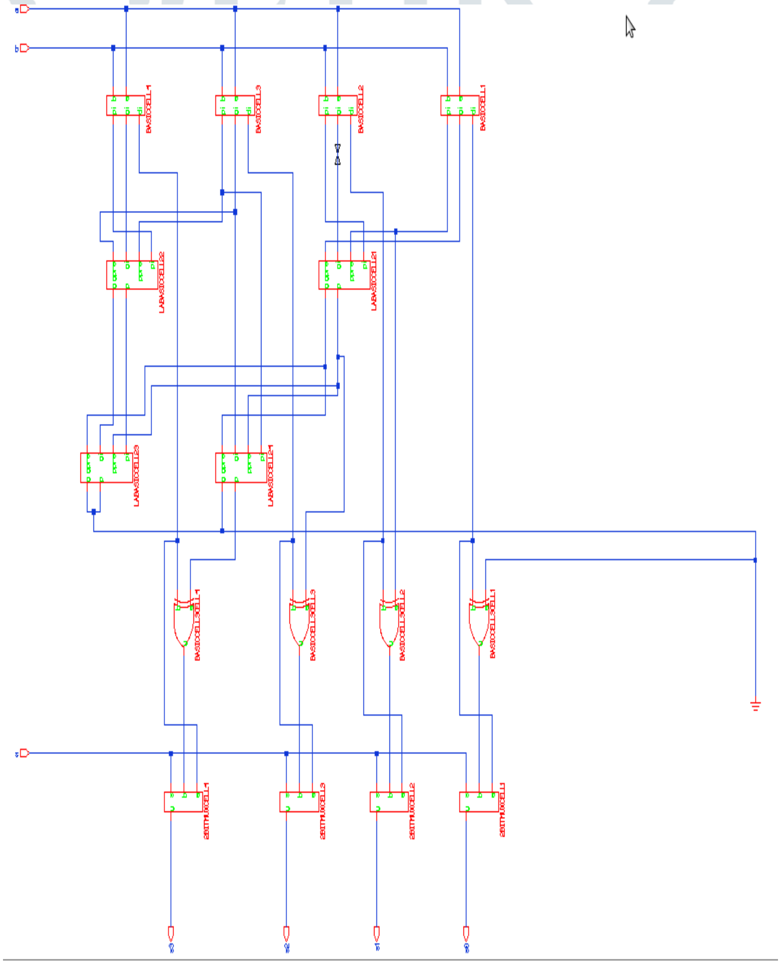


Figure 3.12: 3-bit Ladner-Fischer Adder

3.2.1: 4-bit Ladner-Fischer adder



3.2 : Ling adder design:

In electronics, an adder is a combinatorial or sequential logic element which computes the n-bit sum of two numbers. The family of **Ling adders** is a particularly fast adder and is designed using H. Ling's equations and generally implemented in BiCMOS.

Binary addition is one of the fundamental operations in electronic circuits. Many modern circuit contain several adder units for applications such as arithmetic logic unit; memory addressing and program counter update. Thus, there is a considerable interest to design higher speed and less complex adder architectures. For the last few decades, several adder architectures have been proposed to optimize the adder delay; examples include ripple carry adder, carry-look ahead adder, and parallel prefix adder .The parallel prefix adder is one of the most popular architectures and offers good compromise among area, speed and power. This type of adder implements a logic function to determine whether each bit position generates the carry propagates it or kills it.

Basic Cell:

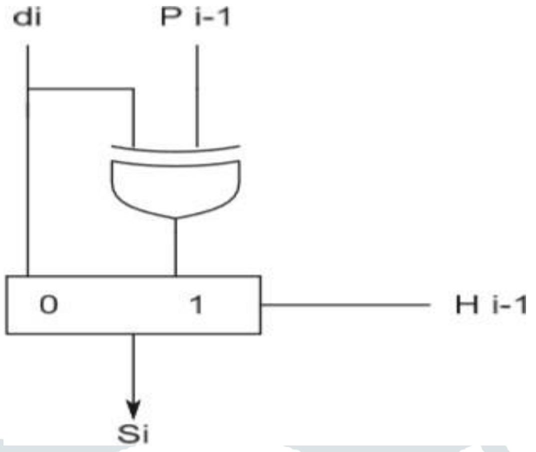
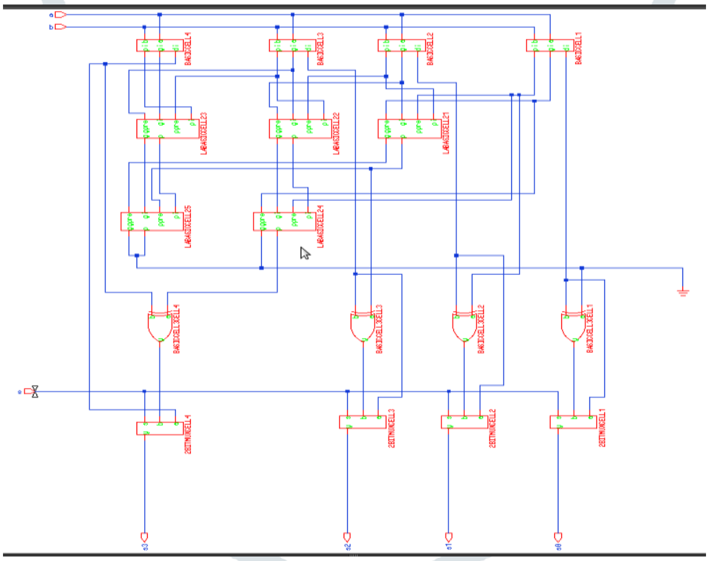


Figure 3.22: Basic cell of Ling adder

3.3.1:4-bit Ling adder:



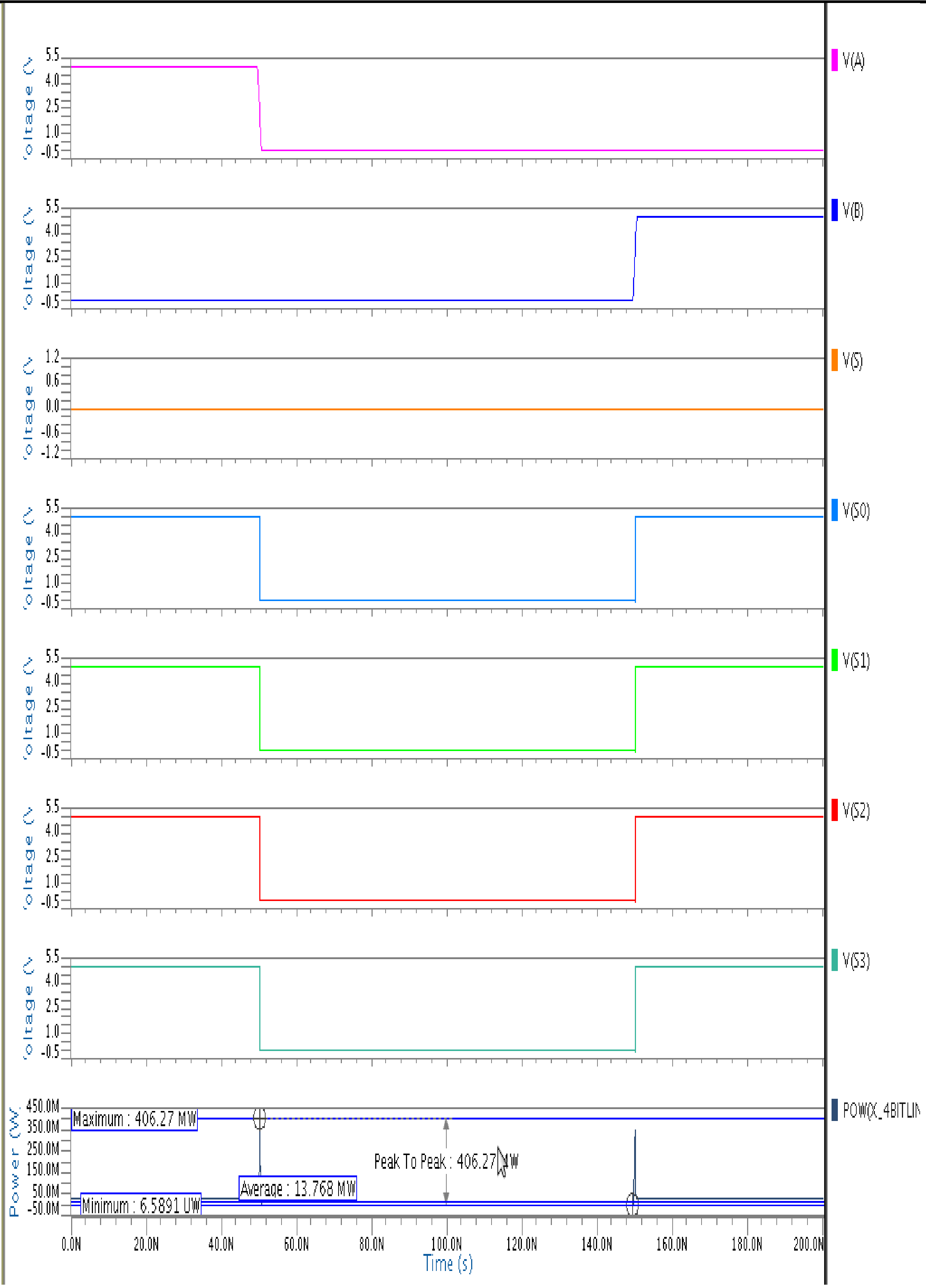
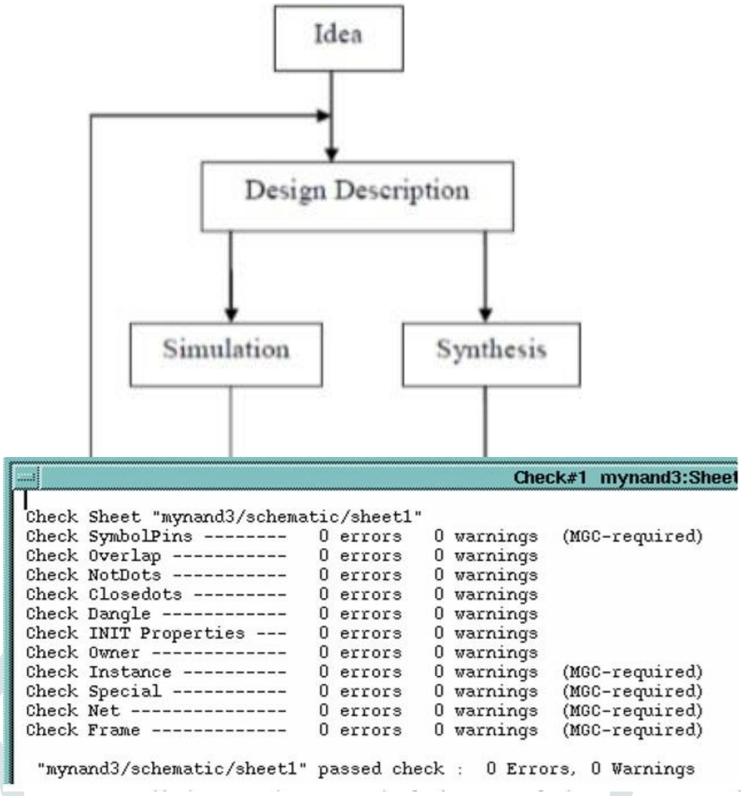


Figure 3.24: Output of 4-bit Ling Adder

IMPLEMENTATION

Design of improved high performance valency Ling adder can be designed and implemented by software means with the help of so many numbers of tools. In this work, the proposed Ling adder can be designed and implemented by Mentor Graphics tool. Thischapter gives the idea about the sequence of various methods to design general VLSI circuit and implementation of proposed architecture with Mentor Graphics tool.

4.1.1 ASIC design flow



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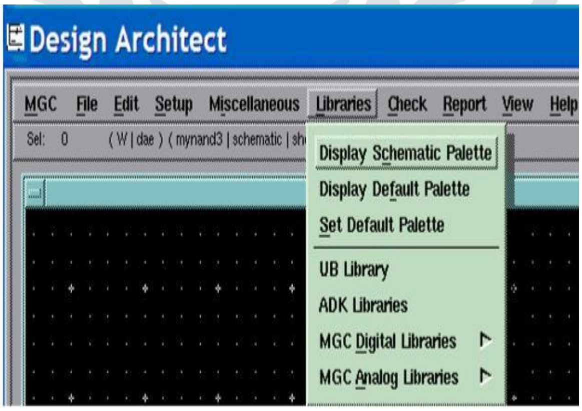
Check Sheet "mynand3/schematic/sheet1"
Check SymbolPins --------   0 errors   0 warnings  (MGC-required)
Check Overlap -----------   0 errors   0 warnings
Check NotDots -----------   0 errors   0 warnings
Check Closedots ---------   0 errors   0 warnings
Check Dangle ------------   0 errors   0 warnings
Check INIT Properties ---   0 errors   0 warnings
Check Owner -------------   0 errors   0 warnings
Check Instance ----------   0 errors   0 warnings  (MGC-required)
Check Special -----------   0 errors   0 warnings  (MGC-required)
Check Net ---------------   0 errors   0 warnings  (MGC-required)
Check Frame -------------   0 errors   0 warnings  (MGC-required)

 "mynand3/schematic/sheet1" passed check :  0 Errors,  0 Warnings
```

Figure 4.1: Major activities in ASIC design

4.1.2 Mentor Graphics tools:

- Design Architect (DA) for schematic design.
- Design Viewpoint Editor (DVE) for creating design viewpoint for your circuit.
- IC Station for layout design. After your layout is finished, you will use DRC check (design to check) whether your layout has any design rule violation.
- Preparing your account first please log into one Sun SPARC station use your UB email ID and password. In the login interface, please click “Options—Session—Common Desktop Environment (CDE)” to select Common Desktop Environment (CDE) session.
- Mentor Graphics Design Architect (DA) tutorial, we are going to use MentorGraphics Design Architect (DA) tool to design a schematic circuit of 2-input NAND gate. Log into a Mentor-capable machine
- Now click on the top left icon of the report window and select “Close” to close the report window. Click on menu “File—save sheet” to save your schematic design, and then click on menu “MGC—Exit” to exit Design Architect.



5.1 RESULTS

In Order to implement 8-bit Ling adder architecture, 8 basicell-1, 17 basic cell-2, 8 basic cell-3, are required. The number of transistors required for the 8-bit Kogge-Stone adder are 798, for Ladner-Fischer adder 760 transistors are required, 756 transistors used for Ling adder design. The time (delay) to perform 8-bit Kogge-Stone adder 99.99ns, for Ladner-Fischer adder 100.00ns, for Ling adder 49.86ns.The power consumed in 8-bit Kogge-Stone adder is 24.014mW, for Ladner-Fischer is 23.174mW, for Ling adder 19.765mW.The comparison of parameters of 8-bit Parallel-prefix adders and Ling adder is shown in thetable 5.1

Table 5.3: Comparison of Parameters of 32-Bit Parallel-prefix adders and Ling adder

S.No	Adder	Area(number of transistors	Delay(ns)	Power(mW)
1.	Kogge-Stone	4546	156.07	165.300
2.	Ladner-Fischer	3950	49.85	51.157
3.	Ling	3188	49.85	31.317

6.1 CONCLUSION

As the no. of bits increases, the delay is increases, to decrease the delay further Ling factorization can be recursively applied to all stages in a carry computation tree of an adder. This makes some other paths more complex, but if the complexity is properly balanced the resulting adder can work faster. 32-bit Ling adders are better in terms of Power, speed and area than the Parallel-prefix adders .In this project, 32-Ling adder is implemented using basic cells of parallel-prefix Adder. For 32-bit, the power consumption, area and delay are reduced by 12.63%, 27.28 % and 18.86%.

6.2 FUTURE SCOPE OF WORK

This approach can be further extended to perform the addition of 64-bit and higher order bits.The power can be further reduced by using reversible logic and by modifying the basic cell structures in Ling ad

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