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DESIGN AND IMPLEMENTATION OF 31-LEVEL ASYMMETRICAL INVERTER WITH MINIMAL COMPONENTS

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Abstract: In this work, a single phase 31-level asymmetrical inverter is presented which consists of fourteen unidirectional switches and four unequal DC sources since asymmetrical configuration is preferred as it provides more number of output voltage levels with minimum number of switches. Main objective of this work is to reduce the THD without increasing the number of switches and levels. The comparative study has been done with earlier topologies to conclude the best one, design of load parameters is explained, Equal phase angle modulation technique and Half height modulation technique are used as control techniques,. the simulation of 31-level asymmetrical inverter circuit has done using MATLAB/Simulink. THD obtained from both the methods are compared.

Index Terms - *multi-level inverter, equal phase angle method, half height modulation technique****,*** *THD.*

I. INTRODUCTION

Now days multilevel inverters are gaining more and more attention due to their high-power operation capability and several benefits like lower harmonics, high power quality, and lower switching losses [1],[2]. These MLIs provide a stepped voltage waveform at its output using various DC sources with a power electronic circuitry comprising different power semiconductor switches [3]. Further, the waveform quality can be improved by the expanding of the level. However, the reliability and efficiency performance of MLI is a challenging task due to the more components in the circuit results in high cost [4]. In general, there exist three structures of MLIs, such as diode clamped or neutral point clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB) [5]. The CHB inverter comprises several single-phase H-bridge topologies and classified into symmetric and asymmetric type based on the DC voltage magnitudes [6]. In the symmetric variety of MLIs, all DC voltage sources magnitude is equal, whereas in case of an asymmetrical type, the magnitudes are not equal. In the conventional CHB type inverter, each unit comprises three output levels, such as positive, negative, and zero voltage levels. The evaluation of CHB type inverter's output is simple as the sum of the output voltages at each unit [7],[8]. CHB type inverters are used in high and medium voltage level, whereas in the case of FC and NPC type inverters, voltage balancing is a complex task in high voltage level [9].

In general, high-power loss occurs in high power applications for high switching frequency [6], [10]– [11]. Several such topologies use more component count, which causes the bulky circuit with high control complexity and produces higher THD with less efficiency. A 31-level asymmetric MLI topology is presented in [12] uses eighteen switches and six DC sources results in more cost and complexity in control. The Switched capacitor multilevel inverter has become a competitive issue due to its self-voltage balance, and their highest voltage stress among the switches in switched capacitor based multilevel inverter[13],Enhanced developed-H-bridge based generalized MLI topology is presented [14],several topologies used more number of bidirectional switches results in more number of IGBTs/MOSFETs,which increases the cost of the inverter[15].

In this paper, a 31-level MLI topology is presented this topology's main benefit is having reduced THD without increasing the output levels. This 31-level asymmetrical inverter topology is well-suited for the high and medium power applications such as FACTS, UPS, active filters and renewable energy sources. This work is organized as follows: Section II describes the asymmetrical inverter topology. Section III elaborates the various results and discussion, and Section V summarizes the work.

II. 31-LEVEL ASYMMERTICAL INVERTER

1. ASYMMERTICAL INVERTER TOPOLOGY

Figure.1 shows the topology of the asymmetrical multilevel inverter which can generate 31-voltage levels. This thirty-one level MLI topology consists of fourteen unidirectional switches S1 to S14 and four asymmetric DC sources V1, V2, and V3 and V4. A module of switches S2, S3, S5, and S6 forms the H Bridge, and the load is connected between Va and Vb points which is shown in Fig.1. The desired 31 level output voltage is obtained by 1:2:4:8 ratio of an asymmetrical configuration of four DC sources hence the magnitude of four DC sources is chosen as V1=1Vdc, V2=2Vdc, V3=4Vdc and V4=8Vdc. Therefore, this asymmetrical inverter can generate 31 output voltage levels.

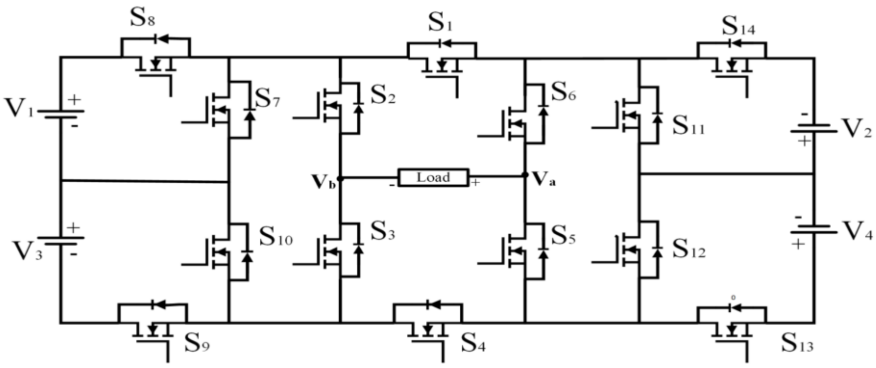

Fig 1. The basic unit of 31-level Asymmetrical Inverter

2. MODES OF OPERATION

This 31-level inverter operates at various operating modes which are explained below. In MODE0: switches S1, S2 and S6 are in conduction stage as shown in figure 2(a) then the resulting output voltage is Vo=0VdcIn MODE1:switches S1, S3, S6, S8, S10 are in conduction stage as shown in figure 2(b),then the resulting output voltage is Vo=+1Vdcl.In MODE2: switches S1,S2 S5 and S12,S14 are in conduction stage as shown in figure 2(c), then the resulting output voltage is Vo=+2Vdc. In MODE3:switches S1,S3,S5,S8, and S10,S12,S14 are in conduction stage as shown in figure 2(d),then the resulting output voltage is Vo=+3Vdc.In MODE4::switches S1,S3,S7 and S9 are in conduction stage as shown in figure 2(d),then the resulting output voltage is Vo=+4Vdc.In MODE5: switches S1,S3 S6 and S8,S9 are in conduction stage as shown in figure 2(e), then the resulting output voltage is Vo=+5Vdc. .In MODE6: switches S1,S3 S5 and S7,S9 and S12,S14 are in conduction stage as shown in figure 2(f), then the resulting output voltage is Vo=+6Vdc.In MODE7: switches S1,S3 S5 and S8,S9,S12,S14 are in conduction stage as shown in figure 2(g),then the resulting output voltage is Vo=+7Vdc.In MODE8: switches S1,S2 S5 and S11,S13 are in conduction stage as shown in figure 2(h), then the resulting output voltage is Vo=+8Vdc.In MODE9: switches S1,S3 S8 and S10,S11,S13 are in conduction stage as shown in figure 2(i),then the resulting output voltage is Vo=+9Vdc.In MODE10:switches S1,S2 S5 and S6,S13,S14 are in conduction stage as shown in figure 2(j), then the resulting output voltage is Vo=+10Vdc.In MODE11: switches S1,S3,S5, S10 and S13,S14 are in conduction stage as shown in figure 2(k), then the resulting output voltage is Vo=+11Vdc.In MODE12: switches S1,S3 S5 and S7,S9 and S11 and S13 are in conduction stage as shown in figure 2(l), then the resulting output voltage is Vo=+12Vdc.In MODE13:switches S1,S3 S5 and S8,S9,S11 and S13 are in conduction stage as shown in figure 2(m), then the resulting output voltage is Vo=+13Vdc.In MODE14: switches S1,S3 S5 and ,S9,S13 and S14 are in conduction stage as shown in figure 2(n), then the resulting output voltage is Vo=+14Vdc.In MODE15: switches S1,S3 S5,S8 and ,S9,S13 and S14 are in conduction stage as shown in figure 2(c), then the resulting output voltage is Vo=+15Vdc.

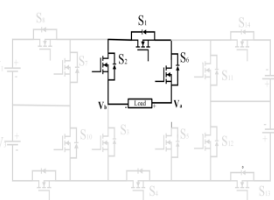

Fig:2(a) mode 0 operation

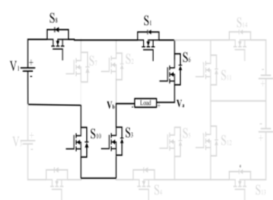

Fig:2(b) mode1 operation

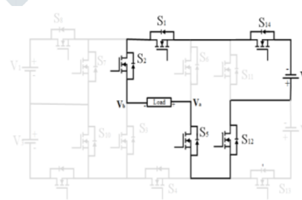

Fig:2(c) mode2 operation

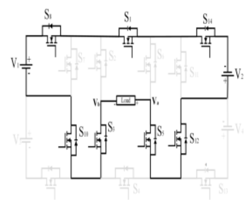

Fig:2(d) mode3 operation

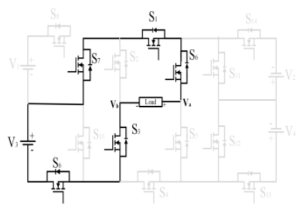

Fig:2(e) mode4 operation

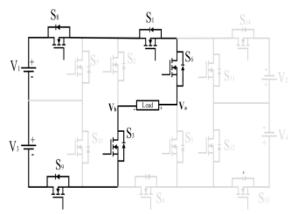

Fig:2(f) mode5 operation

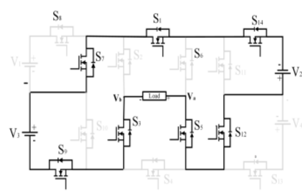

Fig:2(g) mode6 operation

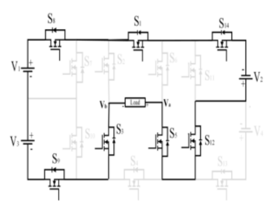

Fig:2(h) mode7 operation

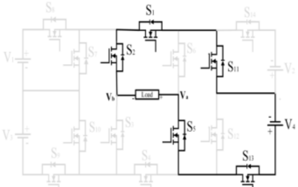
Fig:2(i) mode8 operation

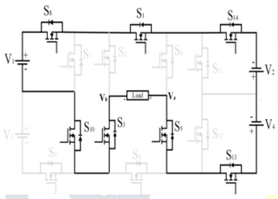
Fig:2(j) mode9 operation

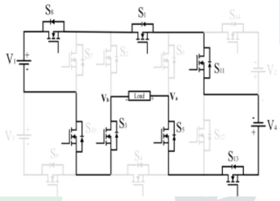
Fig:2(k) mode10 operation

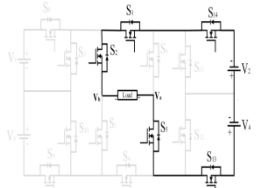
Fig:2(l) mode11 operation

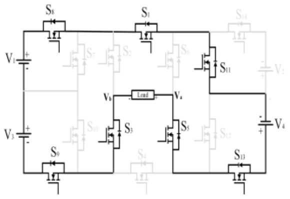
Fig:2(m) mode12 operation

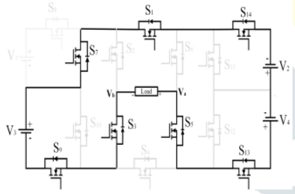
Fig:2(n) mode13 operation

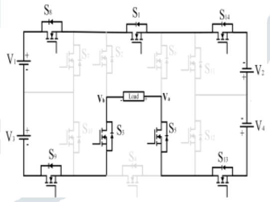
Fig:2(m) mode14 operation

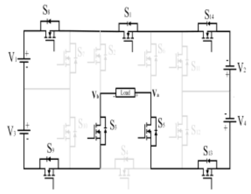
Fig:2(n) mode15 operation

Table 1: Switching table for the 31-level inverter

Voltage level	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	S_{13}	S_{14}
$15V_{dc}$	1	0	1	0	1	0	0	1	1	0	0	0	1	1
$14V_{dc}$	1	0	1	0	1	0	1	0	1	0	0	0	1	1
$13V_{dc}$	1	0	1	0	1	0	0	1	1	0	0	0	1	0
$12V_{dc}$	1	0	1	0	1	0	1	0	1	0	0	0	1	0
$11V_{dc}$	1	0	1	0	1	0	0	1	0	1	0	0	1	1
$10V_{dc}$	1	1	0	0	1	0	0	0	0	0	0	0	1	1
$9\ V_{dc}$	1	0	1	0	1	0	0	1	0	1	1	0	1	0
$8\ V_{dc}$	1	1	0	0	1	0	0	0	0	0	1	1	1	0
$7V_{dc}$	1	0	1	0	1	0	0	1	1	0	0	1	0	1
$6\ V_{dc}$	1	0	1	0	1	0	1	0	1	0	0	0	0	1
$5\ V_{dc}$	1	0	1	0	1	1	0	1	1	0	0	0	0	0
$4\ V_{dc}$	1	0	1	0	0	1	1	0	1	0	0	0	0	0
$3\ V_{dc}$	1	0	1	0	1	0	0	1	0	1	0	1	0	1
$2\ V_{dc}$	1	1	0	0	1	0	0	0	0	0	0	1	0	1
$1\ V_{dc}$	1	0	1	0	0	1	0	1	0	1	0	0	0	0
$0V_{dc}$	1	1	0	0	0	1	0	0	0	0	0	0	0	0
$-1\ V_{dc}$	0	1	0	1	1	0	0	1	0	0	0	0	0	0
$-2\ V_{dc}$	0	0	1	1	0	1	0	0	0	1	0	1	0	1
$-3\ V_{dc}$	0	1	0	1	0	1	0	1	0	0	0	1	0	1
$-4\ V_{dc}$	0	1	0	1	1	0	1	0	1	0	0	0	0	0
$-5\ V_{dc}$	0	1	0	1	1	0	0	1	1	0	0	0	0	0
$-6\ V_{dc}$	0	1	0	1	0	1	1	0	1	0	0	0	0	1
$-7V_{dc}$	0	1	0	1	0	1	0	1	1	0	0	0	0	1
$-8\ V_{dc}$	0	0	1	1	0	1	0	0	0	0	1	0	1	0
$-9\ V_{dc}$	0	1	0	1	0	1	0	1	0	1	1	0	1	0
$-10V_{dc}$	0	0	1	1	0	1	0	0	0	0	0	0	1	1
$-11V_{dc}$	0	1	0	1	0	1	0	1	0	1	0	0	1	1
$-12V_{dc}$	0	1	0	1	0	1	0	0	1	0	0	1	1	0
$-13V_{dc}$	0	1	0	1	0	1	0	1	1	0	1	1	1	0
$-14V_{dc}$	0	1	0	1	0	1	0	0	1	0	1	0	1	1
$-15V_{dc}$	0	1	0	1	0	1	0	1	1	0	0	0	1	1

3. DESIGN OF RL LOAD

RMS Voltage (Vrms) = 230 V, Power = 750 W

I = P/V cos φ = 750/230 * 0.7 = 4.658 A

RMS Current (Irms) = 4.658A

Frequency (f) = 50 Hz

Impedance (Z) = V_{rms} / Irms

Z = 230/4.658 = 49.377Ω

We know that cos φ = R/Z

R = cos φ * Z = 0.7 * 49.377 = 34.5639 Ω

Inductance value is obtained by inductive reactance (XL) which can be calculated as,

$X_L^2 = Z^2 - R^2$ (from the equation $Z^2 = R^2 + X_L^2$)

X_L = 35.262 Ω

But $X_L = L * \omega$

Then, L = X_L/ (2 * π * 50) = 35.262/(2 * π * 50)

L = 112.22m H

4. MODULATION TECHNIQUES

Modulation is the process that used to switch the power electronic device from one state to other. The purpose of the modulation techniques is to generate the multilevel output waveform. Each modulation technique generates different switching pulses to achieve the desired output waveform.

4.1 EQUAL PHASE ANGLE MODULATION TECHNIQUE

In this technique the switching ang1es are distributed average1y over the full complete cyc1e ranging from (0– 360) degrees. The equation to calculate the switching angles by Equal Phase angle (EP) method is given by

Ws = s ∗ (180/ (Q)) where s = 1, 2, 3, 4…, 2Q

Q = Number of output voltage levels.

4.2 HALF HEIGHT MODULATION TECHNIQUE

Half height modulation technique is employed to reduce the harmonic content at the output voltage side. This modulation technique is proposed in this work which gives better total harmonic distortion as compared to equal phase angle modulation technique.

In the Half height modulation technique, the total period (0 – 360 degrees) of the output waveform are divided into four quadrants,

1. The period from 0 to 90 degree is referred as the main switching angle, which is calculated as,

$$a_k = \sin^{-1}\frac{(2k-1)}{(N-1)}$$

Where, k = 1, 2, 3, 4………… $\frac{(N-1)}{2}$ and N = Number of output voltage levels

2. The period from 90 to 180 degree is referred as the second quadrant switching angle which is calculated as,

$$a_{\frac{N+1}{2}} = \pi - a_{\frac{N-1}{2}}, \pi - a_{\frac{N-2}{2}}, \ldots\ldots\ldots, \pi - a_1$$

3. The period from 180 to 270 degree is referred as the third quadrant switching angle which is calculated as,

$$a_N = \pi + a_1, \pi + a_2, \ldots\ldots\ldots, \pi + a_{\frac{N-1}{2}}$$

4. The period from 270 to 360 degree is referred as the final quadrant switching angle, which is calculated as,

$$a_{\frac{3N-1}{2}} = 2\pi - a_{\frac{N-1}{2}}, 2\pi - a_{\frac{N-2}{2}}, \ldots\ldots., 2\pi - a_1$$

4.3 MATLAB Simulink model

In an asymmetrical switching pattern, the input DC voltages are given as V1 = 21.68V, V2 = 43.36V, V3 = 86.72 V, and V4 = 173.44 V. The switches S1 to S14 are Unidirectional MOSFET semiconductor switches.

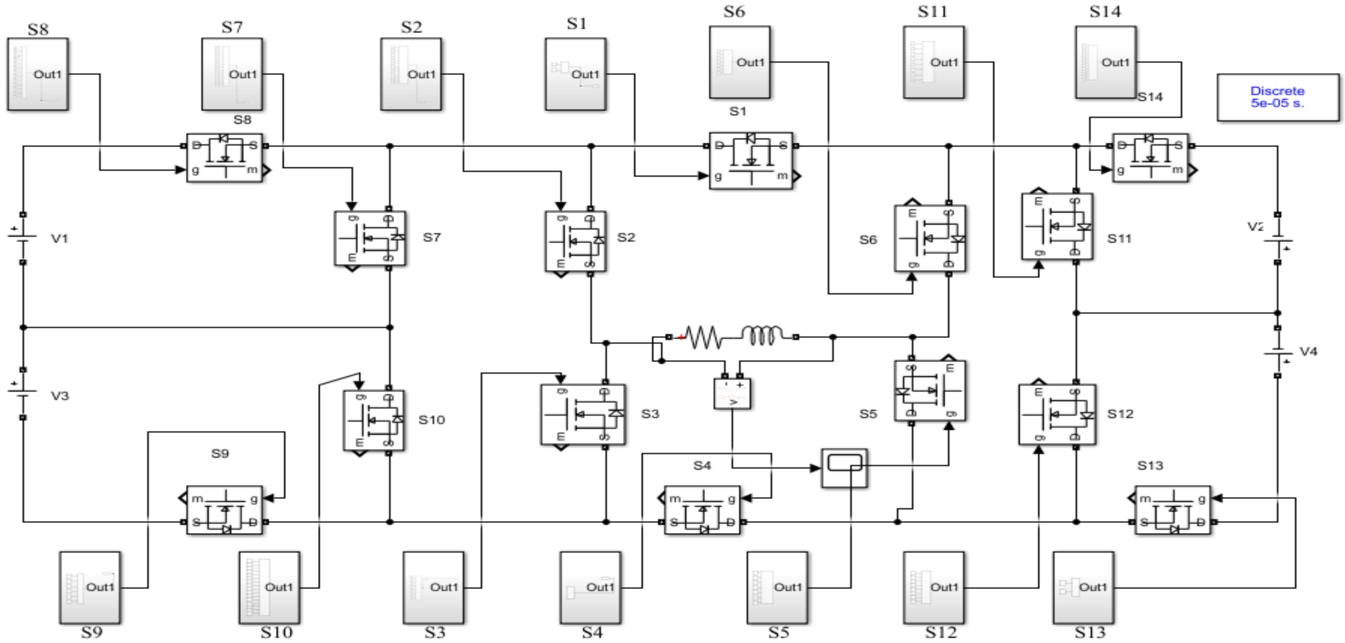

Fig.3 MATLAB/Simulink circuit for 31-level Asymmetrical Multi level inverter

The 31-level asymmetrical multilevel inverter is simulated for the Equal phase angle method and half height modulation technique in the MATLAB/Simulation environment. The results are analyzed for RL load. The detailed analysis of each of the above simulations was done through detailed comparisons; inferences were made on the basis of Total Harmonic Distortion, circuit complexity, voltage stress on devices etc.

In the 31-level MLI, the circuit is built of 14 MOSFET switches. The RL load of R=34.56ohms and L=112.22mH. The asymmetric dc input voltages are used in the ratio of 1:2:4:8. Fig3 represents the simulation circuit of the 31-level asymmetrical inverter.

III RESULTS AND DISCUSSION

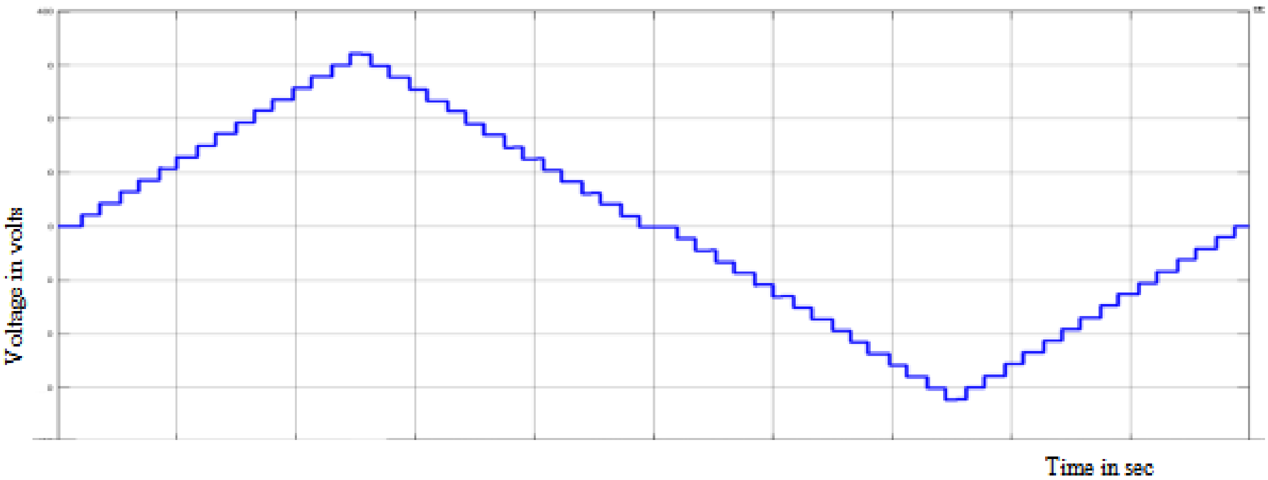

Fig.4. Output voltage waveform of 31-level Asymmetrical inverter using Equal Phase angle method for RL load.

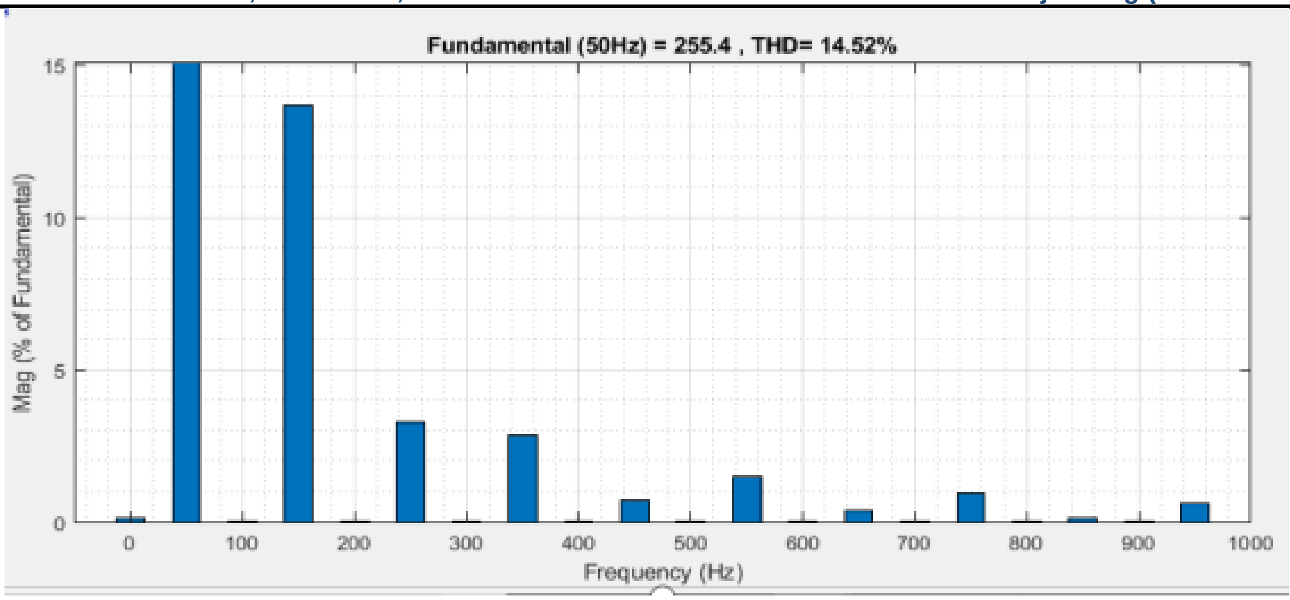

Fig.5 THD spectrum for output voltage using Equal phase angle modulation technique for RL load

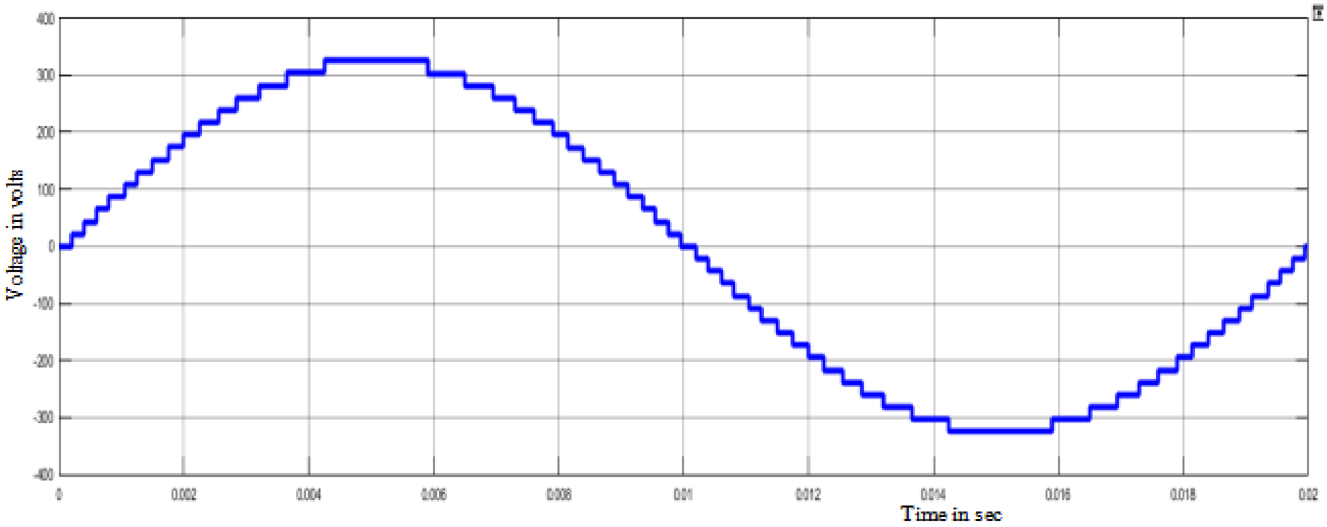

Fig.6 Output voltage waveform of 31-level Asymmetrical inverter using Half height modulation technique for RL load.

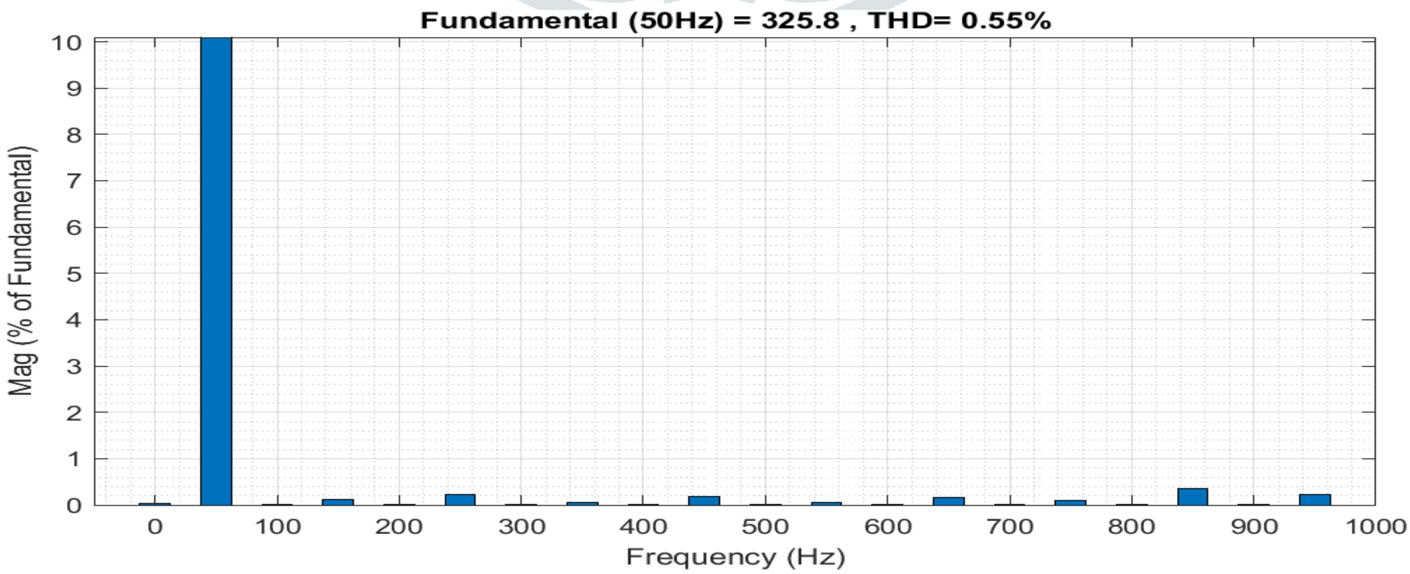

Fig.7 THD spectrum for output voltage using Half height modulation technique for RL load

IV. CONCLUSION

This work mainly concentrates on reducing THD to a very lower value. This 31-level asymmetrical inverter generates 31 levels output waveform. Due to the use of a fewer number of components, the circuit complexity, cost are reduced. This type of inverter circuit produces more output levels in asymmetrical configuration as compared to symmetrical one. The MATLAB simulation is done for equal phase angle modulation technique and half height modulation technique. The comparison is done between equal phase angle modulation technique and half height modulation technique in terms of simulation results with RL loads considering the THD parameter to highlight the best performance of the 31-level asymmetrical inverter. Thus, simulation results show the better performance and superiority of the 31-level asymmetrical inverter circuit over the conventional multilevel inverter topologies. From below Comparison table VI, we can observe that, the total harmonic distortion is 14% by using equal phase angle modulation technique. The THD is reduced from 3.35% which is obtained from staircase modulation technique in the base paper to 0.55% from half height modulation technique which is used in this work. So thereby concluding that THD using half height modulation technique is better and also is in the acceptable value as defined by IEEE standard. The presented MLI is accomplished with reduced THD, and it is superior to earlier topology.

Table 2: Comparison table of results with equal phase angle and half height modulation technique

Modulation technique	Type of load	THD % voltage
Staircase modulation technique	*R-L Load*	3.35%
Equal phase angle modulation technique	*R-L Load*	14.52%
Half height modulation technique	*R-L Load*	0.55%

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