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REDUCTION OF RIPPLE CURRENTS IN A SINGLE-PHASE FUEL-CELL-BASED UNINTERRUPTIBLE POWER SUPPLIES

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Abstract : A well-known issue of fuel-cell-powered single-phase uninterruptible power supplies (UPS) is that the input current from the dc source is coupled with the second-order current ripple due to the ac-side instantaneous power pulsating at twice the line frequency. The low frequency ripple component has been confirmed to have detrimental impacts on fuel cell's reliability and lifespan. To solve this issue, a boost inverter that can work in both differential mode (DM) and common mode (CM) operations is adopted by this paper. The DM operation achieves active power conversion and a well-regulated ac output voltage. Meanwhile, the CM operation ensures effective dc current ripple reduction. In addition to operating with linear loads, the proposed control method extends its working scope to nonlinear loads, where meticulously designed repetitive controllers are employed to handle the multiple low-harmonic situations. Moreover, the proposed control method also introduces an interleaved pulse-width modulation to further reduce the switching frequency ripple in the DC current. The stability of the proposed control system is stringently examined. Finally, presented experimental results validate the theoretical analysis as well as the effectiveness of the proposed method in current ripple reduction**.**

IndexTerms **-** Fuel-cell, uninterruptible power supplies (UPS), differential mode (DM), common mode (CM), frequency ripple, **.**

I. INTRODUCTION

Driven by the increasing demands of sustainable and clean energy, a handful of renewable energy resources have been vigorously investigated. As a significant energy alternative, fuel cells have been widely utilized to support electricity demand by virtue of their high power density, superior energy efficiency and excellent emission control.

Fuel cell powered single-phase uninterruptible power supplies (UPS) are commonly adopted to provide high quality and reliable power for system sensitive loads in case of power failures. However, a well-known issue with such single-phase systems is that the performance of dc side may be affected by the second-order current ripple, which is resulted from the double-line frequency component of ac-side instantaneous power. Notably, this low-order current ripple is proved to have measurable effects on fuel cell's inner chemical reactions, and hence, detrimental to fuel cell's reliability and lifespan. In studying interactions between fuel cells and power converters, [1] examines the fuel cell voltage responses to a series of current sinusoidal perturbations and detected an observable hysteresis at around 100 Hz exclusively. Another paper explores the effects of current ripple on fuel cell's performance [2], the result confirms both the presence of hysteric phenomenon and the proximity of ripple frequency to the fuel cell's cutoff frequency can be factored into additional losses of the output power. Moreover, fuel cell's durability and lifespan can also be crippled as a result of the low-frequency sinusoidal disturbances [3]–[5]. Besides, the low-frequency current ripples are recently found to be a major cause of degradation in the fuel cell's cathode catalyst [6], which is another threat to system performance and reliability. Similar effects are also noticeable in battery-powered systems [7]. Despite already serious concerns induced by second-order current ripple, this issue tends to aggravate when the UPS is exposed to nonlinear loads, where the dc input current is polluted by multiple low-frequency ripple components. Apart from disastrous effects on fuel cells, the existence of these current ripples may cause reduced conversion efficiency, nuisance tripping [8] and distorted output voltage in the UPS system. As a result, UPS would provide unreliable and low-quality power to its loads, disrupting normal operations.

In order to mitigate low-frequency current ripples in the dc side of the single-phase system, a variety of methods have been proposed. Depending on their targeted system segments, they can be broadly classified into hardware and software power decoupling techniques. Hardware power decoupling techniques can be further broken down into PPD and APD. The PPD technique is normally implemented by using energy storage devices to decouple the power oscillation [9]. The most widelyused PPD is to increase the intermediate dc-link capacitor [10].

However, the elevated capacitance may prompt the utilization of E-Cap, giving rise to reduced power density and shortened operation lifetime. In contrast, APD, which leverages an organic combination of auxiliary circuits and film capacitor of much lower capacitance to substitute bulky E-Cap, seems to be a promising alternative. The simplest APD method involves inserting an *LC* circuit to the dc bus [11], making large ECap unnecessary. Nonetheless, this technique introduces inductor as another energy storage, which has lower

energy density and higher ESR compared to film capacitor [12]. Another approach is to install a bidirectional dc–dc converter in parallel with dc bus and make the ripple power solely supplied by this additional converter [13], [14]. However, the extra circuits lead to increased power loss, system complexity and costs. Other shunt film-capacitor based APD techniques are provided in [12], [15]–[17], and they can be generally categorized into dc decoupling and ac decoupling based on the polarity of the decoupling capacitor voltage [9]. However, their common defects from efficiency and system complexity points of view still remain unresolved. Even in the case of [18], where the decoupling circuit shares switches with the full-bridge inverter, making the number of switches remains the same. Yet, the dc voltage requirement for this topology is doubled [8].

II. DUAL-MODE OPERATING MECHANISM

A. Circuit Analysis

As shown in Fig. 1.1, the boost inverter is essentially composed by two identical boost dc–dc converters sharing a common dc source. The upper switches of the two boost converters are connected to form the output of the boost inverter. Vin and iin represent the input voltage and current of the boost inverter, respectively. vo denotes the output voltage of the inverter. Normally, the capacitor voltages vc1 and vc2 are regulated to be

$$v_{c1} = V_{\mathrm{dc}} + \frac{1}{2} V_o \sin(\omega t)$$

$$v_{c2} = V_{\mathrm{dc}} - \frac{1}{2} V_o \sin(\omega t)$$

where Vdc is the dc offset voltage of output capacitors. Vo is the amplitude of output ac voltage, whose fundamental angular frequency is ω. Assuming a resistive load R, the input current iin can be expressed as

$$\begin{aligned} i_{\mathrm{in}} = i_{L1} + i_{L2} &= \frac{1}{1-d_1} i_{S2} + \frac{1}{1-d_2} i_{S4} \\ &= \frac{v_{c1}}{V_{\mathrm{in}}} (i_{c1} + i_o) + \frac{v_{c2}}{V_{\mathrm{in}}} (i_{c2} - i_o) \end{aligned}$$

where iL1 and iL2 are the currents of two inductors with the same inductance L. The two capacitors C1 and C2 are also identical in their capacitance C, the voltages of which are vc1 and vc2 , respectively, whose corresponding currents are ic1 and ic2 . By substituting vc1 , vc2 in (1) and (2) into (3) and making proper transformation, the input current iin can be rewritten as

$$i_{\mathrm{in}} = \frac{V_o i_o}{2V_{\mathrm{in}}} - \frac{V_o i_o}{2V_{\mathrm{in}}} \cos(2\omega t) + \frac{\omega C V_o^2}{4V_{\mathrm{in}}} \sin(2\omega t).$$

The last two terms suggest the existence of an observable scale of second-order current ripple at the input of the boost inverter. By incorporating double-line frequency signals into capacitor's voltage references through the CM dc offset voltage regulation as performed in [24], the second-order current ripple can be theoretically compensated. However, the mathematic solution of the unknown amplitudes involves sophisticated square root and inverse trigonometric calculations as illustrated in [8]. Hence, should the nonlinear loads are supplied by the system, the equation solving process tends to be even more complicated. Moreover, the coefficients obtained through the open-loop control scheme are essentially inaccurate due to the ideal conditions assumed for the two output capacitors. Thus, the effectiveness of current ripple reduction by this approach is hardly satisfactory.

B. Modeling and Operation Mechanism

The most significant feature of the boost inverter identified by this paper is that through proper control, the inverter can essentially work in a dual operation mode. The DM operation aims at delivering power from source to load, realizing active dc–ac power conversion. Meanwhile, under the CM operation, the power flow encircles two boost converters individually, leaving the output load unattended. One of the objectives under this operation is to regulate the dc offset voltage of the two output capacitors, while the other is to force current ripple to be assimilated by the same pair of capacitors. In this way, the fuel-cell source would be theoretically free from the low-frequency current disturbance. Notably, there are two differential equations obtained by Kirchhoff's Voltage Law (KVL) and Kirchhoff's Current Law (KCL) that should always hold true regardless of operations. In fact, the system models of DM and CM operations are later derived from the same equations:

$$L \frac{di_{Lj}}{dt} = V_{\mathrm{in}} - (1-d_j) v_{cj}$$

$$C \frac{dv_{cj}}{dt} = (1-d_j) i_{Lj} + (-1)^j i_o$$

where j can be either 1 or 2 corresponding to the variable footers in the two dc–dc converters. Based on the boost inverter's circuit shown in Fig. 1 and capacitor voltage expressions given in (1) and (2), the output voltage under DM operation can be expressed as the difference of the two output capacitor voltages, while the dc offset voltage under CM operation equals to the sum of the very same two capacitor voltages. Therefore, the system models under two operations can be built respectively based on this observation. To simplify the analysis, all variables involved in DM operation are generally defined as xDM = (x1 − x2)/2, where x could be the voltage, current or duty cycle. The same rule goes to CM operation, wherexCM = (x1 + x2)/2. Taking the DM operation for instance. By replacing xDM into (5) and (6), then applying small-signal analysis and proceeding with ac equations while dismissing second-order ac quantities, the following equations are derived:

$$L\frac{d\hat{i}_{\mathrm{DM}}}{dt}=\frac{D_1\hat{v}_{c1}-D_2\hat{v}_{c2}+\hat{d}_1V_{c1}-\hat{d}_2V_{c2}}{2}-\hat{v}_{\mathrm{DM}}$$

$$C\frac{d\hat{v}_{\mathrm{DM}}}{dt}=\hat{i}_{\mathrm{DM}}-\frac{D_1\hat{i}_{L1}-D_2\hat{i}_{L2}+\hat{d}_1I_{L1}-\hat{d}_2I_{L2}}{2}-\frac{\hat{v}_{\mathrm{DM}}}{R}.$$

The symmetric feature of the two dc–dc converter circuits leads to the equality of dc components of different control variables at the quiescent operating point. Specifically, $Vc1 = Vc2 = Vc$, $IL1 = IL2 = IL$, and $D1 = D2 = D$ are validated under this condition. As a result, the equations above can be simplified

$$L\frac{d\hat{i}_{\mathrm{DM}}}{dt}=(D-1)\,\hat{v}_{\mathrm{DM}}+V_c\hat{d}_{\mathrm{DM}}$$

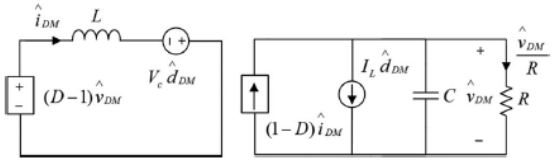


Fig. 1. Small-signal equivalent circuit of DM modeling.

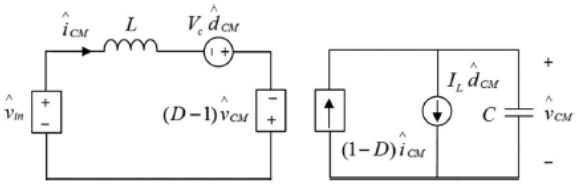


Fig. 2 Small-signal equivalent circuit of CM modeling.

$$C\frac{d\hat{v}_{\mathrm{DM}}}{dt}=(1-D)\,\hat{i}_{\mathrm{DM}}-I_L\hat{d}_{\mathrm{DM}}-\frac{\hat{v}_{\mathrm{DM}}}{R}$$

and their corresponding small-signal equivalent circuit is given in Fig. 5.1. Next, taking the Laplace transform over the above equations and arranging the small-signal model in matrix form, the boost inverter's duty cycle-to-current and current-to-voltage transfer functions under the DM operation can be simply obtained by solving the matrix, which are finally presented as

$$G_{d2i\_\mathrm{DM}}(s)=\frac{\hat{i}_{\mathrm{DM}}(s)}{\hat{d}_{\mathrm{DM}}(s)}=\frac{CV_cs+(1-D)I_L+V_c/R}{LCs^2+L/Rs+(1-D)^2}$$

$$G_{i2v\_\mathrm{DM}}(s)=\frac{\hat{v}_{\mathrm{DM}}(s)}{\hat{i}_{\mathrm{DM}}(s)}=\frac{(1-D)V_c-LI_Ls}{CV_cs+(1-D)I_L+V_c/R}$$

By the same token, the small-signal modeling equations of CM operation can be derived and simplified as

$$L\frac{d\hat{i}_{\mathrm{CM}}}{dt}=\hat{v}_{\mathrm{in}}+V_c\hat{d}_{\mathrm{CM}}+(D-1)\,\hat{v}_{\mathrm{CM}}$$

$$C\frac{d\hat{v}_{\mathrm{CM}}}{dt}=(1-D)\,\hat{i}_{\mathrm{CM}}-I_L\hat{d}_{\mathrm{CM}}$$

whose equivalent circuit is as shown in Fig. 4. Through a series of similar procedures, the equivalent transfer functions under the CM operation can be eventually derived as follows:

$$G_{d2i\_\mathrm{CM}}(s)=\frac{\hat{i}_{\mathrm{CM}}(s)}{\hat{d}_{\mathrm{CM}}(s)}=\frac{CV_cs+(1-D)I_L}{LCs^2+(1-D)^2}$$

$$G_{i2v\_\mathrm{CM}}(s)=\frac{\hat{v}_{\mathrm{CM}}(s)}{\hat{i}_{\mathrm{CM}}(s)}=\frac{(1-D)V_c-LI_Ls}{CV_cs+(1-D)I_L}.$$

Apparently, the equations above show certain resemblance to the small-signal modeling transfer functions of a boost dc–dc converter, except the resistive load is only characterized in DM

III. PROPOSED SYSTEM CONTROLLER DESIGN

Instead of controlling each operation mode through separate loops, this paper proposes a comprehensive control scheme composed by three sub-control block diagrams as shown in Fig. 5.3 Clearly, DM-oriented control scheme is designed to ensure a harmonic free ac output voltage regardless of the types of load it supplies. The CM-oriented control scheme aims at dc offset voltage regulation and input current ripple reduction. In order to present readers an elaborative view over the rationales behind the control schemes design, three sub-control block diagrams will be temporarily disassembled in the following analysis.

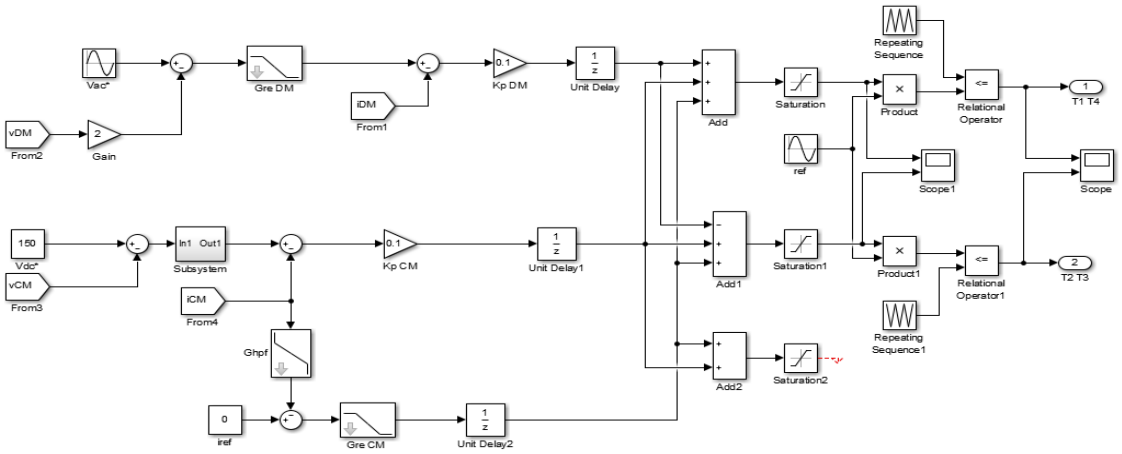


Fig. 3 Overall control block diagram for the boost inverter.

A. DM Control Scheme Design

The classic dual-loop control structure is employed for the boost inverter under DM operation, the implementation of which is presented in Fig. 5.4 Notably, in order to maximally approximate the control model to the real system, all functions are presented in their z-domain forms. For the inner current regulation loop, z-1corresponds to the one-sampled computation delay in the digital control system, while a half-sampled PWM delay derived through zero order hold method is included during continuous-discreet conversion. Furthermore, a proportional gain *Kp* DM is introduced to neutralize the *LC* resonance. *Gd*2*i* DM(*s*) and *Gi*2*v* DM(*s*) represent plant models, whose transfer functions are respectively given in (11) and (12). As for the outer voltage regulation loop, a PR controller is normally adopted to mitigate the harmonics of interest,when only linear loads are concerned. However, in the case that the nonlinear loads are also supplied by the UPS, the ac output voltage may be severely distorted by the imposition of the low frequency odd-order harmonics, e.g., third, fifth, seventh, etc., leading to system malfunction. Under such scenario, multiple

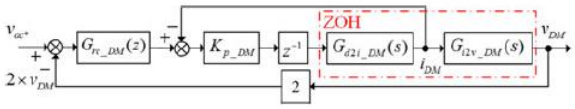


Fig. 4 Closed-loop control for ac voltage regulation (DM operation).

Hence, both mathematic deduction and experimental results in [24] have revealed that the successful suppression of harmonic at one specific order may give rise to the harmonic in the next periodical order, i.e., second order and fourth order in [24].

Therefore, it is extremely difficult to predict the exact number resonant controllers that are adequate to combat the constantly newborn harmonics. In light of the PR controller's ineffectiveness to deal with multiple low-frequency harmonic situation, a modified plug-in repetitive controller is introduced in this paper as Grc DM(z), and its control block diagram is given in Fig. 5.4.

The negative feedback repetitive controller in Fig. 5.4 provides high gains at odd-order harmonic frequencies, which can theoretically suppress all odd-order harmonics below the Nyquist frequency. N denotes the number of delayed samplings, which equals the sampling frequency fs divided by the fundamental frequency fn . Since only odd-order harmonic frequencies are concerned in DM operation, N/2 delays are adequate in this design [28]. Thanks to this particular character, tracking errors may converge to zero in a half fundamental cycle basis, showing a superior dynamic response to that of a conventional plug-in repetitive controller. In addition, Kr1 is the repetitive control gain and is selected properly to achieve plausible damping effect and fast transient response [29]. Q(z) is a zero-phase-shift low-pass filter featured in a unity gain at low frequencies, whose equation is given in (17). The inclusion of such low-pass filter ensures graduate magnitude response attenuation as frequency increases, which strengthens the stability margin of the system.

To further enhance the system stability, a carefully designed phase lead term zm1 is embedded in the forward path to compensate the phase delay caused by the feedback control system, digital computation, and PWM process [29]. Guided by the design procedures prescribed in [29], m1 = 5 is found to have an excellent compensation effect for the DM voltage regulation loop, which is also verified by the system's Nyquist locus in MATLAB as elaborated in the next section. Finally, the transfer function of the modified repetitive controller is given in (18)

$$Q(z) = \frac{z + 2 + z^{-1}}{4}$$

$$G_{\mathrm{rc\_DM}}(z) = K_{r1}\frac{Q(z)\,z^{-\frac{N}{2}+m_1}}{1 + Q(z)\,z^{-\frac{N}{2}}}.$$

B. CM Control Scheme Design

Different from the implementation of DM operation control scheme, the Control design incorporates two correlated control block diagrams as shown in Figs. 5.5 and 5.6, primarily because two functions are fulfilled by the operation. One of the functions is to regulate the dc offset voltages of the output capacitors in order to guarantee that the boost converters are working well within the linear modulation range.

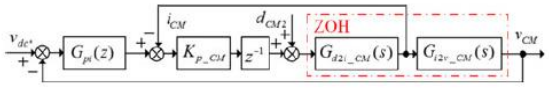


Fig. 5 Closed-loop control for dc offset voltage regulation (CM operation).

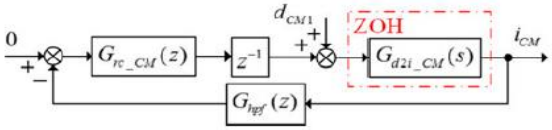


Fig. 6 Closed-loop control for dc current ripple reduction (CM operation).

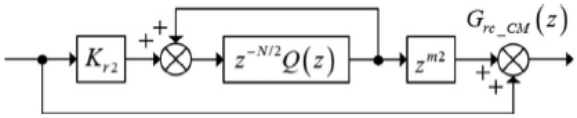


Fig. 7 Plug-in repetitive controller for even-order harmonics reduction.

For the dc offset voltage regulation control block diagram as shown in Fig. 5.5, the inner current loop configuration is nearly the same as its DM current regulation counterpart due to the resemblance of their plant models. Notably, a dCM2 which denotes the duty cycle output by control III in Fig. 5 is added before a full dCM signal is assembled and sent to the next block. The outer voltage loop is well attended by simply using a proportional-integral controller Gpi(z) since only the dc component is concerned. Gd2i CM(s) and Gi2v CM(s) are plant models, whose transfer functions are in given in (15) and (16).

The other function of the CM control scheme can be explicitly reflected from the control block diagram presented in Fig. 9. By properly regulating the CM voltages in the two output capacitors, the predominant second-order component in dc input current can be significantly canceled out in theory, based on the analysis concluded in the last section. However, should the nonlinear loads be put into discussion, the low-order odd harmonics would infiltrate into the ac output voltage and later interact with the fundamental component of the modulation signal, giving rise to the low-order even harmonics in the dc input current, e.g., second, fourth, sixth, etc.

In dealing with the similar multiharmonic circumstance as described in DM output voltage regulation, another derivative of the conventional plug-in repetitive controller is adopted in this part of CMcontrol scheme design as *G*rc CM(*z*). By simply switching the minus sign in the feedback loop into an add sign, the controller in Fig. 7 is reconfigured into a positive feedback repetitive controller dedicated to eliminating all harmonics in the even-order frequencies [30]–[32]. The new controller schematic is given in Fig. 10, where almost all fundamental parameters including *Kr*2 , *N* and *Q*(*z*) share the same values with its negative feedback counterpart used for the DM output voltage regulation.

The only modified parameter is *zm*2 , where *m*2 = 3 is adopted for the better delay compensation effect. Notably, a high-pass filter Ghpf(z) is incorporated in the feedback loop of the closed-loop control block diagram as shown in Fig. 9. This is because the implementation of the modified plug-in repetitive controller may introduce an integral term at 0 Hz frequency in addition to the high gains imposed at even order harmonic frequencies. However, the extra integral term attempts to regulate the mean value of dc input current in a way that may ultimately hamper the DMvoltage regulation. Considering the clear conflict of operations, a first-order low-pass filter is employed to exclusively compensate the high gain brought by the integral term. Finally, the transfer function of the modified repetitive controller in Fig. 10 is written as

$$G_{\mathrm{rc\_CM}}(z) = K_{r2}\frac{Q(z)\,z^{-\frac{N}{2}+m_2}}{1-Q(z)\,z^{-\frac{N}{2}}}. \qquad (19)$$

C. Interleaved Modulation Design

Despite low-frequency harmonics can be dramatically attenuated with the adoption of the modified plug-in repetitive controllers, certain PWM harmonics whose sidebands are centered around the switching frequency and its multiples are non-negligible. The utilization of an *LCL* filter or its more sophisticated ramifications could theoretically suppress these current ripples caused by PWM [33]. However, the introduction of extra electrical components should be strictly obviated unless absolutely necessary. Fortunately, in the case of the boost inverter, the symmetrical circuit structure formed by two identical boost converters enables switching frequency ripple cancellation without incurring additional components. In order to achieve good switching frequency ripple mitigation effect, this paper proposes an interleaved modulation for the boost inverter. In adopting such modulation in system control design, the PWM carriers of the two boost converters are shifted in 180°, which ultimately leads to the opposite changing directions of the two inductor currents *iL*1 and *iL*2 during certain switching periods. Since the dc input current *i*in is the sum of the two inductor currents, an increasing *iL*1 is neutralized by a decreasing *iL*2 and vice versa under the interleaved modulation, which can partially cancel out the switching frequency ripples in the dc input current as shown in Fig. 5.8. Ideally, if the two inductor currents have the same peak-topeak amplitude, the effectiveness of such ripple cancellation is then largely hinged on the values of their respective duty cycles.

Theoretical analysis in [8] suggests the best cancellation occurs at which duty cycles are tuned to be 0.5 for both iL1 and iL2, where nearly all ripple components at switching frequency in *i*in are balanced out. However, the peak-to-peak amplitudes of the inductor

currents in Fig. 1 are constantly changing with the line frequency. Meanwhile, the values of duty cycles are regularly shifting due to the closed-loop control. Therefore, only partial cancellation is de facto achieved in the boost inverter in Fig. 1 under the control scheme design proposed in this paper.

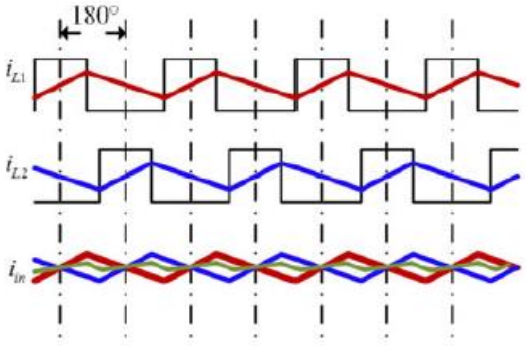


Fig. 8 Interleaved modulation for switching frequency ripple reduction.

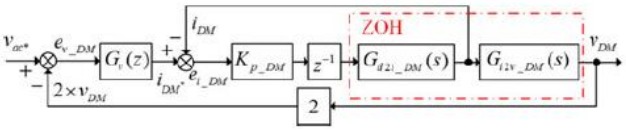
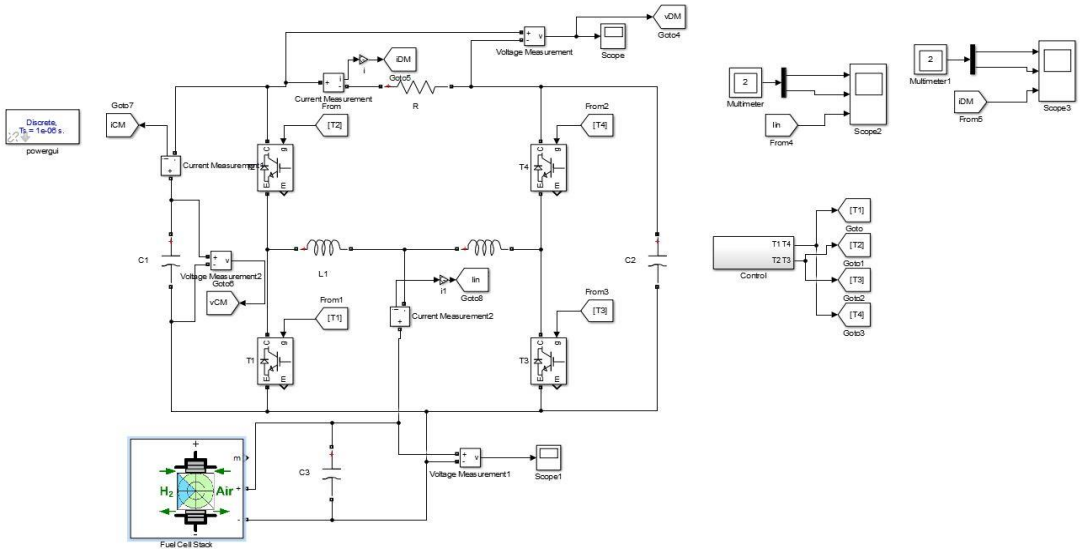


Fig. 9 Alternative control block diagram for ac voltage regulation.

IV. SIMULATION RESULTS

A) RESULTS



B)

Fig 10 MATLAB/SIMULINK diagram of fuel-cell-powered single-phase UPS.

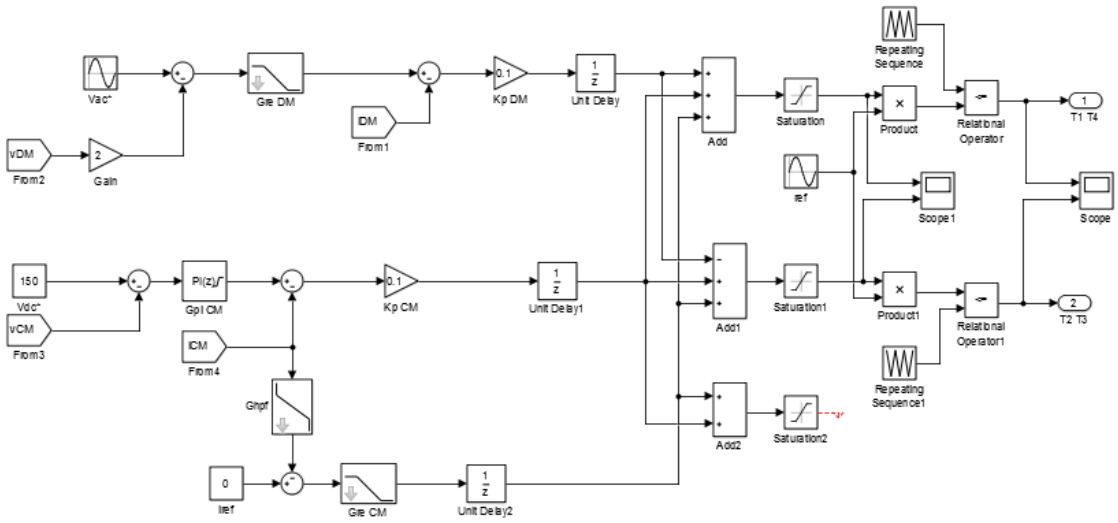


Fig 11 Controller subsytem

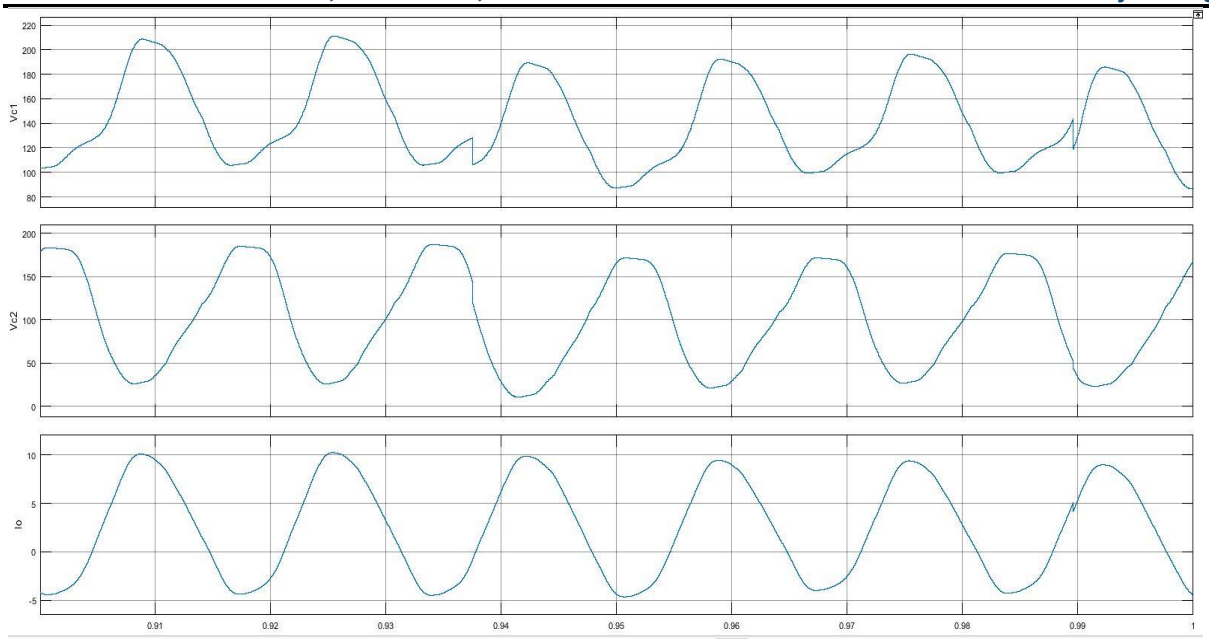


Fig 12 Vdc1,Vdc2 and Idm (load current)

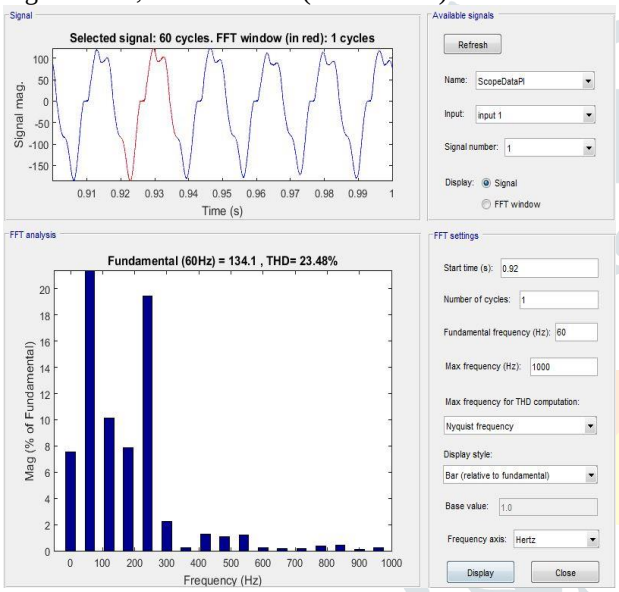


Fig.13 THD of Load current with PI controller

CONCLUSION

This paper has reviewed the root causes of fuel cells' reliability concerns when it is utilized to power single-phase UPS applications. The analysis reveals how the low-frequency current ripples could negatively impact the fuel cells as a dc source. To conquer the reliability-oriented challenge, a dual-mode operated boost inverter with meticulously designed control scheme is presented in this paper. The proposed control method maintains impressive performance under both linear and nonlinear loads. The investigation into the control system performance in conjunction with repetitive controllers suggests excellent system stability and dynamic response. In addition to the effective suppression of the low-frequency current ripples, the current ripples at switching frequency are also considerably reduced thanks to the proposed interleaved modulation.

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