JETIR.ORG ISSN: 2349-5162 | ESTD Year : 2014 | Monthly Issue
JOURNAL OF EMERGING TECHNOLOGIES AND INNOVATIVE RESEARCH (JETIR)
An International Scholarly Open Access, Peer-reviewed, Refereed Journal

AN AREA EFFICIENT LOW POWER CARRY SELECT ADDER USING MODIFIED D-LATCH

Polipalli Aasapriya, M. Tech, Research Scholar, Department of ECE, International School Of Technology and Sciences (Women), Affiliated to JNTUK, NH-16, East Gonagudem, Rajanagaram, Rajamahendravaram, AndhraPradesh, 533294, India.

D.N.V.S.Vijaya Lakshmi, M. Tech, Assistant Professor, Department of ECE, International School Of Technology and Sciences (Women), Affiliated to JNTUK, NH-16, East Gonagudem, Rajanagaram, Rajamahendravaram, Andhra Pradesh, 533294, India.

ABSTRACT

The Carry Select Adder (CSLA) is a commonly used hardware component in digital systems for performing addition operations. However, CSLAs can be quite large and power-hungry, especially in applications requiring high precision or fast operation. In this paper, we propose a modified D-Latch-based implementation of CSLA that offers significant area and power savings compared to conventional designs.

Keywords: Power efficient, Area efficient, CSLA.

I. INTRODUCTION

Low power and area efficient high-speed circuits are most substantial area in the research of VLSI design. Digital logic circuits have become the indispensable part for all electronics gadgets based on arithmetic and logical operations, the complexity of designs are increasing with each generation due to increasing need of number of task, since all the arithmetic operation are dominated by addition, therefore increasing the performance of the adder will increase the performance of the whole design. The Carry Select Adder is one of the fast adders which has less area and reduced power consumption. Carry Select Adder is favoured broadly because it limits the issue of carry propagation delay. In this article, various available design methodologies of Carry Select Adder, such as Carry Select Adder using Ripple Carry Adders (RCA), Binary to Excess Converter (BEC), D-Latch. To compensate area and power consumption in previous technology we are proposing a new technique with modified D latch. The efficiency of all the design methodologies has been investigated by comparing the parameters like area, delay and power consumption. The design with the high efficiency is used in the advanced microprocessor designs. All the architectures are simulated in Tanner tool.

II. EXISTING SYSTEM

CSLA using D-Latch

The existing system for an area-efficient low-power carry-select adder (CSLA) using D-latch is based on the principle of reducing the area and power consumption of the traditional CSLA by using D-latch instead of full adders. The D-latch-based CSLA has been shown to significantly reduce the area and power consumption compared to the traditional CSLA. the existing system of an area-efficient low-power CSLA using D-latch has shown great potential in reducing the area and power consumption of the traditional CSLA. However, there is still scope for further research to optimize the design and improve its performance.

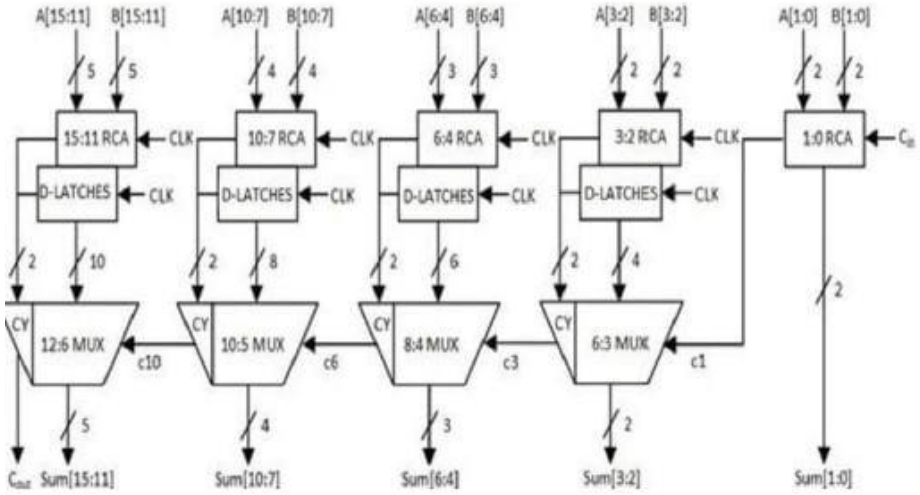

Figure : Block diagram of CSLA using D-Latch

III. PROPOSED SYSTEM

CSLA using modified D-Latch

To compensate area and power consumption in previous technology we are proposing a new technique with modified D latch, The proposed system uses the modified D-latch as the basic building block for the CSLA. The CSLA is a fast and efficient adder that operates by first generating two different carry signals, known as the carry-ripple and carry-propagate signals. These signals are used to determine whether a carry must be generated or propagated from one stage to the next.

The proposed CSLA using modified D-latch consists of two parts: a carry look-ahead (CLA) unit and a final carry-select (CS) unit. The CLA unit generates the carry-ripple and carry-propagate signals, which are then used in the CS unit to determine whether a carry must be generated or propagated.

The CLA unit is designed using modified D-latches, which are used to generate the carry-propagate and carry-ripple signals. The carry-propagate signal is generated using a modified D-latch with transmission gates, which provides a fast and efficient carry-propagate signal. The carry-ripple signal is generated using a modified D-latch with inverters, which provides a slower but more robust carry-ripple signal.

The CS unit is designed using two modified D-latches, one for the sum bit and one for the carry bit. These modified D-latches are connected in parallel, and the final output is selected based on the carry-propagate and carry-ripple signals generated by the CLA unit.The proposed system of CSLA using modified D-latch provides an area-efficient and low-power solution for high-speed arithmetic operations. The use of modified D-latches provides a fast and efficient way to generate carry signals, while minimizing the power and area requirements of the adder.

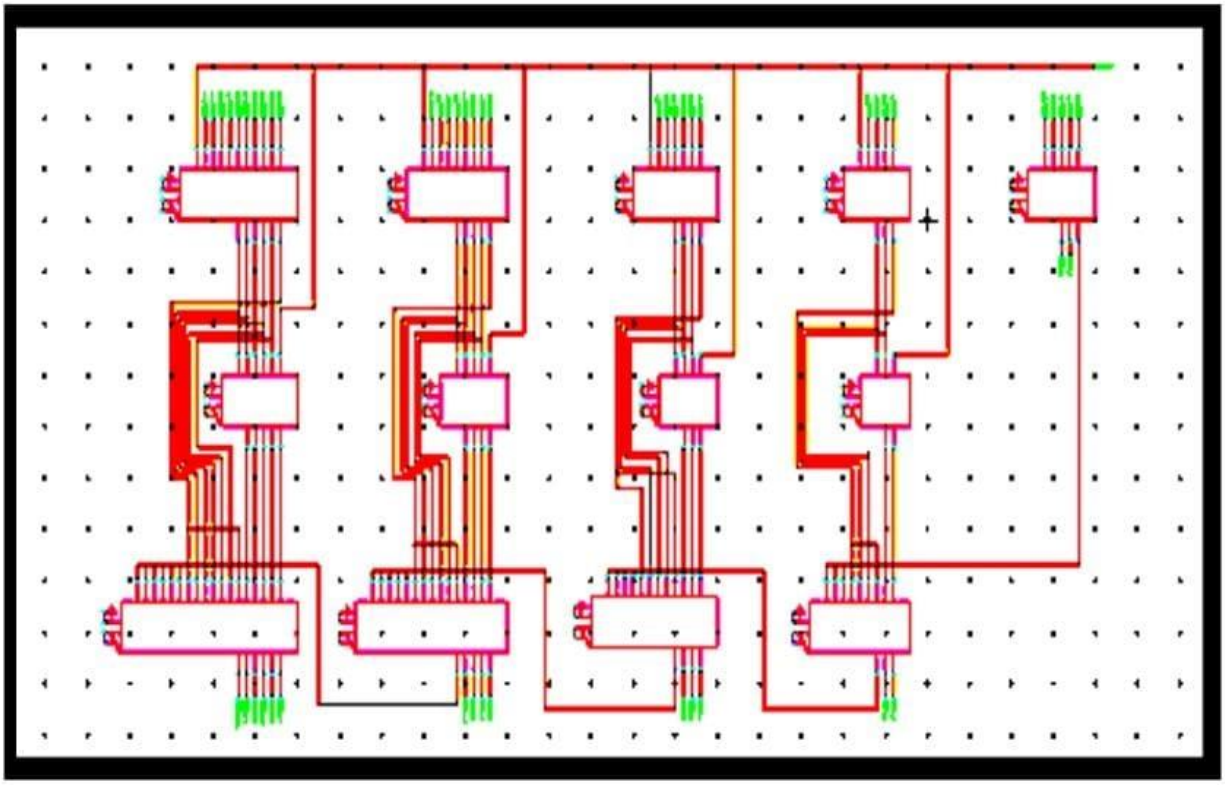

Figure: Schematic diagram of CSLA using modified D-Latch

IV. OUTPUT WAVEFORMS

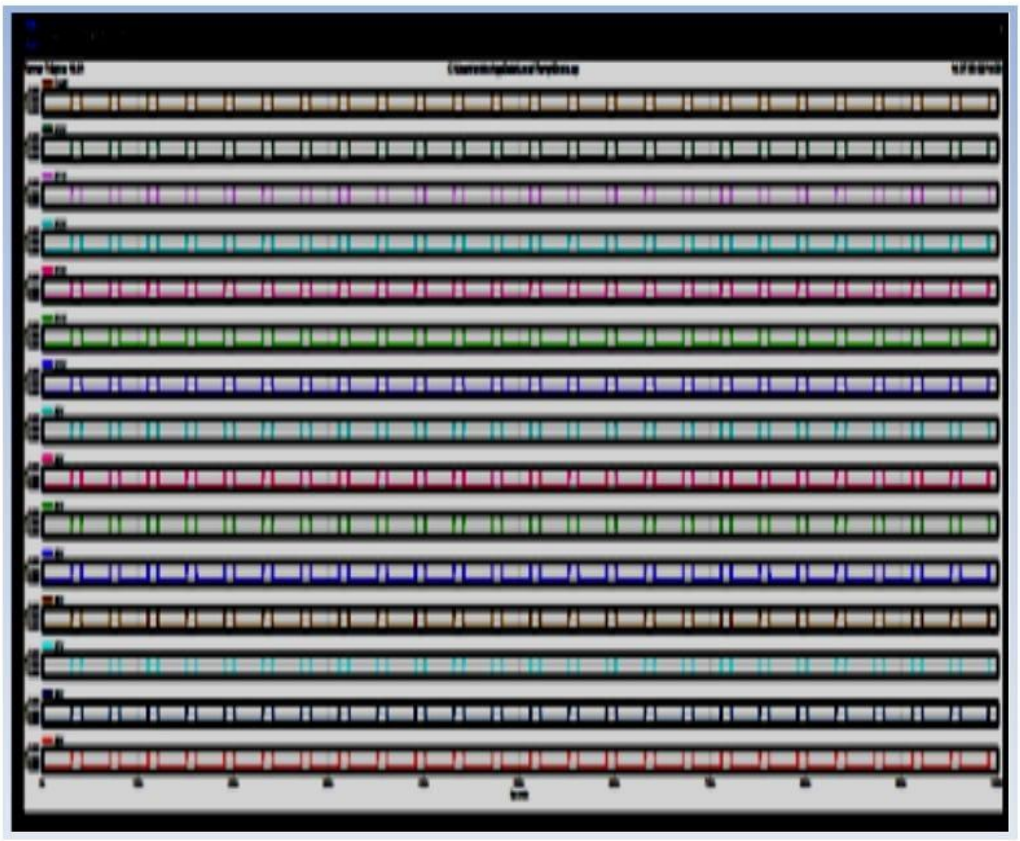

Figure: Output waveform of CSLA using modified D-Latch

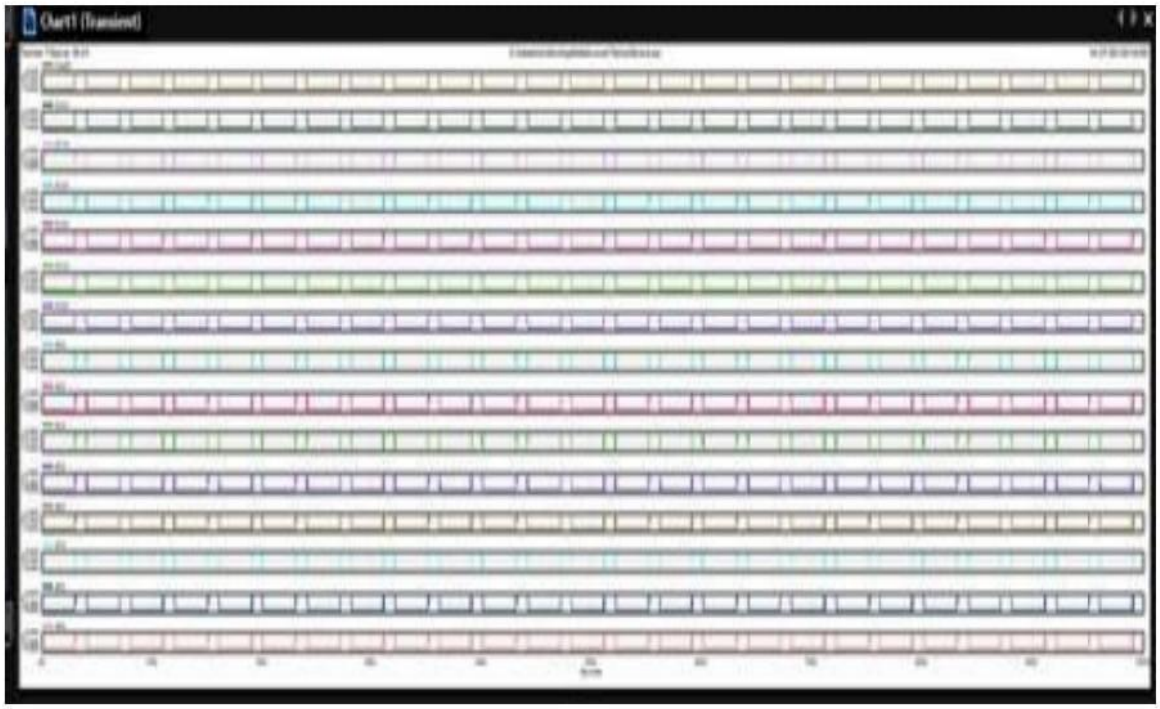

Figure: Output waveform of CSLA using modified D-Latch

V. RESULTS

Results show that CSLA using modified D-Latch has less power consumption and require less number of transistors when compared with other architectures.

Architecture	Area (No of transistors)	Power (watts)	Delay (ps)
CSLA using D-Latch	1540	201	152.34
CSLA using modified D-Latch	1428	188	149.16

Table: Comparison between Proposal and Conventional method Parameters

VI. ADVANTAGES

Faster speed

Reduced Power Consumption

Improved area

VI. APPLICATIONS

High speed arithmetic logic units

Digital signal processing

High speed data processing

Field programmable gate arrays.

VIII. CONCLUSION

A simple and efficient approach design is Carry Select Adder using modified D –latch. In this proposed design the area, power and delay are reduced. The reduced numberof gates offers great advantage in the reduction of area, power and delay. The area, power and delay of the proposed design has deduced which indicates the success of the method and not a mere trade off of delay for power and area. The modified CSLA architecture is therefore, low area, low power, less delay, simple andefficient for VLSI hardware implementation.

IX. FUTURE SCOPE

Results This work has been designed for 16-bit word size and results are evaluated for parameters like area, delay and power. This work can be further extended for higher number of bits. The proposed architecture can be designed in order to reduce the power, area and delay of the circuits. Steps may be taken to optimize the other parameters like

frequency, number of gate clocks, length etc..

X. References

[1] Nagulapati Giri and Muralidharan D, "A Survey on Various VLSI Architectures of Carry Select Adder", IJITEE ISSN: 2278-3075, Volume-8 Issue-5 March, 2019.

[2] Sahu, S. K., and Sahu, S. "Design of Area Efficient and Low Power Carry Select Adder using Modified D-Latch," International Journal of Electronics and Communication Engineering & Technology, vol. 8, no. 2, pp. 30-41, Mar-Apr 2017.

[3] D. D. Shivashankar and R. V. Jagadeesh Kumar, "Design of Area Efficient Low Power Carry Select Adder using Complementary Pass Transistor Logic," International Journal of Engineering Research & Technology, vol. 3, no. 2, pp. 252-256, Feb. 2014.

[4] P. M. Nagendra Kumar, P. H. P. Kumar, and S. S. Varma, "Design of a Low-Power and High-Speed Carry-Select Adder Using Efficient GDI Techniques," International Journal of VLSI Design & Communication Systems, vol. 2, no. 2, pp. 105-112, Mar-Apr 2011.

[5] M. A. Riyaz, V. H. Rajashekar, and K. V. R. M. Prasad, "Low Power and High Speed Carry Select Adder using GDI Technique," International Journal of Computer Applications, vol. 19, no. 3, pp. 23-26, May 2011.