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A NEW SINGLE PHASE 33-LEVEL INVERTER TOPOLOGY WITH MINIMAL NUMBER OF SWITCHES USING HALF-HEIGHT MODULATION TECHNIQUE

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Abstract: This work proposes an asymmetrical H-bridge based multilevel inverter with minimal switch count. This circuit has thirty-three level output with eight semiconductor switches, four bidirectional switches, and four unequal voltage sources. This topology has an inherent H-bridge to invert the levels at the fundamental frequency. The Half-Height modulation technique is used to generate the switching pulses. This topology is suitable for RL load and could be used to drive applications. The performance of the proposed asymmetrical multilevel inverter circuit is verified by extensive simulation using MATLAB Simulink. The simulation results confirm that the total harmonic distortion of the output voltage complies with IEEE 519 standards.

Keywords - multi-level inverter, MOSFET, THD, half-height modulation, MATLAB.

I. INTRODUCTION

The academic and industrial sectors are very interested in multilevel inverters. Multi Level strategies improve the inverter's output power quality while also allowing for higher voltage levels in power electronic circuits. [1]. Low–medium rated semiconductor switches are available on the market and can be used to achieve higher power levels. A sequential connection of switches is required to create a high rated converter with standard two-level operation. Because of their benefits, multilevel inverters are used in a variety of applications, including uninterruptible power supply systems (UPS) [2], hybrid photovoltaic UPS systems [3], traction [4], ships [5], renewable systems [6], electric vehicles [7], and power quality [8]. Multilevel converters, despite their differences, frequently need a large number of switches consisting of greater losses and costs, and use significant modulation techniques. Many research studies are being undertaken to solve these issues.

Neutral point clamped (NPC) MLIs, flying capacitor (FC) MLIs, and cascaded H-bridge (CHB) MLIs are the three primary types of MLIs [9]. Over the last two decades, the benefits and drawbacks of the three types of MLIs outlined above have been thoroughly researched. In summary, the major disadvantages of these MLIs include altering the voltage in NPC, the control complexity for making a balance in voltages in the FC, and the more switches count and independent excitations in CHB. Cascaded MLIs may provide more voltage levels, and dependability than other MLI topologies due to their modular architecture. [10]. Asymmetric MLIs are topologies with uneven dc-link voltages, whereas symmetric cascaded inverters have equal dc sources. Asymmetric topologies may give a wider range of output voltage values than symmetric topologies. These are not possible to implement practically and difficult to balance the supplied power across every source of the circuit with the load with the existence of two or more excitations with same magnitudes [11]. Many techniques for opting the size of input sources are described to get a larger output level asymmetric type of design. Reference [12] Describes a single-sourced MLI that employs various types of configurations such as equal and unequal sources, series and parallel voltage balancing methods in capacitor in order to double the magnitude of the input voltage. The inverter TSV is relatively low because there is no extra H-bridge circuit. Utilizing two unequal sources and dual capacitors, the inverter [13] is able to produce 13 levels at its output. Because the connection type as cascade with the other modules offers greater levels at the output without the use of an extra H-bridge, reducing stress across the switches in this type of configuration. MLI [15] covers the usage of T-type architecture and cross sectional-connected units to produce the output. Due to the extra power switches in this configuration in order to facilitate charging and discharging behavior of the capacitor, stress across the switches is high. The topology in [14] finds a second-order connection between the peak inverse voltages of the circuit (PIV) with levels count. As a result, the inverter is expensive and unsuitable for applications requiring high voltage.

A 33-level asymmetric MLI architecture is proposed and implemented in this work, with lower THD. The number of switches, voltage levels, DC source count and RL load are used to determine MLI's total harmonic distortion. The developed MLI is built using simulations in the environment of MATLAB/Simulink. where it is evaluated under various loaded circumstances such as combination of both resistive and inductive loads. The MLI THD is compared to that of different current topologies.

In this paper, work has been carried out with the aim of reducing the number of power semiconductor devices, while achieving a higher number of levels at the same time. This paper is organized as follows: Section II describes the topology with its extension for a higher number of levels. To set the benchmark of this topology, Section III gives a quantitative comparison of the topologies employing the same number of switches. Section IV elaborates the various experimental results and Section V summarizes the work.

Table 1 Switching states for 33 level Inverter topology

Voltage Level	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}
16Vdc	0	1	1	0	0	1	1	0	1	0	0	1
15Vdc	0	1	1	0	0	1	1	0	1	0	1	0
14Vdc	0	1	1	0	0	1	0	1	1	0	0	1
13Vdc	0	1	1	0	0	1	1	0	0	1	0	1
12Vdc	0	1	0	1	0	1	1	0	1	0	0	1
11Vdc	0	1	0	1	0	1	1	0	1	0	1	0
10Vdc	0	1	0	1	0	1	0	1	1	0	0	1
9Vdc	0	1	0	1	0	1	0	1	1	0	1	0
8Vdc	0	1	0	1	0	1	1	0	0	1	1	0
7Vdc	0	1	0	1	0	1	0	1	0	1	0	1
6Vdc	0	1	1	0	1	0	1	0	1	0	1	0
5Vdc	0	1	1	0	1	0	0	1	1	0	0	1
4Vdc	0	1	1	0	1	0	1	0	0	1	0	1
3Vdc	1	0	1	0	0	1	1	0	1	0	0	1
2Vdc	1	0	1	0	0	1	1	0	1	0	1	0
Vdc	0	1	0	1	1	0	0	1	1	0	0	1
0	0	1	0	1	1	0	0	1	1	0	1	0
Vdc	1	0	1	0	0	1	1	0	0	1	1	0
-2Vdc	0	1	0	1	1	0	0	1	0	1	0	1
-3Vdc	0	1	0	1	1	0	0	1	0	1	1	0
-4Vdc	1	0	0	1	0	1	0	1	1	0	1	0
-5Vdc	1	0	0	1	0	1	1	0	0	1	1	0
-6Vdc	1	0	0	1	0	1	0	1	0	1	0	1
-7Vdc	1	0	1	0	1	0	1	0	1	0	1	0
-8Vdc	1	0	1	0	1	0	0	1	1	0	0	1
-9Vdc	1	0	1	0	1	0	1	0	0	1	0	1
-10Vdc	1	0	1	0	1	0	1	0	0	1	1	0
-11Vdc	1	0	1	0	1	0	0	1	0	1	0	1
-12Vdc	1	0	1	0	1	0	0	1	0	1	1	0
-13Vdc	1	0	0	1	1	0	0	1	1	0	1	0

-14Vdc	1	0	0	1	1	0	1	0	0	1	1	0
-15Vdc	1	0	0	1	1	0	0	1	0	1	0	1
-16Vdc	1	0	0	1	1	0	0	1	0	1	1	0

II. MULTILEVEL INVERTER WITH REDUCED SWITCH COUNT

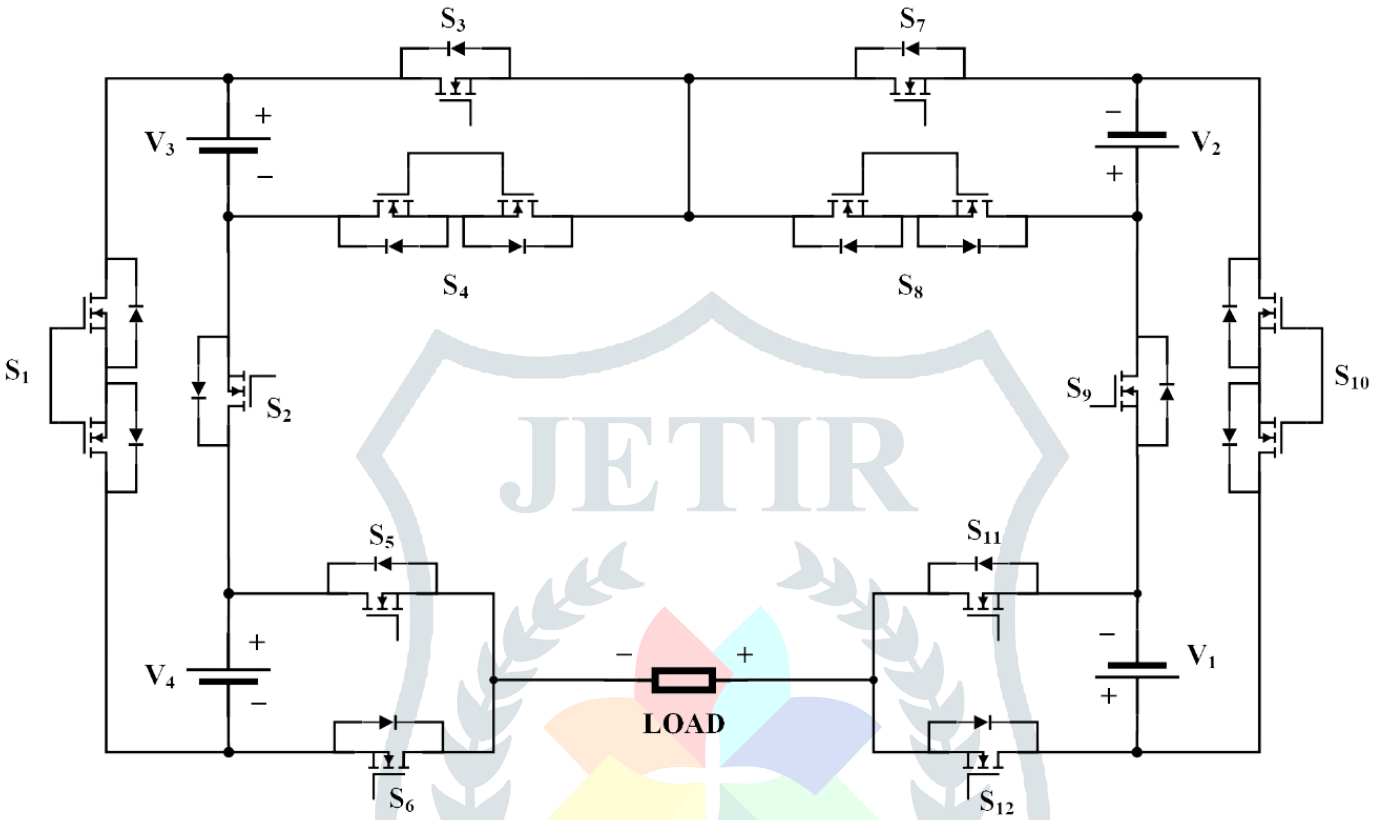
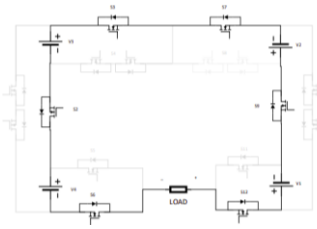


Figure 1. 33 Level Inverter Topology

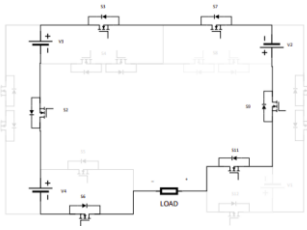
The circuit configuration of the developed 33-level MLI topology is represented in Figure 1. It has eight unidirectional and four bidirectional semiconductor switches with four input DC voltage sources. The basic unit of the proposed architecture is able to generate thirty-three levels of voltage at the output. The magnitudes of the input DC sources V1, V2, V3, and V4 are selected in the ratio of 1:2:4:9 [31].

2.1 Mode of Operation

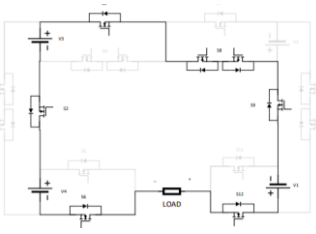
The basic unit generates 33 number of voltage levels, including 0V, ±1Vdc, ±2Vdc, ±3Vdc, ±4Vdc, ±5Vdc, ±6Vdc, ±7Vdc, ±8Vdc, ±9Vdc, ±10Vdc, ±11Vdc, ±12Vdc, ±13Vdc, ±14Vdc, ±15Vdc and ±16Vdc at its output with a step size of Vdc with the DC voltage sources of V1 = 1VDC, V2 = 2VDC, V3 = 4Vdc, V4 = 9Vdc. The proposed configuration generates 16 positive output voltage steps from +Vdc to +16Vdc, zero output voltage step, and 16 negative output voltage steps from −Vdc to −16Vdc. The switching states for the proposed 33-level MLI during both levels of operation (positive and negative) is represented in TABLE 1. The current paths to the load along with the voltage stress.



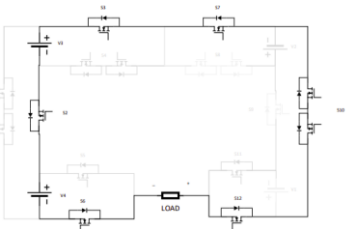
+16Vdc



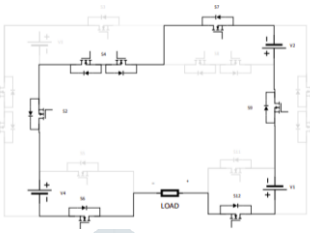
+15Vdc



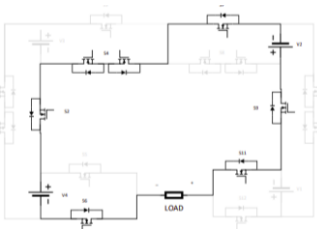
+14Vdc



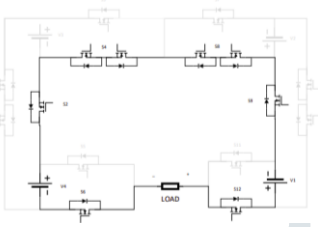
+13Vdc



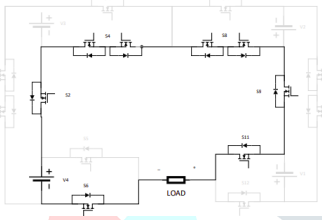
+12Vdc



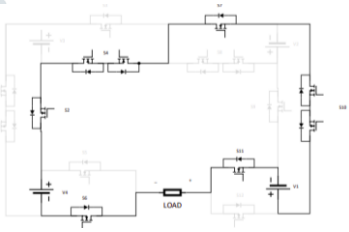
+11Vdc



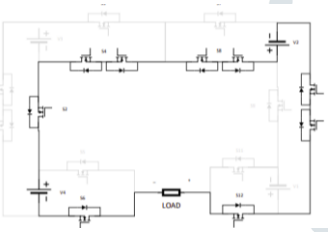
+10Vdc



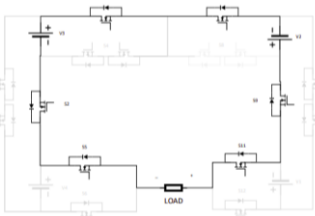
+9Vdc



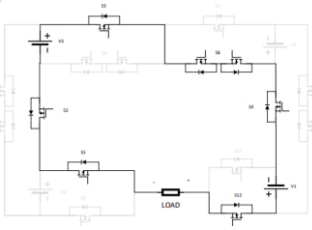
+8Vdc



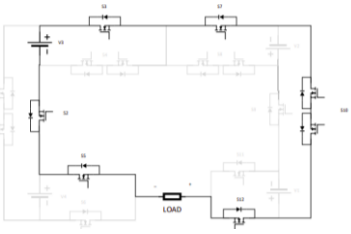
+7Vdc



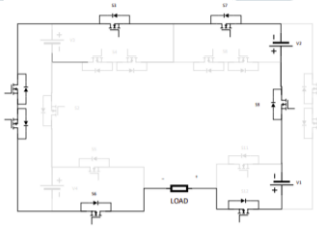
+6Vdc



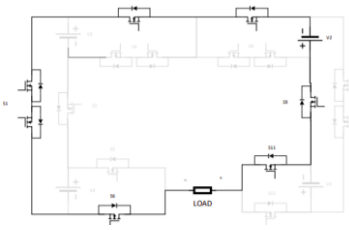
+5Vdc



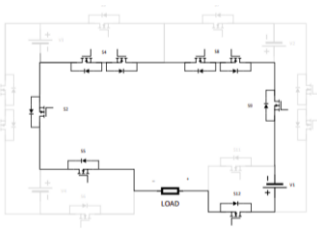
+4Vdc



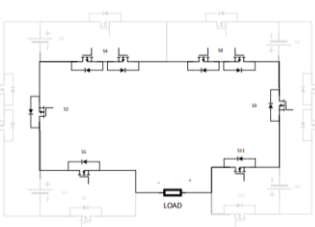
+3Vdc



+2Vdc



+1Vdc



0Vdc

2.2 Design of Load

RMS Voltage (Vrms) = 230 V

Power = 3000 W

I = P/V cos φ = 3000/230 * 0.8 = 16.3 A, RMS Current (Irms) = 16.3 A

Frequency (f) = 50 Hz

Impedance (Z) =V_{rms} / I_{rms} => Z = 230/16.3 = 14.11 Ω

We know that cos φ = RZ

R = cos φ * Z = 0.8 * 14.11 = 11.28 Ω

Inductance value is obtained by inductive reactance (XL) which can be calculated as,

$X_L^2 = Z^2 - R^2$ (from the equation $Z^2 = R^2 + X_L^2$) => X_L = 8.46 Ω

But $X_L = L * \omega$. Then, $L = X_L /(2 * \pi * 50)$. Therefore, L = 8.46/(2 * π * 50) => L = 0.026 H

2.3 Switch Ratings

Table 2 Ratings of the switch

Voltage Ratings of the Switch	Current Ratings of the Switch
RMS Voltage, V_{rms} = 230 V Peak voltage, $V_p = \sqrt{2} * 230$ = 325.26 V Let us consider a safety margin (safety factor) as 10% Therefore, 10% of 325.26V is 32.52V Including safety margin, Total voltage is V_t = 325.26 + 32.52 = 357.78V	Load current, I_L = 16.3A Safety margin is 10% above the load current, i.e. 1.63 A Therefore, current rating of the switch is I = 16.3 + 1.63 = 17.93A ≅ 18A

The switching frequency of the inverter output is 50Hz

2.4 Modulation Technique for the Inverter

2.4.1 Half-Height (HH) Modulation Technique

This modulation technique gives better total harmonic distortion as compared to equal phase modulation technique.
In the Half Height switching modulation technique the total period (0 – 360 degrees) of the output waveform are divided into four quadrants i.e.

1. The period from 0 to 90 degree is referred as the main switching angle which is calculated as,

$$a_k = \frac{(2k-1)}{(N-1)} \qquad (2.1)$$

Where, k = 1, 2, 3, 4……$\frac{(N-1)}{2}$ and N = Number of output voltage levels

2. The period from 90 to 180 degree is referred as the second quadrant switching angle which is calculated as,

$$a_{\frac{N+1}{2}} = \pi - a_{\frac{N-1}{2}}, \pi - a_{\frac{N-2}{2}}, \ldots\ldots\ldots, \pi - a_1 \qquad (2.2)$$

3. The period from 180 to 270 degree is referred as the third quadrant switching angle which is calculated as,

$$a_N = \pi + a_1, \pi + a_2, \ldots\ldots\ldots, \pi + a_{\frac{N-1}{2}} \qquad (2.3)$$

4. The period from 270 to 360 degree is referred as the final quadrant switching angle which is calculated as,

$$a_{\frac{3N-1}{2}} = 2\pi - a_{\frac{N-1}{2}}, 2\pi - a_{\frac{N-2}{2}}, \ldots\ldots, 2\pi - a_1 \qquad (2.4)$$

2.4.2 Equal Phase (EP) Modulation Technique

In this technique the switching ang1es are distributed averagely over the full complete cyc1e ranging from(0–360)degrees. The equation to calculate the switchinganglesbyEqual Phase angle (EP) method is given by,

$$W_s = S * \frac{180}{Q} \qquad (2.5)$$

Where S = 1, 2, 3, 4, … 2QQ = Number of output voltage levels

III. Results and Discussion

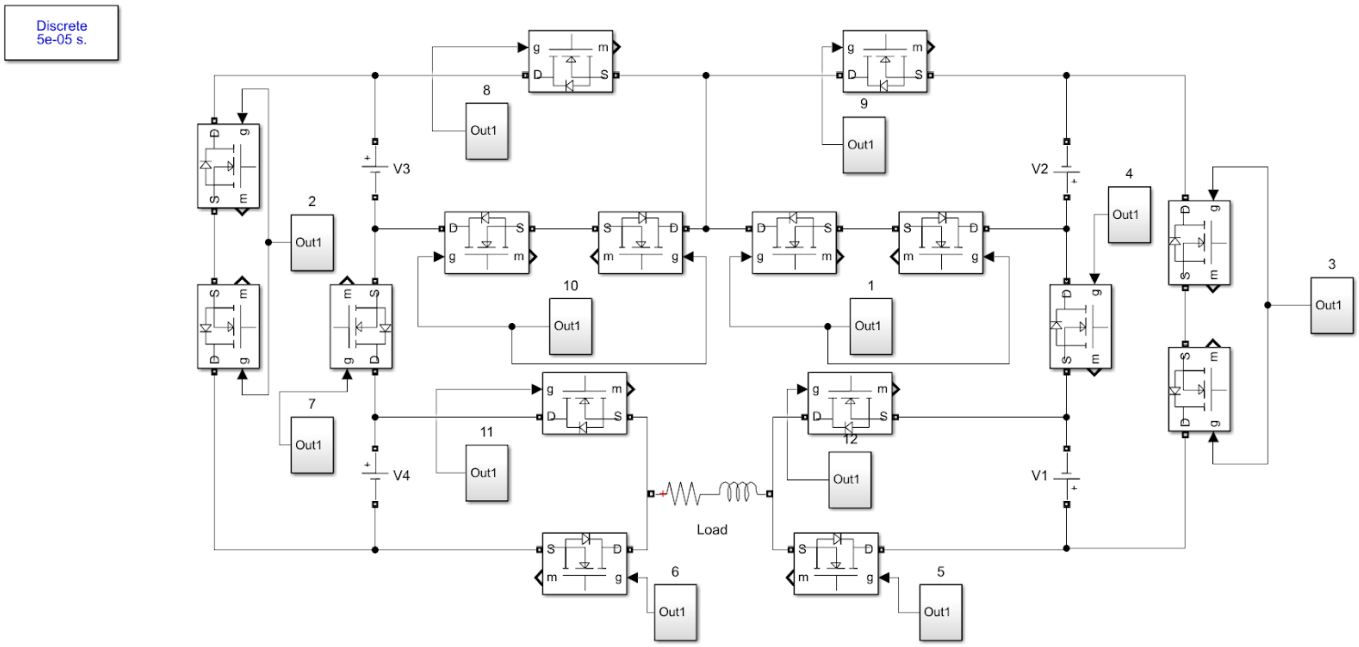
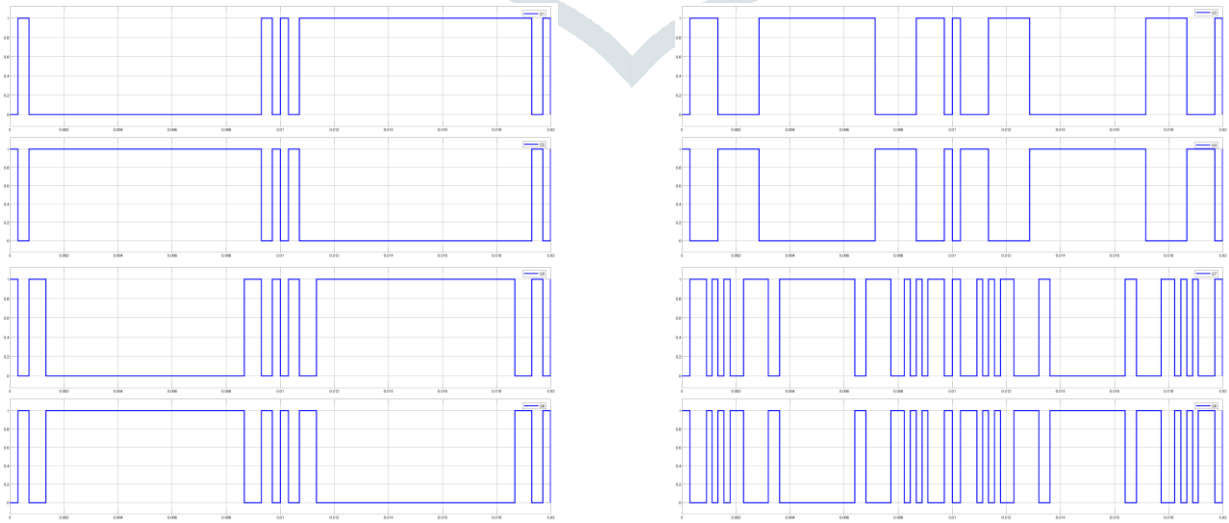


Figure 2. 33-Level Asymmetrical Inverter Simulation Circuit

In an asymmetrical switching pattern, the input DC voltages are given as V_1=36V and V_2=36V, V_3=108V, V_4=108V. The switches S_1 to S_8 are Unidirectional MOSFET semiconductor switches. The switches S_9 and S_{10} are Bi-Directional MOSFET semiconductor switches.

3.1 Gate Pulses for one full cycle



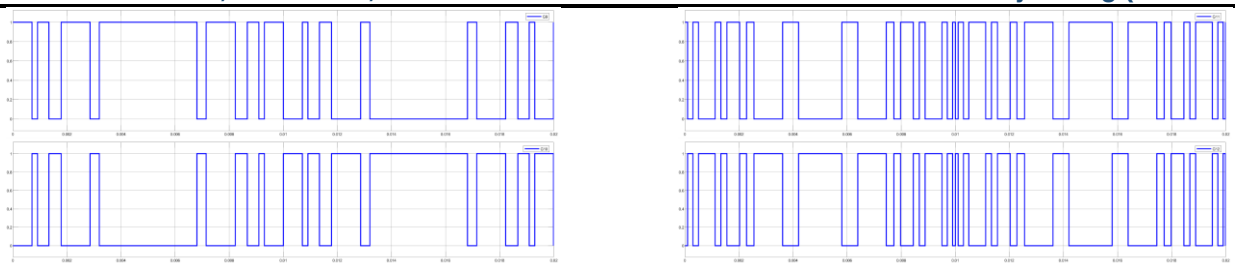


Figure 3. Gate Pulses for 33 level inverter circuit

The proposed asymmetrical multilevel inverter is simulated for the Half Height method in the MATLAB/Simulation environment. The results are analyzed for RL load. The detailed analysis of each of the above simulations was done and through detailed comparisons, inferences were made on the basis of Total Harmonic Distortion, circuit complexity, voltage stress on devices etc.

In the 33 level MLI, the circuit is built of 8 MOSFET switches. The load is RL load of R=11.288 ohms and L=0.026 H. The asymmetric dc input voltages are used in the ratio of 1:2:4:9. Figure 2. represents the simulation circuit of the proposed 33-level inverter.

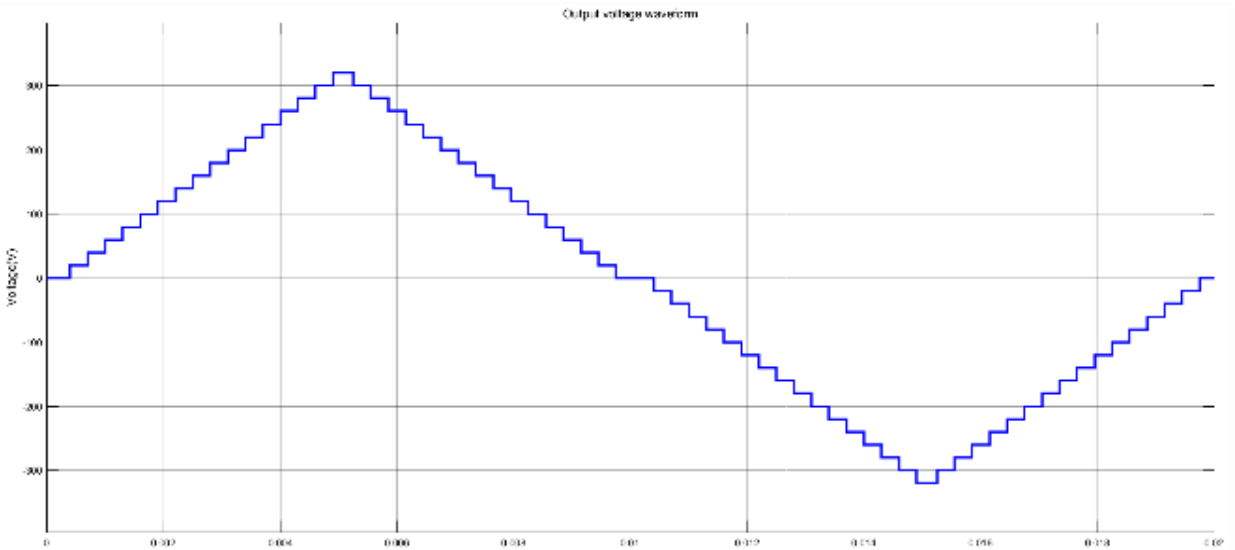


Figure 4. Output voltage waveform of 33-level Asymmetrical inverter using Equal Phase modulation technique for RL load

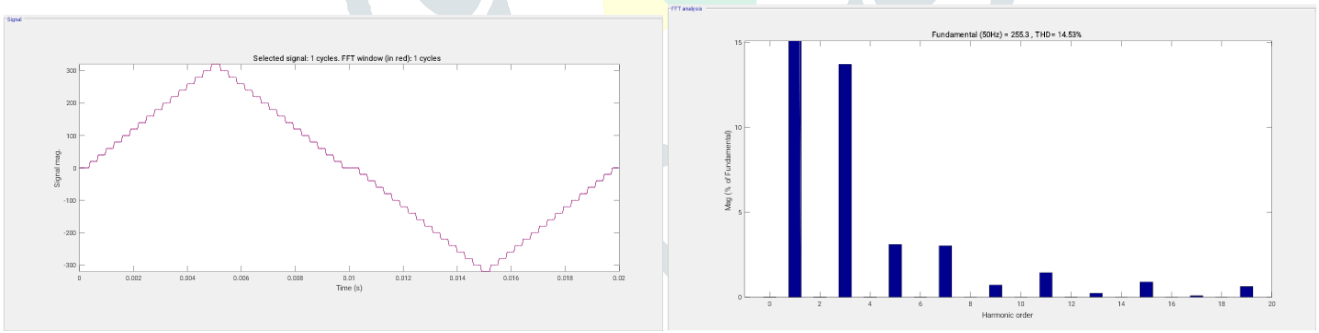


Figure 5. THD spectrum for output voltage using Equal Phase modulation technique for RL load

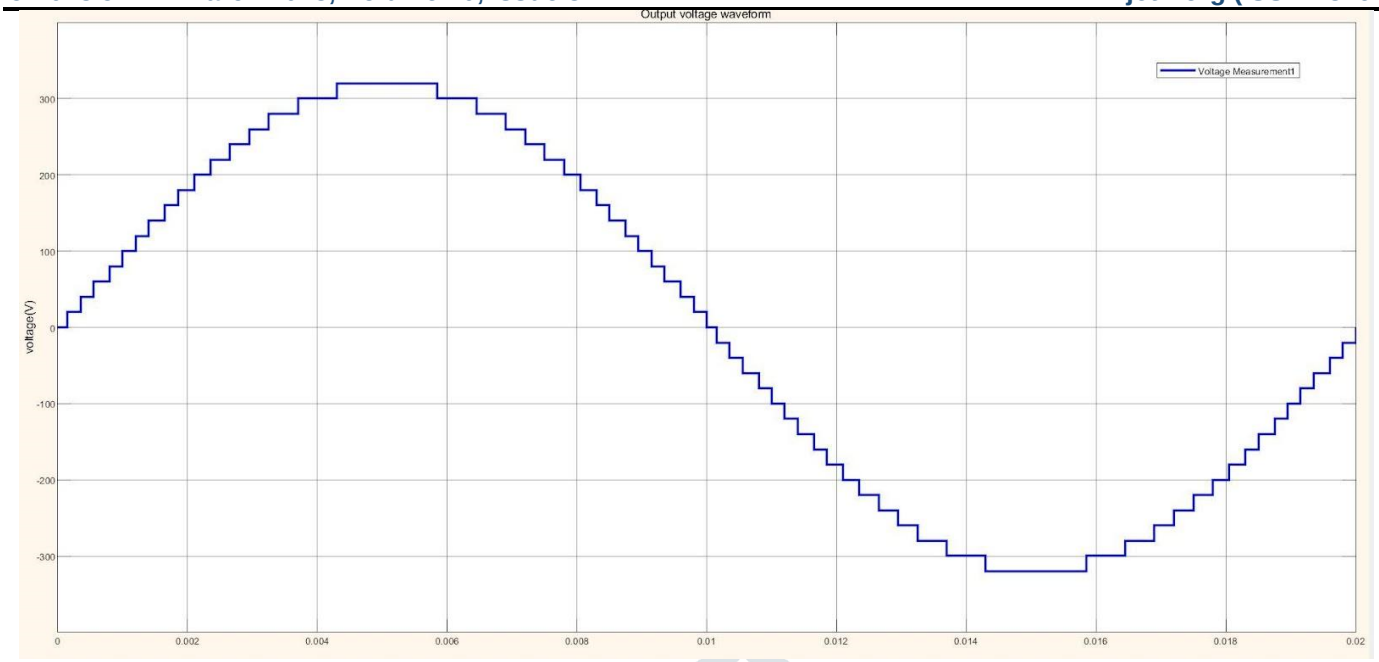


Figure 6. Output voltage waveform of 33-level Asymmetrical inverter using Half-Height modulation technique for RL load

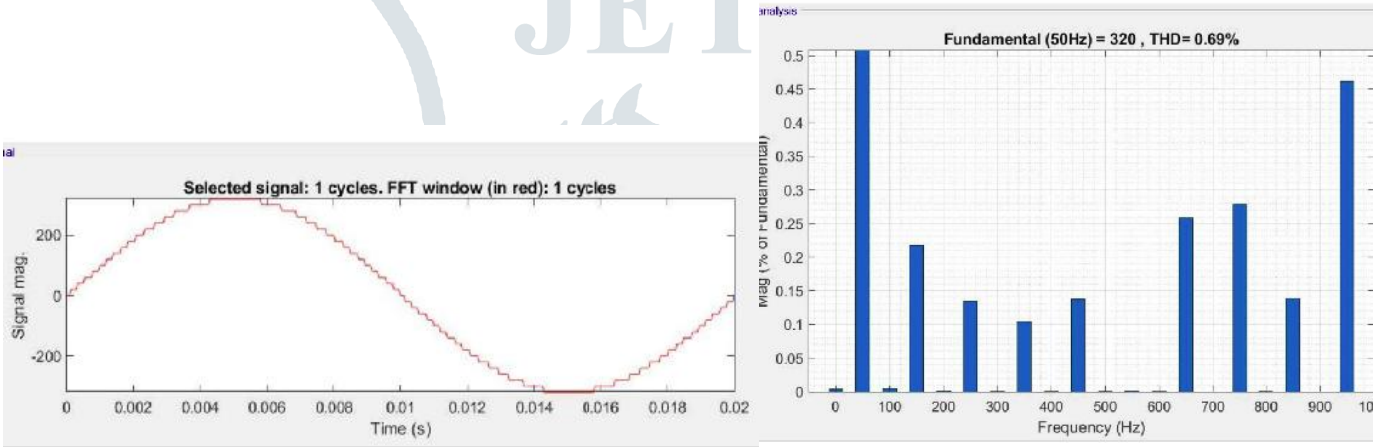


Figure 7. THD spectrum for output voltage using Half-Height modulation technique for RL load

IV. Conclusion

A new thirty-three level asymmetric multilevel inverter with minimal device count is considered in this work. The topology of the thirty-three level is demonstrated with the Equal Phase and Half-Height modulation techniques. The inverter is simulated RL load. The proposed inverter is with RL load. The total harmonic distortion of the output voltage of the multilevel inverter is 14.87 with Equal Phase modulation technique and 0.69% with Half-height modulation technique. The total harmonic distortion is similar to other thirty-three level inverter topologies, but in this work it is achieved with a minimal number of device counts. The circuit is modeled in MATLAB Simulink and results are discussed.

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