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A Survey of Wideband Semiconductor Device Switching Oscillations

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Abstract : At present, Due to their superior performance, wide bandgap (WBG) devices give power converters the benefits of high frequency, highly efficient, and high-power density. However, they are also more prone to switching oscillations because to their low parasitic capacitance and quick switching speed. The performance of power converters and systems can be significantly impacted by the switching oscillations, which can result in voltage and current overshoots, shoot-through, electromagnetic interference, additional power loss, and even device damage. Although comprehensive and in-depth on this topic is lacking. For practical engineering, this article discusses the types, the causes and detrimental effects, the effects of parasitic factors, and the suppression techniques of these switching oscillations. At first switching oscillations are divided into distinct types, and their causes and the negative effects are analyzed. The impact of various parasitic factors on switching oscillations are discussed. It is discovered that because silicon carbide metal-oxide semiconductors have various physical structures. The effects vary depending on the type of transistor used, including field-effect transistors, enhancement-mode gallium nitride high electron mobility transistors (eGaN HEMTs), and cascade GaN HEMTs. Lastly, the primary techniques for suppressing switching oscillations are outlined, together with their benefits and drawbacks. Further study on this subject and the paper's conclusion are also included, which will expand readers' understanding of the switching oscillations of WBG devices and motivate readers to use WBG devices more effectively for high frequency and high-efficiency power conversion.

IndexTerms **- High frequency, parasitic parameters, switching oscillations, wide bandgap (WBG) devices**

I. INTRODUCTION

In the past few decades, silicon (Si) devices have dominated the world of power electronics. However, as power density continues to increase, Si devices are closer to the limitations of their own materials [1], [2]. Accordingly, power devices based on wide bandgap (WBG) materials are gradually regarded as kind of promising devices [3-4]. Fig. 1 shows the advantages provided by WBG materials over conventional Si material [5-6]. For WBG materials, the energy gap, electric breakdown field, melting point, and electron velocity are all significantly higher. These characteristics make WBG devices more suitable for high-voltage and high frequency applications.

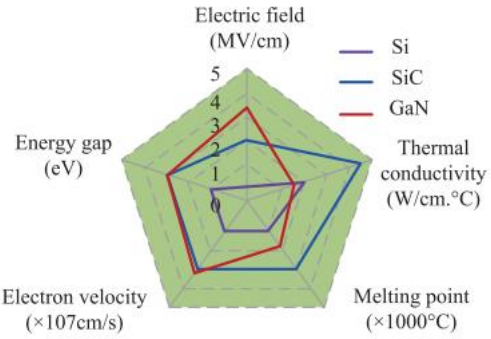

Fig. 1. Comparison of material properties of Si, silicon carbide (SiC), and gallium nitride (GaN).

As the switching frequency increases, the power density of the converter can be increased due to the reduction in the volume of the passive components [7-8]. However, high switching speed and switching frequency are more likely to cause some overshoot and parasitic ringing due to high $\frac{di}{dt}$ and $\frac{dv}{dt}$ [9-11]. More seriously, these may cause severe switching oscillations due to low on-resistance and parasitic capacitance of the WBG devices [12]. In terms of the oscillation type, the switching oscillations can be divided into damped oscillation and undamped oscillation. The damped oscillation is usually the parasitic ringing caused by resonance between the parasitic inductor of the circuit and the parasitic capacitor of the switching device. An unintentional negative differential resistance oscillator or some unique mechanisms of the device [13] commonly form the undamped oscillation. In terms of the oscillation position, the switching oscillations have the oscillations of the gate-source voltage and the oscillations of the drain-source voltage. The gate-source voltage oscillations mainly include false turn-on [as shown in Fig. 2(a)] and even more serious false triggering oscillation [as shown in Fig. 2(b)]. While the drain-

source voltage oscillations mainly include parasitic ringing generated by LC resonance [as shown in Fig. 2(c)] and the sustained oscillation which is unique to GaN devices [as shown in Fig. 2(d)].

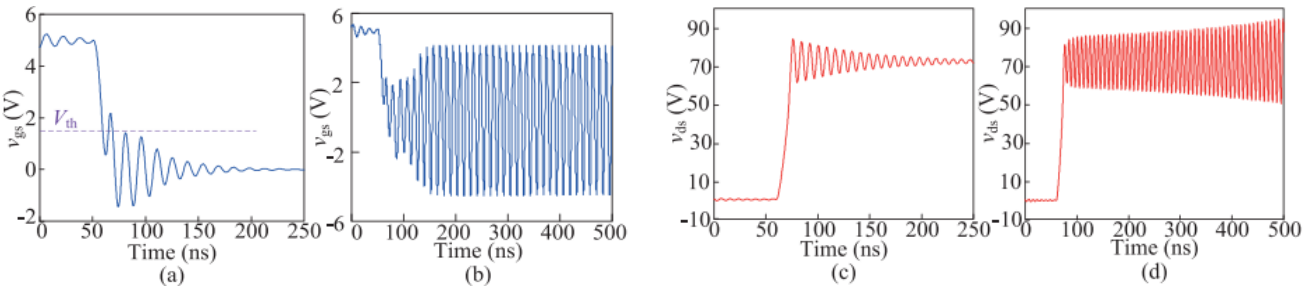

Fig. 2. Switching oscillations in phase-leg configuration. (a) False turn-ON of the gate-source voltage. (b) False triggering oscillation of the gate-source voltage. (c) Parasitic ringing of the drain-source voltage. (d) Sustained oscillation of the drain-source voltage.

The switching oscillations have serious negative effects on the power converters, including voltage and current overshoots, shoot-through; electromagnetic interference (EMI), additional power loss, and even device damage [14-16]. Accordingly, researchers have done a lot of work on some particular oscillation in order to solve these problems [17-18]. These studies explore switching oscillations through specific parameters [19], mechanisms [20], or analytical modeling and propose some solutions. For example, reducing the common source inductance and increasing the gate resistance can suppress the sustained oscillation of the drain source voltage [12]. Reducing stray gate-loop inductance and switching speed and adding a small ballasting capacitor across the gate–source terminals can suppress the false triggering oscillation of the gate-source voltage. Additionally, some reviews related to WBG devices have been presented recently, such as the basic structure, physical performance, and commercialization challenges. In addition, the loss distribution, measurement techniques, and applications of the WBG devices are summarized in [21]. As mentioned above, the switching oscillations are closely related to the performance of power converters, it is very important to have a deep and thorough review on the generation mechanisms, parasitic parameter impact analysis, and suppression methods of them for better use of the WBG devices. However, there is no such review up to now within the scope of our knowledge.

The rest of this article is organized as follows. The causes and negative effects of the switching oscillations are analyzed in Section II. Section III presents the main methods to suppress the switching oscillations, and the advantages and disadvantages of them are comparably analyzed. Finally, conclusion drawn from this research is presented in Section IV.

II. Causes And Negative Effects Of Switching Oscillations

2.1 Causes of Switching Oscillations

Commonly, WBG devices have much faster switching speed than Si devices due to their low parasitic capacitance. However, faster switching speed means higher $\frac{di}{dt}$ and $\frac{dv}{dt}$, which leads to a greater oscillation challenge. In the following, the causes of the four typical switching oscillations shown in Fig. 2 are particularly presented

1) False Turn-on and False Triggering Oscillation of the Gate-Source Voltage: The false turn-ON mechanism of the Si MOSFETs is greatly related to the recovery current of the body diode in addition to the high $\frac{di}{dt}$ and $\frac{dv}{dt}$. However, the SiC MOSFETs have a quite low reverse recovery current and the GaN MOSFETs have no reverse recovery current. It is discovered that the false turn-ON of the WBG devices is mainly caused by high dv/dt and di/dt. Fig. 3 shows the false turn-ON problems in the phase-leg configuration, which are the turn-ON gate oscillation and the turn-OFF gate oscillation, as shown in Fig. 3(a) and (b), respectively. For the turn-ON gate oscillation, the drain-source voltage of the top switch Q1 increases rapidly during the turn-ON process of the bottom switch Q2. Due to the fast-switching speed, the displacement current through the Miller capacitor Cgd1 will be induced by high dv/dt and flows to the gate node, which may result in high gate-source voltage vgs1. In addition, the high di/dt produces a negative voltage on the common source inductor (CSI) Ls1, which further increases vgs1. Accordingly, the false turn-ON and even more severe false triggering oscillation may occur. For the turn-OFF gate oscillation, the current through the Miller capacitor Cgd2 caused by high dv/dt must be sunk through the gate inductor LG2 when the bottom switch Q2 is turned OFF. The oscillation between the gate inductor and the input capacitor may also cause the gate-source voltage vgs2 to exceed its threshold voltage, and results in false turn-ON.

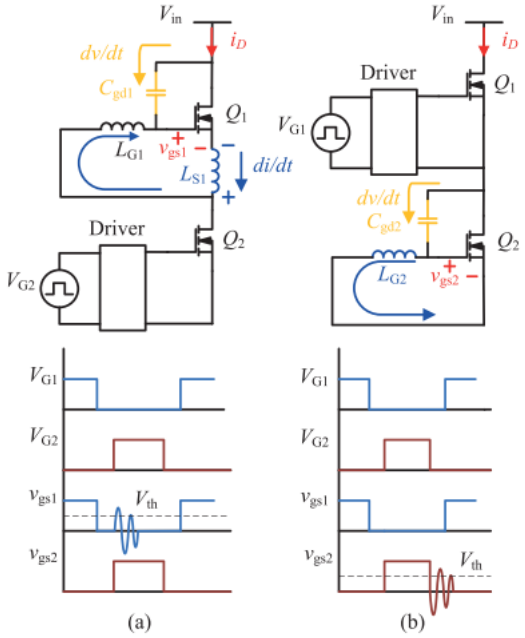

Fig. 3. False turn-ON problems in phase-leg configuration. (a) Turn-ON gate oscillation. (b) Turn-OFF gate oscillation.

2) Parasitic Ringing of the Drain-Source Voltage: The parasitic ringing of the drain-source voltage mainly occurs in the turn-ON and turn-OFF transients of the switch. Fig. 4 shows the equivalent circuit for the parasitic ringing period in a synchronous buck converter. It can be observed that when the switch is turned OFF, only the output capacitor needs to be considered, and the power loop parasitic inductor of the circuit resonates with the parasitic capacitor of the switch. Accordingly, the parasitic ringing occurs. Because of the high ringing frequency, the high-frequency damping resistor Rloop will be generated, which represents the loss related with the high-frequency ringing current, such as high-frequency power loop resistor, radiation loss, etc. Since the ringing frequency is often above 100 MHz, the high-frequency ac resistance is much greater than the dc resistance due to the skin effect and the proximity effect. The skin effect and the proximity effect have a significant influence on the current distribution in conductors and devices, making the current crowd to the adjacent side surfaces of the conductors and devices. The higher the frequency, the more obvious the skin effect, which will cause the high-frequency ac resistance to be several times greater than the dc resistance. The amplitude and oscillation time of the parasitic ringing are greatly affected by Rloop.

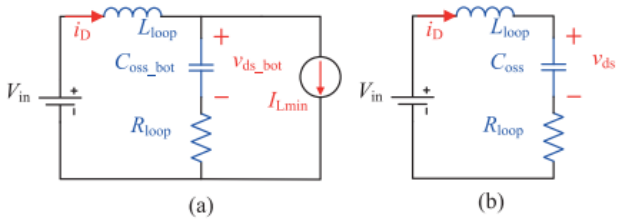

Fig. 4. Equivalent circuit of parasitic ringing of the synchronous buck converter. (a) Ringing period when the top switch is turned ON. (b) Ringing period when the top switch is turned OFF. (Coss-bot is the output capacitance of the bottom switch and Coss is the output capacitance of the top switch.)

3) Sustained Oscillation of the Drain-Source Voltage: The sustained oscillation occurring in GaN devices is analyzed in. This oscillation will not occur in Si and SiC MOSFETs based circuits. The main reason lies in that the reverse conduction characteristics of GaN devices are quite different from that of Si and SiC MOSFETs. Si or SiC MOSFETs have body diodes to conduct reverse current, while GaN devices do not have body diodes. When the gate-source voltage vgs or gate-drain voltage vgd is greater than the threshold voltage of the GaN device, the electrons are attracted to the heterostructure interface of the aluminum gallium nitride and GaN so that the two-dimensional electron gas is reestablished, and thus the GaN devices can conduct reverse current. Fig. 5 shows the simplified structure of GaN devices when conducting reverse current. The phase-leg configuration circuit with an inductive load in Fig. 6(a) is used to study this sustained oscillation. When the active switch Q2 is turned OFF, the load inductor current IL flows through Q1 from its source to drain, which may cause the gate-drain voltage vgd to exceed the threshold voltage and Q1 has a channel current. In this case, the sustained oscillation may occur due to the reverse conduction characteristics of GaN devices and parasitic parameters. It should be noted that when the sustained oscillation occurs, the gate-source voltage of Q2 is normal, thus Q2 only considers the output capacitor Coss2. Accordingly, the small-signal circuit diagram is shown in Fig. 6(b). The small-signal circuit can also be described by a feedback system, as shown in Fig. 7. The sustained oscillation will occur when the feedback system satisfies the Barkhausen stability criterion.

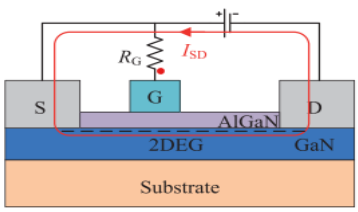

Fig. 5. Simplified structure of GaN devices when conducting reverse current.

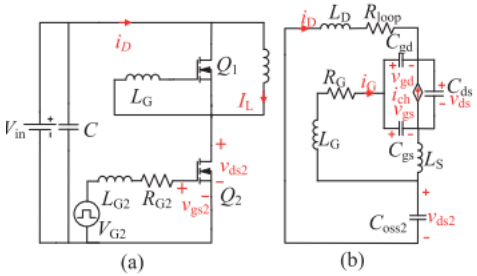

Fig. 6. (a) Phase-leg configuration circuit and (b) its small-signal circuit diagram .

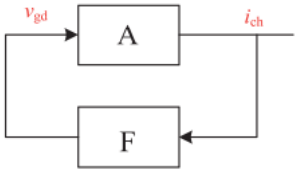

Fig. 7. Block diagram of the feedback system. (A is the amplified gain and F is the feedback transfer function.)

2.2 Negative effects of Switching Oscillations

The switching oscillations can cause many undesired negative effects, including voltage and current overshoots, shoot-through, EMI, additional power loss, and even device damage, which can seriously affect the performance of power converters and systems.

1) Voltage and Current Overshoots: Voltage and current overshoots are reported in and during the turn-OFF transient of the switch, the parasitic inductor of the circuit resonates with the parasitic capacitor of the device, which causes voltage and current overshoots. In the SiC turn-OFF switching waveforms in the phase-leg configuration are studied. Under the test conditions that the input voltage is 300 V and the drain current is 75 A, the turn-OFF voltage peak-to-peak value of SiC device reaches Vpp = 300 V. It is shown that under the test conditions of input voltage 600 V and load inductor current 20 A, the turn-OFF voltage amplitude of SiC device reaches 848.3 V. When the power loop inductance is increased from 100 to 200 nH, the turn-OFF voltage overshoot is more serious, which indicates that the power loop inductance has a significant effect on the voltage overshoot. Therefore, the PCB layout and device package should be optimized to reduce the parasitic inductance and the related voltage overshoot.

2) Shoot-Through: As mentioned earlier, high dv/dt and di/dt may cause the gate-source voltage to exceed the threshold voltage, thereby inducing the false turn-ON. At this time, another switch in the same phase-leg is also in the conducting state, which may generate a very large current and cause the device to pass through or be damaged eventually. In it is shown that when the false turn-ON occurs, the load inductor current IL increases with Vin/Lloop (where Vin is the input voltage and Lloop is the power loop inductance), because Lloop must take almost all the source voltage of Vin (where Vin = Lloop × dIL/dt), a large short-circuit current will pass through the two switches. From the experimental results, the short-circuit current rises to nearly 150 A, which seriously affects the performance and reliability of the system.

3) Electromagnetic Interference: During the switching transients, switching oscillations induced by high dv/dt,di/dt and resonance of parasitic inductor and capacitor may also cause severe conducted and radiated EMI noise. According to the current conducting direction, conducted EMI (150 to 30 MHz) can be divided into common mode and differential mode emissions. Conducted and radiated EMI emissions often produce undesirable effects on electronic systems, such as radio receivers, medical equipment, and communication systems. Furthermore, they cause malfunctions and non-operations in control systems.

4) Additional Power Loss: In addition to the abovementioned problems, the switching oscillations can also cause additional power loss. In particular, the CSI has been extensively studied due to the sharing of the driver loop and the power loop. The CSI acts as negative feedback to slow down the driver during the turn-ON and turn-OFF transitions and significantly increases the switching losses. In the effect of CSI on the switching loss of SiC MOSFET has been explored based on boost converters. The experimental results show that the switching energy per cycle increases 9.2% from 148.4 to 162.0 μJ at hard-switching mode after the CSI increases from 0 to 8.5 nH. Based on the above-mentioned analysis, the causes and negative effects of the typical switching oscillations are summarized in Table 2.1.

Table 2.1: Causes and Negative Effects of Switching Oscillations

Oscillation type	Cause of oscillation	WBG devices	Negative effect
False turn-on and false triggering oscillation	1)The high dv/dt generates a displacement current in the Miller capacitor, which may cause high gate-source voltage; 2) The high di/dt produces a negative voltage on the CSI.	SiC and GaN based devices	Voltage and current overshoots; shoot-through; EMI; additional power loss; device damage.
Parasitic ringing	The power loop parasitic inductor of the circuit resonates with the parasitic capacitor of the device	SiC and GaN based devices	
Sustained oscillation	Unique reverse conduction characteristics are formed by the physical mechanism of GaN devices	GaN based devices	

III. Suppression Method Of Switching Oscillations

Since the switching oscillations have many negative effects, it is necessary to use some effective methods to suppress them. From the cause analysis of the switching oscillations in Section II, it can be seen that the switching oscillations are mainly caused by the high dv/dt and di/dt, the resonance between the parasitic capacitance and the parasitic inductance. Accordingly, reducing the parasitic inductance of the circuit, controlling dv/dt and di/dt, and increasing damping are possible ways. Therefore, device selection and PCB layout to reduce parasitic inductance, gate driver design to control dv/dt and di/dt, and adding ferrite beads or RC snubbers to increase damping are currently the main suppression methods. Although these methods are well known, different design techniques are critical to suppress them well, and the performance of the converter can be improved in the end.

Different techniques are:

- Device Selection and PCB Layout
- Gate Driver Design
- Adding Ferrite Beads or RC Snubbers

Table 3.1: Comparison among different Oscillation Suppression Methods

Suppression method	classification	Description	Advantage	Disadvantage	Reference
Device selection	N/A	• Select devices with small package inductance. • Kelvin connection to eliminate CSI. • The TO-263 package inductance is 32% lower than the TO-247 package inductance, which results in a 29% reduction in total per-cycle switching losses(600V/20A)	• Simple and easy to implement.	• Limited oscillation	[22],[23]
PCB layout	N/A	• PCB layout to minimize power and driver loop inductance; • The optimal double-sided layout based on the phase-leg circuit can reduce the power loop inductance to nH, which is only 25% of state-of-art layout and only 8% of the voltage overshoot.	• No additional auxiliary circuit required. • Certain oscillation suppression effect.	• Complex PCB layout design. • Difficult to implement	[24]-[26]
External gate resistor	N/A	• External gate resistor to reduce dv/dt and di/dt. • The overshoot voltage and the oscillation duration are reduced by 4% and 13.1% respectively.	• Simple and easy to implement.	• Increased large switching losses; • Limited oscillation suppression effect.	[27]-[29]
Active gate driver	The false turn-on(crosstalk) suppression	• Control gate voltage, gate current, and gate loop impedance through the gate auxiliary circuit; • Effectively reduce crosstalk, overshoot and false triggering oscillation by controlling dv/dt and di/dt.	• Achieve fast switching speed; • Reduce switching losses; • Certain oscillation suppression effect	• Make the design of the gate driver circuit more complicated; • Cause extra cost for external circuits.	[30], [31]
	False triggering oscillation suppression				[32]
	Drain-source voltage ringing suppression				[33]-[34]
Ferrite beads	N/A	• Increase high-frequency damping to suppress voltage and current overshoots; • The overshoot voltage and the oscillation duration are reduced by 3.8% and 78.5% respectively	• Simple and easy to implement.	• Limited oscillation suppression effect • Slightly increased conduction losses.	[35], [36]
RC snubbers	The second-order design	• Simplify the circuit into a second-order model and obtain the RC values by equation (8) and (9); • The overshoot voltage and the oscillation duration are	• Simple and easy to implement.	• Limited oscillation suppression effect	[37],[38]

		reduced by 40% and 65% respectively.		• Slightly increased switching losses; • Suitable for second order circuits	
	The third-order design	• Consider or distinguish more parasitic parameters, use root locus method to get RC values; • When the breakaway point ϒ of the characteristic equation D(s) = 0 satisfies D(ϒ) =0 and dD(ϒ)/ds=0, the oscillation can be sufficiently suppressed.	• Simple and easy to implement. • Good oscillation suppression effect.	• Medium complex design; • Slightly increased switching losses; • Suitable for no more than third-order circuits.	[39]
	The high-order design	• Obtain the root locus of the characteristic equation of the higher-order equation; • Make the damping ratio of all characteristic roots as large as possible	• Simple and easy to implement • Good oscillation suppression effect. • Suitable for high-order circuits.	• Slightly increased switching losses; • Complex design	[40]

According to the above-mentioned analysis, the advantages and disadvantages of different oscillation suppression methods are summarized in Table 3.1. It can be seen that different design methods have different effects on switching oscillation suppression. Selecting the devices with small package inductance or Kelvin connection, the good PCB layout to reduce power and driver loop inductance, the effective active gate driver or proper RC snubber may be a good choice to suppress switching oscillations.

IV. Conclusion

This paper reviews the switching oscillations of WBG devices, which mainly include the types of switching oscillations, the causes and negative effects of various switching oscillations, the effects of various parameters of switching oscillations, and the main suppression methods. Further, the design challenges and future research trends are summarized. The following observations and conclusions can be obtained from this article.

1) WBG devices can be used in high-frequency circuits to improve the system's power density due to their fast switching speed. However, their low parasitic capacitances and threshold voltage make them more susceptible to switching oscillations.

2) The causes of different types of switching oscillations are not the same. In addition, the negative effects of switching oscillations, including overshoot, shoot-through, EMI, and additional power loss, are critical to the performance of the power converter.

3) Switching oscillations can be mitigated or suppressed by selecting the proper device and optimizing the PCB layout to reduce loop inductance, reducing dv/dt or di/dt, using active gate driver, adding ferrite beads or RC snubber circuits.

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