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TRANSMISSION GATE -BASED 8T SRAM CELL FOR BIO MEDICAL APPLICATIONS

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Abstract: **- In this project, a transmission gate based SRAM cell is designed for biomedical applications by eliminating the use of peripheral circuitry during the read operation. There is an immense necessity of several kB of embedded memory for biomedical systems which typically operate in the sub-threshold domain with perfect efficiency. SRAMs dominate the total power consumption and the overall silicon area, as 70% of the die has been occupied by them. This topology offers smaller area, reduced delay, low power consumption and improved data stability in the read operation. The SRAM cell is implemented in 45nm CMOS technology operated at 0.45 V.**

Index Terms **– SRAM, Bio medical applications, Low power etc.**

1. INTRODUCTION

Static random-access memory is a type of semiconductor memory that uses bistable latching circuitry to store each bit. The term static differentiates it from dynamic RAM which must be periodically refreshed. SRAM exhibits data remembrance, but is still volatile in conventional sense, that data is eventually lost when memory is not powered. The continuous scaling down of bulk CMOS creates major issues due to its base material .The primary obstacles to the scaling of bulk CMOS to 32nmgatelengths include short channel effects ,Sub-threshold leakage ,gate-dielectric leakage and device to device variations. Due to sudden increase in threshold voltage i.e. Vt oscillation produced by overall and general process variations occur in ultra-short channel devices, 6T SRAM cell and their modifications cannot be operated at advance scaling of supply voltages without functional and parametric failure causes yield loss. The design of standard 6T SRAM cell undergoes a lot of problem on write delay [1].The design of Low power 6T SRAM cell could decrease the write power and access delay [2] but could not improve their stability. In deep submicron ranges, none of the earlier works has studied about the improvement of variability in SRAM cell at the schematic level .Therefore, we design a vigorous and variation accepting SRAM cell design technique capable of gripping Vt shift due to random dopant fluctuation(RDF), and variation in further device and their process parameters (such as length, width, sub-wavelength-lithography ,oxide thickness, etching, and annealing) and still be able to perform expected functions need to be investigated. To fulfill this drawback we propose a transmission gate 8T SRAM cell (TG8T) and compare their performance with standard 6T SRAM cell at cadence virtuoso tool at 45nm technology.

The Moore's law of scaling has been the main observation behind the semiconductor industry. Scaling has straightforwardly or in a roundabout way been the underlying driver of the colossal abilities of today's ICs and their universal use in about all cutting edge electronic frameworks. In power consumption, reduction makes a device more reliable. In recent years, the demand of low power devices has been increased and due to scaling of CMOS technology. Due to the scaling, the important advantage is the size of the chip decreases and the no. of transistors increases in a system of chip (SOC). Power consumption is the most attentive parameter to design low power devices because it plays an important role in increasing the total power consumption of the devices. As the procedure technology keeps on scaling, the soundness of embedded Static Random Access Memories (SRAMs) is a developing worry in the configuration and test group. A low power design has now become a most important issue in VLSI design, basically for high speed and high performance systems. A low power and high-performance of SRAMs cell requires an optimization of the technology and the circuits. At the technology level, technology optimization is the final tool that a designer can use to produce low power and a high-performance of SRAMs. This paper presents a novel design technique for low power CMOS 8T SRAM circuits by using transmission gates for high speed VLSI design. In this paper , the proposed TG 8T SRAM cell decreases the voltage swing, which is define as a difference between of maximum output voltage and minimum output

voltage . however number of transistors are increased and area also in comparsion to conventional SRAM cell but a low power dissipation at higher frequency can easily overcome this drawback.

The organizational framework of this study divides the research work in the different sections. The Literature survey is presented in section 2. Further, in section 3 shown Existing System is discussed and in section 4 shown in proposed system, In section 5 Experimental Results work is shown. Conclusion and future work are presented by last sections 6.

2. LITERATURE SURVEY

The goal of this paper is to analyze the SNM (Static Noise Margin) of 6T SRAM cell during read operation with increase in transistor using 180nm technology. Using this paper, we can overcome the power consumption due to additional transistor. In this paper, we use 6T SRAM in 45nm CMOS technology to provide interface with CPU and to replace DRAMs in system. We can overcome the large fraction of total power in SRAM cell. Here, we can provide low leakage power using improved self controlled voltage level circuits in 9T SRAM which results in total average power. In the design of low power 9T SRAM cell, we can consume less dynamic power and high read stability. when compared to other technology, there is a decrease in power consumption and stability increases. In this work, adiabatic technique is used for reduction of average power dissipation. Here we can reduce 87% of power during write operation, 66% of power during hold operation and 85% of power in read operation.

3. EXISTING SYSTEM

6T SRAM Cell

A SRAM cell should perform read, write and hold operations as long as the power is applied. An ordinary flip-flop could accomplish this requirement, but the size is quite large. This is a good trade-off in large RAM arrays where the memory cells dominate the area. This smaller cell size offers shorter wires and therefore it results in lower dynamic power consumption. The 6T SRAM cell shown in figure 1,it contains a pair of weak cross-coupled inverters holding the state and a pair of access transistors to read or write the state. The 6T SRAM cell achieves its compactness for reading and writing the cell. The positive feedback corrects disturbances caused by leakage or noise.

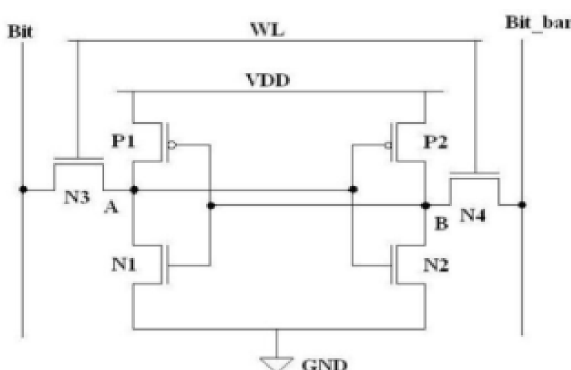

Fig. 1: 6T SRAM CELL

Operation

Standby Mode (the circuit is idle):

The word line will be 0 in the standby mode, so the transistors N3 and N4 will be passed to connect 6T cell, which means that the cell cannot be accessed. The cross coupled inverters N1-N2 will continue to feedback as long as they are connected to the supply, data and hold in the latch.

***Read Mode (the data has been requested)*:**

The word line will be 1 in read mode which enables both the transistors N1 and N2.The values stored in nodes a and b are transferred to the bit lines. If we give 1 at node a, the bit line bar will discharge through driver transistor N1 and the bit line will pull up through the load transistor P1 towards VDD.

Write Mode (updating the contents):

In write mode, if we wish to write 0 or 1, the bit line should be lowered to 0v, bit bar is raised to VDD and cell is selected by raising the word line to VDD. If we wish to write 0 at node a, N3 operates in saturation where its source voltage is 1. Drain terminal of starting at 1 which is pulled down by N3 because access transistor N3 is stronger than N1. Now N2 turns on and P1 turns off, thus new value has been written which forces bit line lowered to 0V ad bit bar to V.

8T SRAM Cell

The main motive behind the forceful device scaling is to achieve enriched performance and increased integration. These improvements led to the cost of increased sensitivity to standby leakage, delay mostly in area constrained circuit such as SRAM that requires minimum geometry devices. In this work, an effort has to be done to solve these problems in conventional 6T SRAM cell by considering minimum area consequences and achieve its fully differential architecture.

These system uses differential operation and does not possess as much architectural changes except adding a PMOS in parallel with each access NMOS in conventional 6T SRAM cell shown by M5 and M6, by this we make it TG8T SRAM cell shown in figure 2. An additional control WLB is required for switching the access PMOS. The WLB and WL (word line) are non-overlapping opposite signals. Therefore, during read and write operation, to retrieve the data from cell all access FETs are swapped simultaneously. But, during hold mode all access FETs remain shot off.

This fragment shows the proposed architecture of TG8T SRAM which is resembles to the standard 6T SRAM cell.

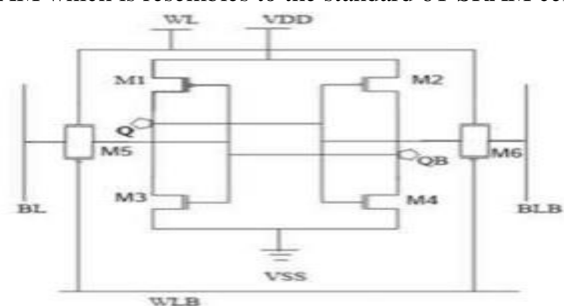

Fig. 2: 8T SRAM CELL

Operation

Read Operation:

In read operation, Bit lines are pre-charged to supply voltage before the operations starts. At first, the word line(WL) is enabled and connecting the internal nodes of the SRAM bit cell to bit lines. N-mos transistors pull down the bit line voltage at the'0'storage node and the difference between two bit line voltages will be detected by sense amplifier. When the word line(WL) is high, one of the bit line voltages is pulled down through transistors M2 and M6 or M1andM4.Th transistors M2andM6 forms voltage divider, because of current flowing through M2,the potential at node is no longer at '0'V.To avoid destructive read, it should not go beyond switching threshold inverter(INVI).

Write Operation:

The pre charged logic is kept low during write operation. If we wish to store logic '1',bitline is charged to and bit bar line is discharged to ground. When the word line is activated, the data on bit and bit bar lines are written into the output nodes of the cell. During updating of the content, one should remember that the voltage where logic '1' is stored must be less than the threshold voltage of the driver transistors of other inverter. The bit line voltage is pulled down by the n MOS transistor at the '0' storage node and the difference between two bit line voltages will be detected by sense amplifier.

dd

4. PROPOSED SYSTEM

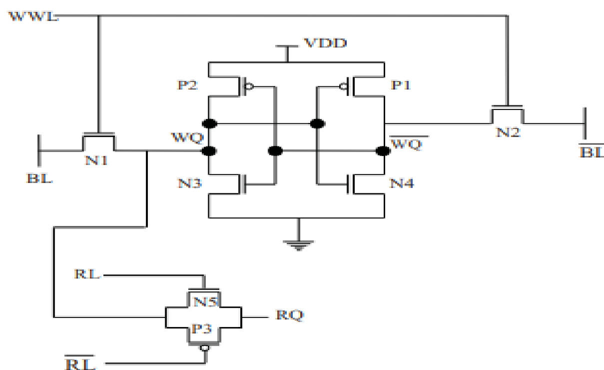

Fig. 3: Proposed SRAM Cell

The proposed design chiefly concentrates on the read operation, which in the existing designs exclusively instillsontheperipheralcircuits.TheWriteoperationishomogeneoustotheConventionalandtheotherSRAMcells. The Write functionality is controlled by the Word Line (WWL). The content which we incline to write is given to the Bit Lines BL and BL Bar. Now, the enabled Word Line, making the access transistors active, allows the data of the Bit Lines to intrude into the memory cell. The intruded data will thus be cached into the two storage nodes WQ and WQBar.

The read operation is controlled by the two complementary Read Lines RL and RL Bar and must be enabled before starting the read process. The read port is separately designed by employing a Transmission gate. Here, the main intention is to read the data that is present in the storage node WQ. Therefore, the data that is cached in the storage node WQ is conferred to the Transmission gateN5 and P3 which are in ON state as the Read Lines are enabled priorly. Now, the Transmission gate passes the data and confers it to the Read node RQ. The data stored in the node WQ will appear in the node RQ through N5 and P3transistors. Thus, the content of the cell can be directly.

Read with the help of a Transmission gate instead of using complex peripheral circuits. The generalized read energy equation can be given as follows

$$E_{rd} = C_{RBL}\left\{\Delta V^2_{prech} + \Delta V^2_{disch}\right\}$$
$$= C_{RBL}\left\{\left(V_{dd} - V_{RBL}\right)^2 + \left(V_{dd} - V^{1}_{RBL}\right)^2\right\}$$

Where VRBL represents the voltage of read bitlineandV^{1}representsthevoltageofreadbitlineafterthecompletionofreadoperation.Butthisdesignasofnotusingthesenseamplifierandprechargecircuit,the read energy can be reduced.

This design reduces the chip area of about 15% as the number of transistors are reduced that are used for designingtheperipheralcircuits.Thereductioninthenumberoftransistorsused,inturn reduces the total power consumption. This is because the leakage power relys on the number of transistors used in a design as explained below.

P total=Pdyn +PLeak

Pdyn=CeV²f

PLeak=VddNtrKdIs

Where Ntr represents the No.of transistors, Kda device specific constant and Is the normalized static current for each transistor.

The decrement in the transistor count results in the reduction of the leakage power of those transistors there by reducing the overall power dissipation of the circuit. Since the sense amplifier and the precharge circuits used for the read functionality in the existing designs are eliminated in the proposed design, the delay of generating the output i.e reading the data present in the storage nodes can also be reduced. This is because of undergoing the read operation directly with the help of transmission gate.

This approach also maintains the stability since the read and writes ports are separated. The averaging consequence of the two parallely placed transistors of a transmission gate helps in nullifying the read current producing better stability than that of using as single NMOS for the read current to pass by. The cell failure probability can be predicted by assuming the Gaussian distribution for Threshold voltage of a transistor [26].It is calculated as,

Pfail=Prob[SNM<Vth]

Where,Vth=kT/q

kT=26 mVat300K

The comparison of the proposed design is done for the read operation itself since the design is intended to perform the read process only. Since the Write and Hold operations are similar to the existing designs, the performance results are also homogeneous. Therefore the result discussed here considers the read state. Generally, the performance analysis of SRAMs is based on certain parameters such as Power Consumption,

Delay, and Stability and Area occupancy of the cell. The performance comparison of the Conventional 6T(C6T), other existing techniques (8T, 10T-E1, 10T-E2 and10T-E3)and the Proposed technique (8T-P) is done in CMOS 45-nm Technology at 0.45V at room temperature.

5. SIMULATION RESULTS

All the simulations are performed on Tanner EDA Tool.. The main focus of this work is to meet all challenges faces in designing of memory circuit at Nano scale technology, where deviations arisesdue to process and environmental parameters such as operating voltage and temperature. The basic cause of variations is scaling. The leakage current of TG8T SRAM cell is improved as compared to conventional 6T SRAM cell. The simulation results are shown below figure 4 and figure 5.

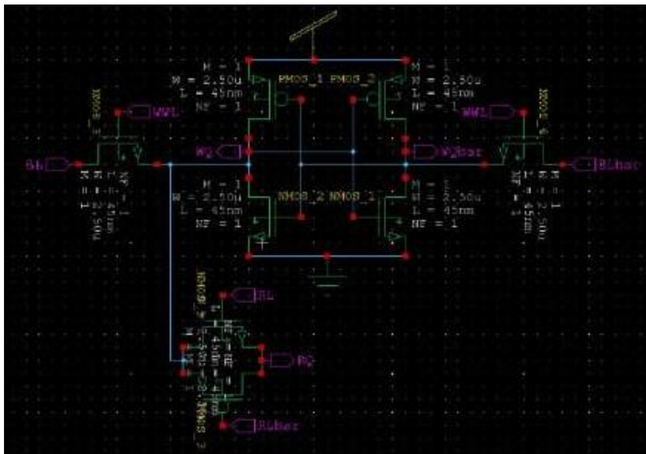

Fig. 4: Designed 8T SRAM CELL in Tanner EDA Tool

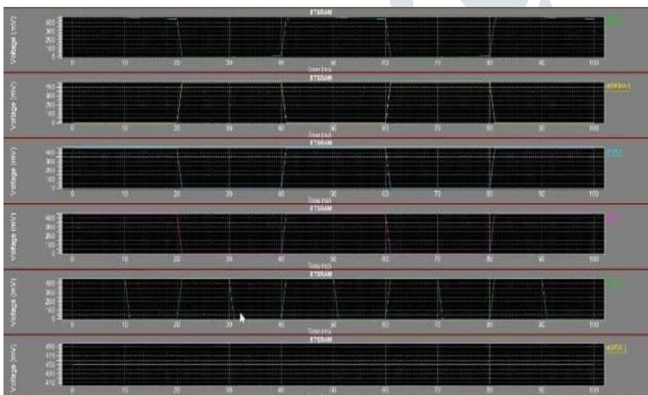

Fig. 5: Output waveform of 8T SRAM CELL

6. CONCLUSION

As it is noticed that the proposed design of SRAM cell contributes to major reduction in power dissipation, future research to develop a more power efficient and area minimized SRAM architecture and memory designing. In future, the operating voltage should be minimized for technology scaling system. Also speed and delay consideration should be developed for the system so that both power and speed is optimized. By developing these research works, the proposed system can be taken to a better efficiency level considering power, speed and area. As it is noticed that the proposed design of SRAM cell contributes to major reduction in power dissipation, future research to develop a more power efficient and area mini-mized SRAM architecture and memory designing. In future, the operating voltage should be minimized for technology

Future Scope

In future Further optimization of the layout design can help to reduce the area overhead and improve the performance of the 8T SRAM cell. This could involve exploring different transistor sizing, positioning, and routing techniques to minimize parasitic capacitance and maximize signal integrity.

ACKNOWLEGMENT

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