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DESIGN OF APPROXIMATE RADIX 256 BOOTH ENCODING FOR DIGITAL SIGNAL PROCESSING

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Abstract **-** In this project, a novel low power 16x16 bit multiplier based on the approximate Radix 256 booth encoder has been proposed. The proposed approximate radix-256 Booth encoding with partial encoding approach uses appropriately selected partial product pairs to resolve hard multiple issue and obtaina small error distance. The multiplier design based on the proposed Booth encodingexhibits better performance- accuracy tradeoff. A partial encoding approach is usedto produce partial product pairs, which can be obtained easily by simple shifting andcomplementing operations. The exact encoding values are thus replaced by the sumof each corresponding partial product pair. The evaluation on DSP applications further validates its applicability for error-tolerant computing. The performance of the proposed work is evaluated in terms of power, delay and Power delay Product. The parametric analysis of the proposed work is also carried out to assess the impactof various parameters. The total work has been carried out using different CMOS technology 45nm using Xilinx Vivado tools.

Index Terms: Approximate computing, radix-256, Booth encoding, energyefficient.

I. INTRODUCTION

The current trend in computer technology is towards increased compactness, speed, and affordability. The achievement of increased chip density and operation frequency can be attributed to the advancements in VLSI technology. The escalation in power consumption has led to a proximity to the constraints of both dependability and expense. In addition, as the system is reduced to the Nano scale range, there are design resilience challenges that emerge, such as signal integrity, soft errors, and process variability. Furthermore, issues related to power consumption and durability tend to develop gradually. The aforementioned circumstance has resulted in a perplexing situation in the development of information systems, which is anticipated to hinder forthcoming progress. According to computer system experts who are pioneers in the field, it is imperative to consider power consumption and system robustness throughout every stage of the design process. The careful consideration of logic types is of utmost importance in circuit design as it has a direct influence on power consumption, efficacy, and resilience. The current state of Static CMOS logic is deemed insufficient to meet the forthcoming computational requirements. The two primary circuit architectures in CMOS technology are static logic and dynamic logic. The static complementary metal-oxide-semiconductor (CMOS) technology is known for its high energy efficiency and robustness. However, it is observed to be significantly slow in critical and large designs. Conversely, the Domino logic methodology exhibits high speed performance, however, it consumes a significant amount of power and lacks durability. Consequently, there is a need for an improved digital logic methodology and design that is characterized by energy efficiency, high speed, and noise immunity. The Approximate Computing technique was selected for this study due to its low power consumption and versatility in implementing various functionalities. This led us to suggest an improved multiplier that functions without augmenting manufacturing intricacy and can be executed with reduced power consumption. The present study introduces an Approximate multiplier that utilizes radix-256 booth encoding. In comparison to other designs, a significant amount of energy is conserved. This thesis conducts a peer analysis of approximate booth multipliers and subsequently compares them to analogous circuits developed using alternative logic methodologies.

II.EXISTING SYSTEM

In the existing systems, high radix Booth encodings provide significant decrease on the number of partial products in the multiplication. However, due to the generation on hard multiples, additional delay and power are incurred, which in turn hampers the use of high radix Booth encodings. As multiplier is the most basic block in various applications in which the performance of the design is determined. In various multipliers using booth algorithm which are designed with half adders and full adders are utilized and the speed of the circuit been reduced and area of the circuits are increased which effects the performance of the designs. A multiplier has two operands: a multiplicand as well as a multiplier which produces the result. In the initial step, the multiplier and multiplicand have been bit-by-bit multiplied to obtain the intermediate result. This is the most crucial step since it is the most complex and affects the rate at which the total multiplier combines the partial products to get the outcome. A half-adder would be the easiest way to do multiplication. M cycles are required to operate an N-bit adder for inputs that appear to be M & N bits larger. M partial products are added together using the shift-add multiplication technique. Every partial product is calculated by multiplying a multiplier bit by a multiplier bit and then shifting the result based on the multiplier bit's position.

Disadvantages:1. Delay is maximum and hardware complexity of the circuit is more.

2.Area of the design and computational time is high which leads to higher power consumption.

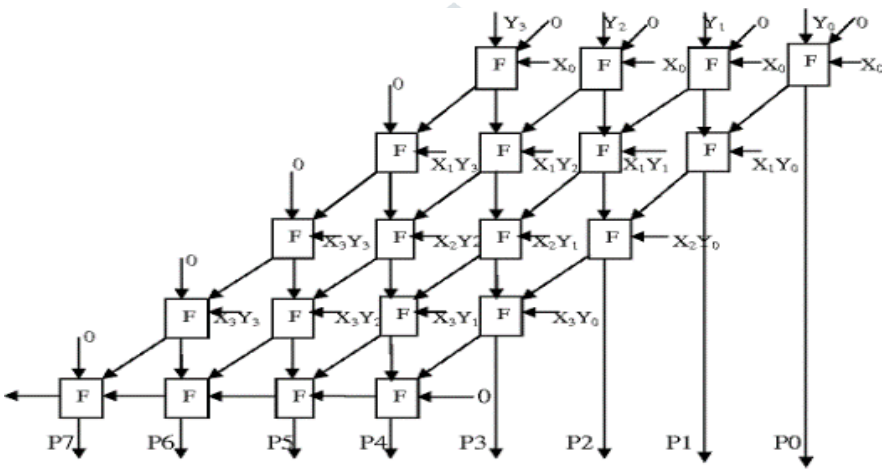

Figure.1: Conventional array multiplier with CSA

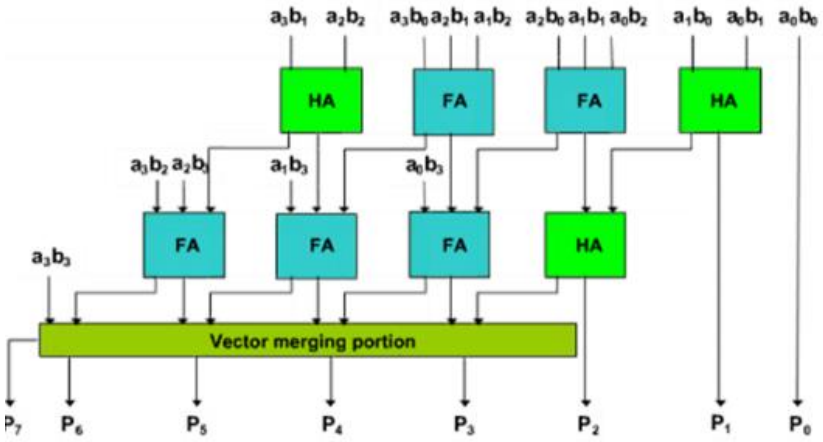

Figure.2: 4x4 Wallace tree multiplication

III.PROPOSED METHOD

In the proposed method, to maintain a reasonable output quality, hybrid Booth encodings are employed, where the proposed 256 Booth encoding is used for the less significant bits (LSB) of the multiplier; while for the more significant bits (MSB), radix-4 Booth encoding is employed. The n-bit multiplier is partitioned into two: 8 LSBs and a supplemented '0' are used for 256 Booth encoding, while the rest of the bits are used for radix-4 Booth encoding. In the partial products matrix generated from the hybrid Booth

encodings, a simplified sign extension method is utilized. For an n-bit multiplier, there are (n−8)/2 and two partial products generated from radix-4 and AR256 Booth encodings, respectively. The correction bits for both are located at the corresponding LSB positions

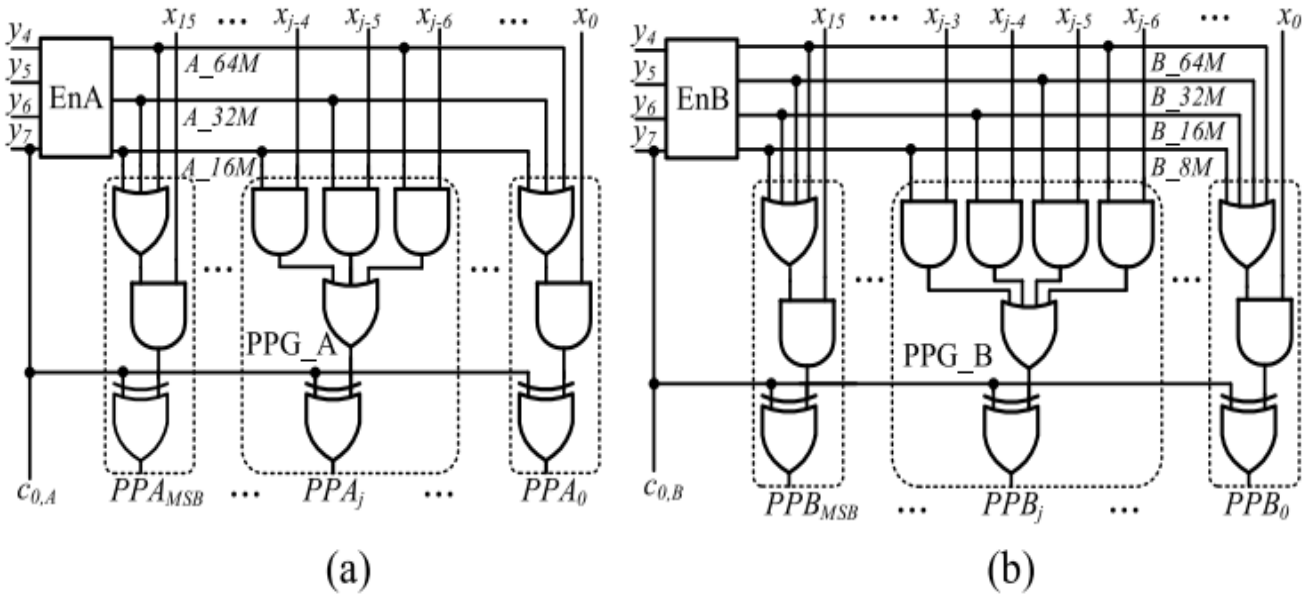

Figure.3: The partial product generation of (a) PPA and (b) PPB with proposed approximate radix-256 Booth encoding

$y_{8k+7}y_{8k+6}$ $y_{8k+5}y_{8k+4}$	Input Patterns	d_k	c_k	PPA	PPB	Select Signals(A,B)	P_k	MAE	$y_{8k+7}y_{8k+6}$ $y_{8k+5}y_{8k+4}$	Input Patterns	d_k	c_k	PPA	PPB	Select Signals(A,B)	P_k	MAE
0000	[0, 31]	[0, 16]	0	0	8X	0,8M	8X	8X	1000	[-255, -224]	[-128, -112]	1	-64X	-64X	64M,64M	-128X	16X
0001	[32, 63]	[16, 32]	0	16X	8X	16M, 8M	24X	8X	1001	[-223, -192]	[-112, -96]	1	-64X	-32X	64M, 32M	-96X	16X
0010	[64, 95]	[32, 48]	0	32X	8X	32M,8M	40X	8X	1010	[-191, -160]	[-96, -80]	1	-64X	-16X	64M,16M	-80X	16X
0011	[96, 127]	[48, 64]	0	32X	16X	32M,16M	48X	16X	1011	[-159, -128]	[-80, -64]	1	-64X	-8X	64M,8M	-72X	8X
0100	[128, 159]	[64, 80]	0	64X	8X	64M,8M	72X	8X	1100	[-127, -96]	[-64, -48]	1	-32X	-16X	32M,16M	-48X	16X
0101	[160, 191]	[80, 96]	0	64X	16X	64M,16M	80X	16X	1101	[-95, -64]	[-48, -32]	1	-32X	-8X	32M,8M	-40X	8X
0110	[192, 223]	[96,112]	0	64X	32X	64M,32M	96X	16X	1110	[-63, -32]	[-32, -16]	1	-16X	-8X	16M,8M	-24X	8X
0111	[224, 255]	[112, 128]	0	64X	64X	64M,64M	128X	16X	1111	[-31, -0]	[-16, 0]	1	-0	-8X	0,8M	-8X	8X

TABLE.1: APPROXIMATE RADIX-256 ENCODING RULE

Table.1 elucidates the encoding rules. As shown, y8k+7y8k+6y8k+5y8k+4 are the most significant 4 bits of every 9-bit set, which represents the input pattern. dk is a signed digit which represents the exact encoding value. Pk indicates the approximate partial product. ck is the sign correction bit which is used to distinguish positive and negative encoding results. The select signal pair (A, B) is used to select the multiples from the corresponding multiplicand for the generation of the final approximate partial product. To maintain a reasonable output quality, hybrid Booth encodings are employed, where the proposed AR256 Booth encoding is used for the less significant bits (LSB) of the multiplier; while for the more significant bits (MSB), radix-4 Booth encoding is employed. Fig. 1 indicates the partitioning of the multiplier bits with hybrid Booth encodings and the corresponding partial product matrix. The n-bit multiplier is partitioned into two: 8 LSBs and a supplemented '0' are used for AR256 Booth encoding, while the rest of the bits are used for radix-4 Booth encoding. In the partial products matrix generated from the hybrid Booth encodings, a simplified sign extension method is utilized. For an n-bit multiplier, there are (n−8)/2 and two partial products generated from radix-4 and AR256 Booth encodings, respectively. The partial product bits generated from these two encoding approaches are differentiated with symbols of triangles and circles. The correction bits for both are located at the corresponding LSB positions. According to Table III, two separate encoders, Encoder A and Encoder, are required to generate the partial product pair, PPA and PPB, respectively. Each of them is encoded in parallel to generate a set of select signals. For Encoder A, the signals for selection are from the set {16M, 32M, 64M}

Advantages of Project:

- Power, Delay, PDP are optimized
- Hardware complexity of the circuit reduces.

Applications:

- MAC unit

- DSP applications
- Digital image processing

IV.RESULTS DISCUSSION

The various 8 X 8 multipliers outlined above have been synthesized and simulated using an FPGA board utilizing the Xilinx Spartan 7 XC7S15-1FTGB196C architecture. The inputs of the multiplier are connected to the input switches of the FPGA and outputs of the multiplier are connected to the LEDs present on the FPGA. For the implementation of the existing and proposed multipliers on to FPGA board, Xilinx ISE is used. By varying the switches on the FPGA, the corresponding LEDs are verified. However, this technique raises the delay time greater than the existing methods. In this case, simulation is performed for multipliers with an 8-bit width. A multiplication using the proposed multiplier with inputs X and Y as 16bits each is depicted in Figure 5. The output result of the multiplication process is represented by P.

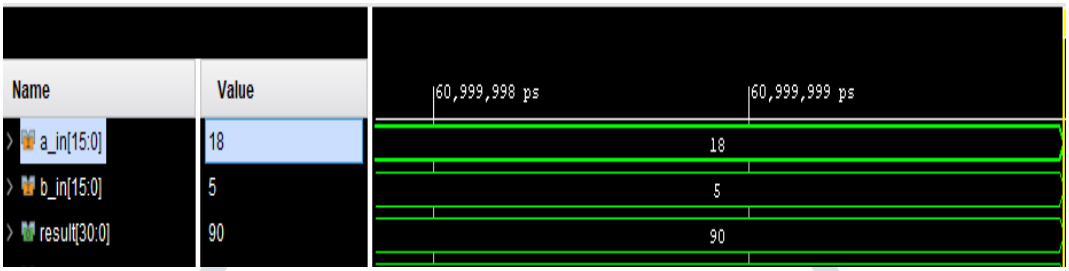

Figure.4: 8X8 Wallace Tree Multiplier

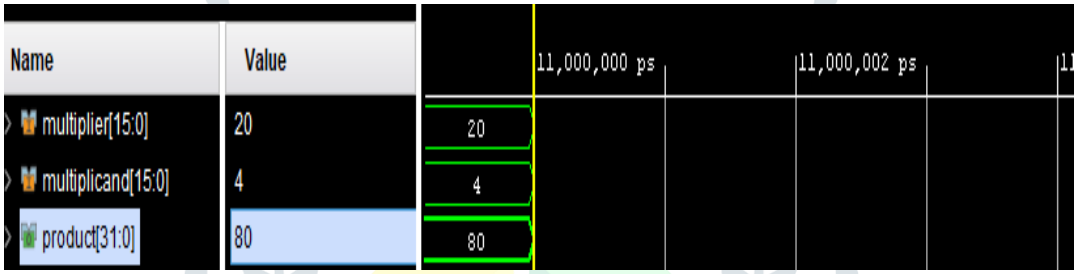

Figure.5: 16x16 proposed Radix-256 Multiplier

Parameter	Existing Wallace treeMultplier	Proposed Booth Multiplier
Area(Units)	877	489
Power(mW)	707	150

Table.2: Performance analysis of various multipliers

V. CONCLUSION

With the rising demand for huge multiplier in a wide range of applications, several designs have indeed been investigated and examined in order to build an efficient design. The suggested Radix-256 Multiplier employing Radix-4 Booth Algorithm has indeed been developed using Xilinx Vivado software. This work examines radix-4 booth algorithm and Radix 256 Booth multiplier. Design failures related to structural irregularities may be reduced by employing this Vedic multiplier. Because this multiplier does have a regular layout, the processing capabilities of the multiplier may be readily enhanced by increasing the data input and output data bus. Because the proposed multiplier's architecture is periodical, it is simple to build in a silicon wafer. Amongst some of the multipliers examined, the proposed multiplier is combined with radix-4 booth encoding to generate a modified radix -256 multiplier that has less delay propagation and operates at a faster speed. This approach takes relatively little time to get a 32-bit output. For efficient implementation of FIR filters and signal processing applications, proposed multipliers are utilized. When

compared with traditional designs, the look up tables occupied by a suggested multiplier is minimized by at least 60%, and also the power has minimised by at least 25%.

Furthermore, when the speed of technological advancement quickens, new inventive solutions and design elements may be created to fulfil technological scalability standards. Furthermore, as CMOS technology progresses, researchers may concentrate on CMOS IC design methodologies with a high degree of assurance and power efficiency for wireless healthcare and medical application sectors. There is space to create building techniques at both the circuit block and system levels throughout the whole foundation of technical breakthroughs. Approaches for designing ultra-low-power CMOS circuits for the full network impact of wireless health and medical care that are strategically positioned at low-technological nodes.

REFERENCES:

1.J. M Rabaey, A. Chandrakasan, B, Nikolic, Digital Integrated Circuits: A Design Perspective, Upper saddle rive, NJ: 2e Prentice-Hall, 2002.
2. S. M. Kang, Y. Leblebici, CMOS Digital Integrated Circuits: Analysis & Design, TATA McGraw- Hill Publication, 3e, 2003.
3. N. Weste, K. Eshraghian, Principles of CMOS VLSI Design, A systems perspective, Addison Wesley MA, 1988.
4. J. P. Uyemura, CMOS logic circuit design, Kluwer Academic, 2002.
5. K.S. Yeo, K. Roy, Low- Voltage, Low-Power VLSI Subsystems, McGraw Hill Professional, 2005.
6. K. Roy, S. Prasad, Low-Power CMOS VLSI Circuit design, Willey Interscience Publication, 2000.
7. K. K. Kim, Y. -B. Kim, M. Choi, N. Park, "Leakage minimization technique for nanoscale CMOS VLSI based on macro-cell modelling," in IEEE Design &Test of Computers, Dec. 13, 2006.
8. I. -C. Wey, Y.-G. Chen, A.-Y. Wu, "Design and Analysis of Isolated Noise Tolerant (INT) Technique in Dynamic CMOS Circuits," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 16, no. 12, pp. pp.1708-1712, Dec. 2008.
9. P. Meher, K. K. Mahapatra, "Ultra low-power and noise tolerant CMOS dynamic circuit technique," in IEEE Region 10 Conference TENCON 2011, pp.1175-1179, Bali, 21-24 Nov. 2011.
10. R. G. Dreslinski, M. Wieckowski, D. Blaauw, D. Sylvester, and T. Mudge, “Nearthreshold Computing: Reclaiming Moore’s Law through Energy Efficient Integrated Circuits,” Proceedings of the IEEE, vol. 98, no. 2, pp. 253–266, 2010.