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Design and Performance Analysis of Low Power CECRL and CPFAL Diverse Full Adder Circuits

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***Abstract*—Designing low-power, energy-efficient circuits using DG FINFET technology presents a formidable obstacle. This study describes internal logic structure and circuit operation for creating different Full adder cells utilizing DG FINFET and CMOS devices. A CMOS & DG FINFET-based diversified full adder (DFA) is constructed at transistor level. The cadence tool is used to do simulations in 90nm technology, and results are contrasted with those from a performance analysis of these DFA in 90nm DGFINFET technology. In comparison to DFA, DFA using DG FINFET methods achieves low leakage and current power for enhanced mobility & transistor scaling. This work evaluates and contrasts the power dissipation of standard CPFAL-based, CMOS, and CECRL-based CMOS circuits. The results are applied to redesign a circuit in which input power is assumed to come from a sinusoidal source of 0.7 V. In comparison with the conventional diverse full adder (DFA) circuit, the designed CECRL and CPFAL diverse full adder (DFA) circuit has lesser power dissipation and also for full adder conventional CMOS circuit with CECRL and PFAL based full adder respectively.**

***Keywords*—CMOS, Diverse Full Adder, DG FINFET, Leakage Power, Area, Cadence.**

I. INTRODUCTION

The development of mobile operating programs like those found on PDAs and personal computers, in addition to progression of shrinking technology, calls for a silicon area that is smaller, hardware that has better throughput, and power consumption that is lower [1][2][3]. Multi-gate transistors, like double-gate FinFETs, have a lower leakage current and smaller sub-threshold Swing (SS) than Standard CMOS transistors. [4]. Adders are crucial for performing subtraction, multiplication, addition, and division in complex arithmetic circuits. They serve as the system's core components and have a big impact on how well DSP-based processors handle tasks like filtering, video processing, and Fast Fourier Transform while using a minimum amount of power and energy [5][6]. Power may be saved by adjusting input voltage and running frequency. Yet, combined effects of delay and improved driving abilities [7][8][9]. A number of Full Adders are created earlier, every with its own set of advantages and disadvantages. Utilizing efficient structures, full adder attracts attention in carry skip, carry look ahead, carry choose, and conventional adders [10][11]. Moreover, the Full adder must be designed and improved to operate at ultra-low voltages. Digital CMOS circuits are widely utilized because of their excellent performance and versatility in a wide variety of computer, computing-intensive, and signal-analytical applications. As contrasted to other families of logic components, CMOS offers noise margins, higher logic levels, performance, and almost low static power consumption. As a result, it is family that is most commonly used. These circuits are in high demand, and their popularity is only expected to grow in the future as our need for quicker signal processing grows. When the number of transistors integrated into a device increases, computation speed increases. Unfortunately, this enhancement in performance is coupled with a rise in power and energy loss. [12]. More power and energy dissipation have downside of necessitating more costly packaging and cooling technologies for circuits, which reduces dependability and raises costs. As the need for faster calculations drives up clock frequency and on-chip integration, power and energy consumption of these high - performing circuits presents a dangerous design challenge that must be addressed [13]. Power dissipation of circuits is expected to increase to thousands of watts at clock rates of above 30 GHz, the pace at which high-end microprocessors use billions of transistors on a chip to reach TIPS (Tera Instructions per second). The performance of circuits is hampered by reliability issues including thermal stress, hot carrier, and electro migration brought on by such a high density of power dissipation. Especially for demand for low-power chips and low battery consumption chips, circuits with a greater power dissipation would consume more battery power. [14][15][16]. Portable digital devices, such as tablets, notebooks, laptops, etc., rely on batteries for power, therefore conserving energy is of paramount importance.

II. MPLEMENTATION AND OPERATION OF DIVERSE FULL ADDER CIRCUIT

A. 12T Diverse Full Adder Circuit

In the study, two novel designs of varied complete adders with transistor XOR gates are given. Simulations of the same were performed at various supply voltages with reverse biassing applied to NMOS transistors, and findings demonstrated advancements in adder power consumption. Thus, we selected and adopted 12-transistor diverse full adder described in that study, and we contrasted it to similar circuits. The 12-transistor diverse full adder circuit is depicted in Figure.1, and its transient response is depicted in Figure.2.

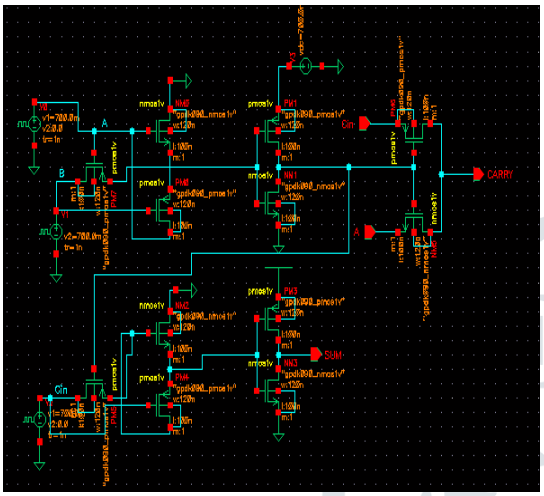

Fig. 1. Schematic of 12T Diverse Full Adder Circuit

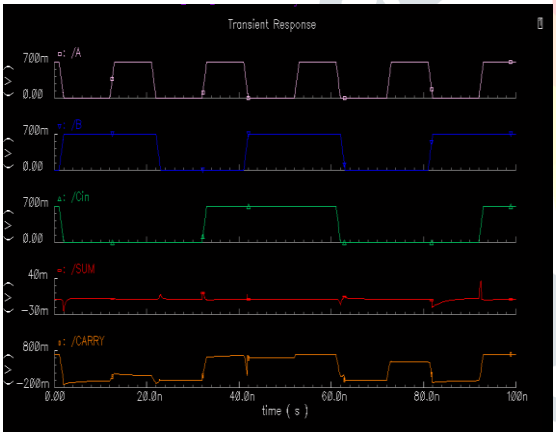

Fig. 2. Transient Response of 12T Diverse Full Adder Circuit

B. 10T Diverse Full Adder

We required a four-transistor XNOR circuit and a two-to-one multiplexer for development of different, ten-transistor complete adder circuits. Figure 3 depicts the circuit diagram of a 10T diverse Full Adder Circuit, whereas Figure 4 depicts output waveform.

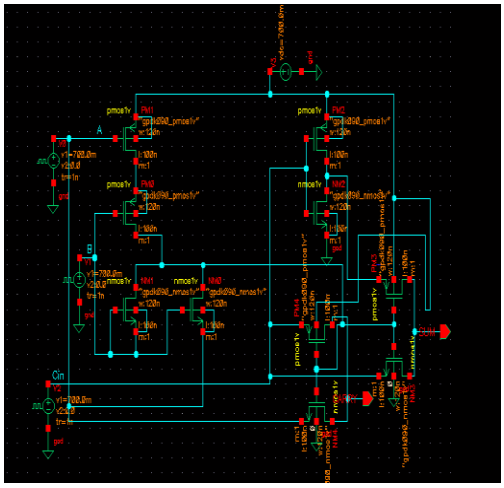

Fig. 3. Schematic of 10T Diverse Full Adder Circuit

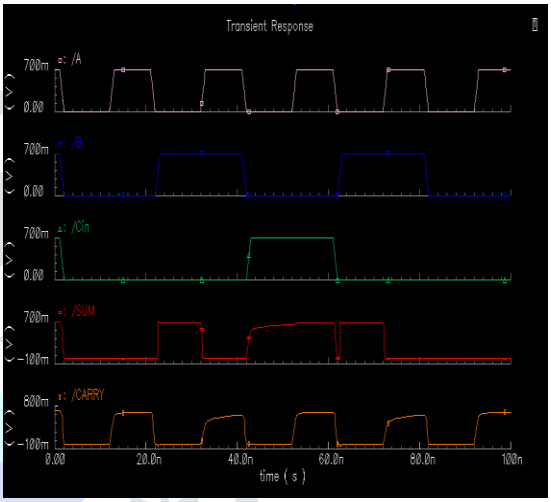

Fig. 4. Transient Response of 10T Diverse Full Adder

C. Diverse Full Adder Using DG FINFET Technique

Fin Field Effect Transistor is the abbreviation for this technology. Non-Planar Dual-Gate Transistor Field-Effect Transistors (FINFETs) is a key component of the high-density computing Silicon Architecture. Scientists at the University of California, Berkeley developed the FINFET to make better use of SiO2. The FET structure utilized in FINFET development is named from way it resembles a line of cutting edges when seen. The FINFET is characterized by its primary channel being encased in a thin silicon "fin," from whence it derives its name. The thickness of balance is what determines the length of a powerful channel in a gadget. On several Full Adder cells, a dual gate FINFET system is coupled. It is possible to make efficient use of self-determining control of back and front gates in DG FINFET in this context in order to enhance execution and minimize control consumption. It is possible to integrate parallel transistors using non-fundamental techniques by employing self-determining entry control. Two transistors are matched in parallel by connecting their source and drain connections. That DG (Double-Gate) FINFETS are able to control short-channel impacts and spilling current is evidenced by the fact that second gate in DG FINFETS is inserted in opposite direction of conventional gates. FINFET operations can be simplified into SG (short gate) mode, in which 2 transistor gates are attached; IG (independent gate) mode, in which self-deciding digital signals are utilized to drive 2 gadget gates; low power & ideal power mode, in which back gate is linked to a turnaround inclination voltage to minimize spillage control; and crossover mode, that employs a combination of SG & IG modes. The constant downscaling of bulk CMOS, as a result of its basic material, creates

crucial problems. Scaling mass CMOS to gate lengths of 45 nm causes a number of big problems, the most important of which are short channel effects, ideal current, gate dielectric leakage, and differences between devices. Still, FINFET-based designs give more control over short-channel impacts, less leakage, and a higher yield in 45nm, which helps more than scaling problems. Figure 5 depicts the schematic of DG FINFETs coupled to various Full Adders. Figure 6 depicts the output waveform of several Full Adders employing DG FINFET technique.

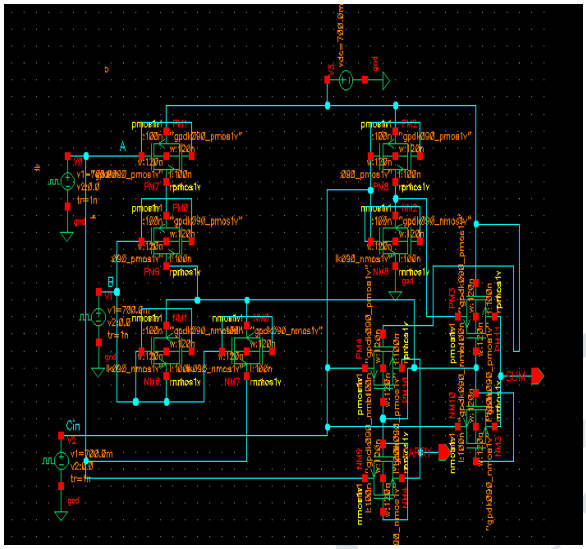

Fig. 5. Schematic of Diverse Full Adder using DG FINFET Technique

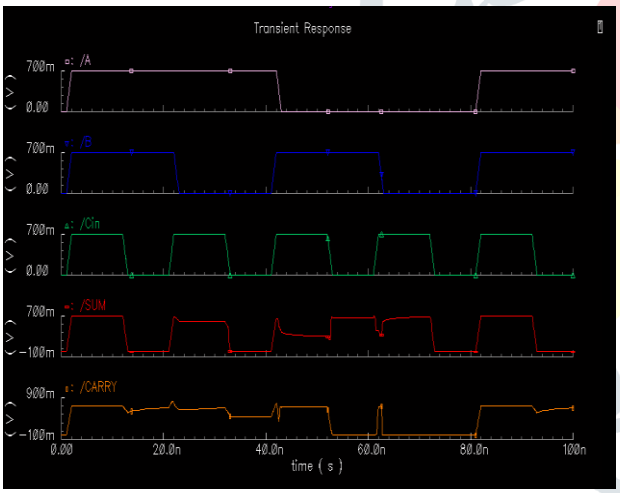

Fig. 6. Transient Response of Diverse Full Adder using DG FINFET Technique

D. Adiabatic Switching

Changing the topology of circuit as well as operating principles as situation calls for it is necessary in order to bring about an improvement in energy efficiency of logic circuits. The quantity of energy that can be recycled with adiabatic processes depends on switching speed, process technology, and voltage swing. Modifying the circuit to operate on ramping power-clock signals rather than a constant operating voltage or ground allows for signal energy recovery. The 1n1p-logic inverter illustrated in Fig.7, together with dual clock waveforms that it uses, demonstrates how energy may be fed into circuit and then recovered back to clock.

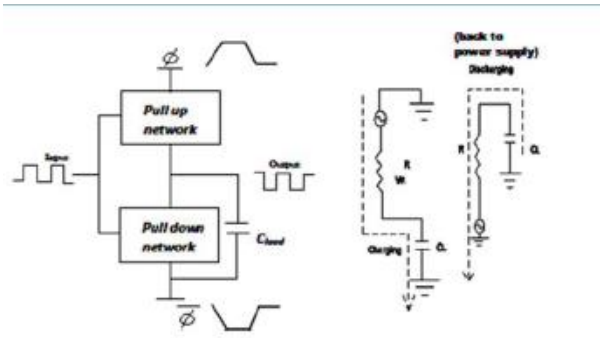

Fig. 7. shows the model of an adiabatic logic

Figure 7 depicts the schematic for adiabatic logic, which consists of a series-connected ideal switch, some form of resistance, and 2 voltage-counterpart clocks. In standard CMOS logic, the load capacitance is charged using a source that maintains a constant voltage; however, in adiabatic logic switching circuits, a source that maintains a constant current is employed in place of a source that maintains a constant voltage. Figure7.

III. Diverse Logic Design of Adiabatic Circuits

A. CECRL

Pairs of pull-down devices approximating the logic function make up the basis of an efficient charge recovery logic structure (NMOS). In addition, PMOS devices prevent CMOS ECRL from detecting power clock, which is used in quasi-adiabatic logic. CECRL uses a method in which pre-charge and evaluation are done at the same time. When the power clock goes from zero to VDD, the output of CECRL inverter stays at ground level. This is logic function of device. When the power clock reaches VDD, logic values for outputs 'out' & '/out' change to zero and VDD, respectively. These values will be carried on to next step of usage. If the power clock goes from VDD to zero, '/out' command will return its energy to power clock, which will then recover given charge.

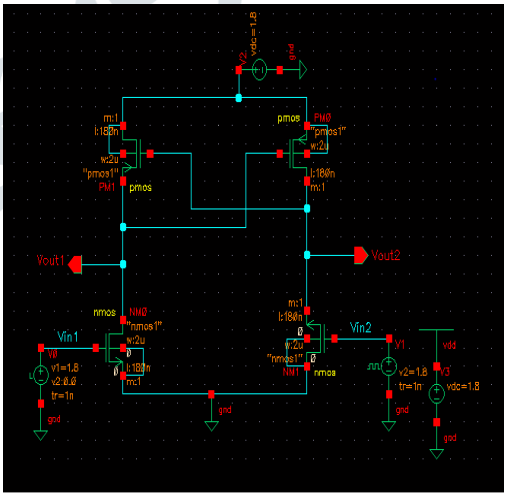

Fig. 8. CECRL adiabatic inverter

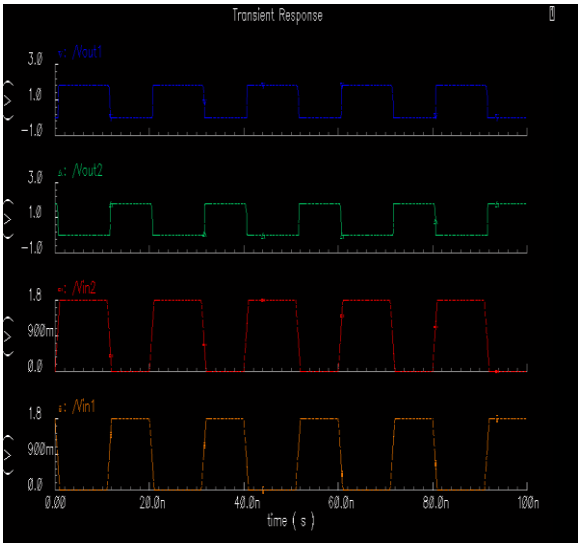

Fig. 9. Transient Response CECRL adiabatic inverter

B. *CPFAL*

In positive feedback adiabatic logic, logic level deterioration may be prevented by using a latch that was constructed with the assistance of 2 NMOS and 2 PMOS devices. In PFAL, much as in ECRL, logic function is determined by NMOS devices, however, these devices are coupled in parallel with PMOS devices. PFAL's benefits include transmission gate construction and generation of both negative as well as positive outputs at functional blocks.

The PFAL logic function is that output (out) remains at ground level and/or follows power clock when power clock grows from zero to VDD. Out and /out preserve logic values zero and VDD when power clock reaches VDD. These output values can be utilized in subsequent phases. When power clock goes below VDD, supplied charge is restored by the/out node feeding power back into power clock.

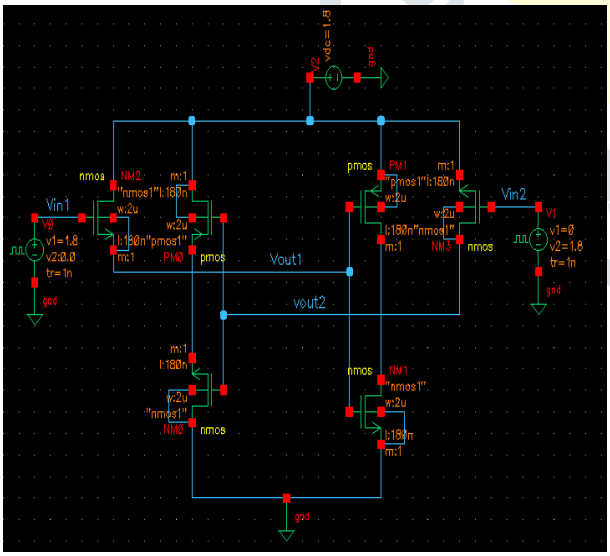

Fig. 10. CPFAL adiabatic inverter

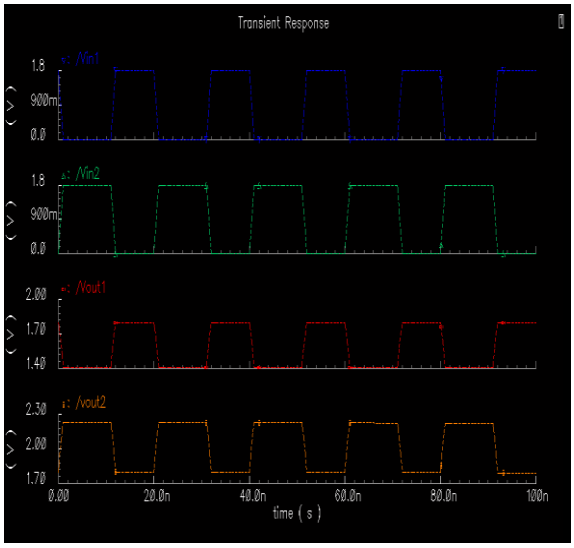

Fig. 11. Transient Response of CPFAL adiabatic inverter

IV. Diverse Full Adder with CECRL and CPFAL

A. *Diverse Full Adder with CECRL*

We required a four-transistor XNOR circuit and a two-to-one multiplexer for development of different, ten-transistor complete adder circuits. Pairs of NMOS pull-down devices are used to estimate logic function in effective charge-recovering logic structures; in contrast, PMOS devices prevent CMOS ECRL from picking up power clock, therefore the latter behaves as quasi-adiabatic logic. Diverse Full adder with CECRL employs a technology that simultaneously performs pre-charge and assessment. Figure 12 depicts a circuit diagram of a 10T diverse Full Adder Circuit utilizing CECRL components.

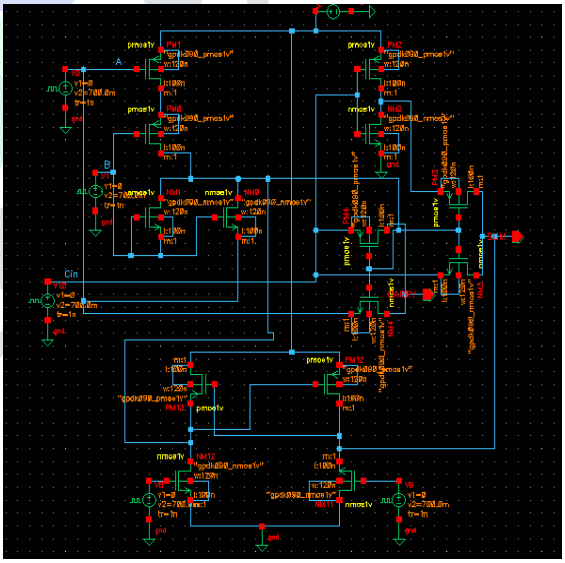

Fig. 12. Schematic of Diverse Full Adder with CECRL

B. *Diverse Full Adder with CPFAL*

This research presents the diversified full adder with 12 transistors using CPFAL. In positive feedback adiabatic logic, logic level deterioration is prevented by a latch constructed using 2 PMOS and 2 NMOS transistors. In a diversified full adder with PFAL, NMOS devices are responsible for determining logic function, much like they are in an ECRL, but they are coupled in parallel with PMOS devices. These values might be taken into consideration for subsequent stages. Figure.13 illustrates schematics of a 12T diversified Full Adder Circuit with CPFAL. This

is option that we selected and one that we took. It has also been contrasted to other circuits.

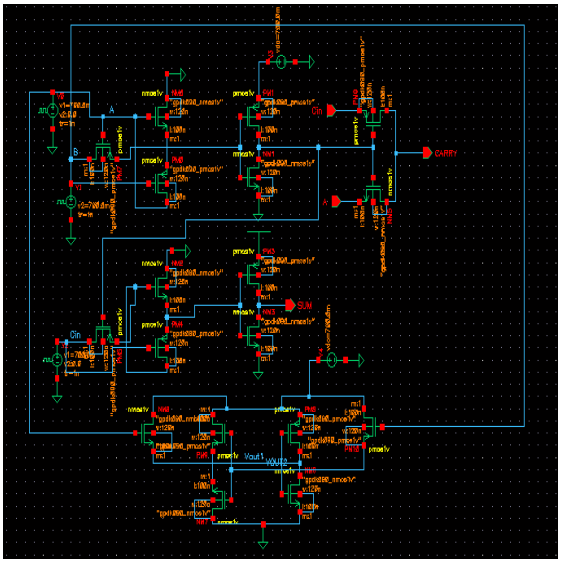

Fig. 13. Schematic of Diverse Full Adder with CPFAL

V. SOME EQUATIONS RELATED TO ADDER ARE:

A. *Sub-threshold Current*

Whenever the gate voltage is less than Vth, the transistor operates in a weak inversion zone, resulting in a drain-to-source current that is subthreshold. To calculate the MOSFET device's sub threshold leakage current, one uses the following formula:

$$I_{subthreshold} = I_0 e^{\frac{(Vgs-Vth)}{nV_T}} [1-e^{-(\frac{V_{ds}}{V_T})}]$$

Where

$$I_0 = \frac{W \mu_0 C_{OX} V_T^2 e^{1.8}}{L}, \quad V_T = \frac{KT}{q}$$

The voltages from drain to source and gate to source are represented by Vds and Vgs, respectively, while the thermal voltage is represented by VT. W and L refer to the width and length of the transistor that is now being employed. 0 represents the carrier mobility, Cox represents the capacitance of gate oxide, and n represents sub-threshold swing coefficient.

B. *Gate Oxide Tunneling Current*

Every new generation of technology necessitates a reduction in oxide thickness used to mitigate short channel effects. Aggressive scaling of oxide thickness, on other hand, results in generation of a large electric field, which in turn leads to a high amount of direct tunneling current through the transistor gate insulator. A substantial quantity of direct tunneling current passes through transistor gate insulator as a consequence of aggressive scaling of oxide thickness, on other hand, that generates a significant electric field.

Gate oxide tunneling current can be expressed as:

$$Igate = W.L.A(\frac{Vox}{Tox})^{2e} \frac{-B(1-(1-\frac{Vox}{Tox})^{\frac{3}{2}})}{\frac{Vox}{Tox}}$$

Where W and L represent the actual width and length of transistors being used.

Where

$$A = \frac{q^3}{16\pi^2 h \emptyset ox}$$

$$B = 4\pi\sqrt{2m_{ox}}\frac{\emptyset ox^{\frac{3}{2}}}{3hq}$$

mox represents the effective mass of tunneling particle, fox the height of tunnelling barrier, to the thickness of oxide, h the product of 1/2p and Planck's constant, and q the charge of an electron.

C. *Band-to-Band Tunneling Current*

The drain pn junction and source pn junction both connect to well regions in MOS transistor. The reverse biassing of these junctions results in a leakage current at pn junction. The junction's doped sites determine this current's

magnitude. Band-to-band tunnelling (BTBT) leakage predominates over reverse-biased junction leakage when both p and n regions are substantially doped. Electrons can tunnel from p-valence to n-conduction band in a reverse-biased pn junction when an electric field is applied. Tunneling current flows through a junction when the entire voltage drop across it, including applied reverse bias (Vapp) and built-in voltage (Ψbi), is greater than band gap. The density of tunneling current in a pn junction made of silicon is given by:

$$J_{BTBT} = A\frac{EV_{app}}{E_g^{\frac{1}{2}}} e^{(-B\frac{E_g^{\frac{3}{2}}}{E})}$$

$$A = \frac{\sqrt{2m^* q^3}}{4\pi^3 h^3}, \text{ and } B = \frac{4\sqrt{2m^*}}{3hq}$$

The effective electron mass is represented by symbol m*, while the energy band gap is represented by symbol Eg. The applied reverse bias is represented by the symbol Vapp, electric field at junction is marked by symbol E, the charge carried by an electron is represented by q, and the value of h is equal to 1/2p multiplied by Planck constant.

D. *Simulation Result*

Diversified Full Adder Circuit Simulations have been performed with the cadence tool with 90nm technology and a notional supply voltage of Vdd = 0.7 V. At room temperature of 27°C, gate leakage is only dominating mechanism, hence many strategies have been employed to reduce power consumption while retaining the performance of a 2:1 MUX with CECRL & CPFAL Circuit. In Table.1 below, we see how Diverse Full Adder compares to CECRL and CPFAL Circuits using DGFINFET approach for analyzing leakage current & leakage power.

TABLE I. SUMMARISES THE FINDINGS OF A COMPARATIVE ANALYSIS OF VARIOUS SINGLE-BIT, FULL-ADDER CIRCUITS. SIMULATED RESULT SUMMARY

Performance Parameter	Diverse Full adder Circuit	Diverse Full Adder with CECRL	Diverse Full Adder with CPFAL	Diverse Full Adder with DG FINFET
Technology Used	90nm	90nm	90nm	90nm
Supply Voltage	0.7V	0.7V	0.7V	0.7V
Leakage Power	20.4pW	8.4pW	2.3pW	1.3pW
Leakage Current	18.8pA	6.9pA	1.4pA	1.1pA

TABLE II. COMPARISON SHOWS PREVIOUS WORK

Circuits	Previous work [17]	Our Work
	130nm technology	90nm technology
	Power Dissipation	Power Dissipation
Conventional Full Adder	48.04pW	20.4pW
CPFAL with Diverse Full Adder	3.90pW	2.3pW

VI. CONCLUSION

In this work, DFA circuits have been suggested using XNOR Gate. The analysis and performance of the diverse full-adder diverse circuits are entirely influenced by performance of its basic segments. Several full adder designs, including CPFAL and CECRL circuits, have been suggested to decrease leakage current consumption and leakage power consumption. A variety of full adders, including CECRL & CPFAL designs, have been used to calculate circuit's leakage power consumption and leakage current consumption. The designed diverse full adder with CECRL and CPFAL circuits are contrasted in terms of leakage current & leakage power. We have designed and compared diverse full adders with DG FINFET, CECRL, and CPFAL in terms of power. It solves the problems with diving abilities that other full adders have, and it only needs 0.7V to run. The performance study of these DFA is contrasted to that of 90nm DGFINFET technology via simulations performed with the cadence tool in 90nm technology.

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