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Design and Implementation of High-performance Arithmetic and Logic Circuits based on FinFET 16nm Technology

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Abstract

Fin-type field-effect transistors (FinFETs) are promising substitutes for bulk CMOS at the nanoscale. FinFETs are double-gate and multi-gate devices. Double-gate (DG) and Multi-gate FinFETs has better Short Channnels Effects(SCEs) performance compared to the conventional CMOS and stimulates technology scaling. The two gates of a FinFET can either be shorted for higher performance or independently controlled for lower leakage or reduced transistor count. In this paper, we are designing 16nm DGFinFETs and extracting their transfer characteristics by using HSPICE simulation tool. By using this phenomenon logic circuits can be configured in one of the modes such as SG mode, LP mode, IG mode and IG/LP mode. NAND gate is designed in the above mentioned nodes and comparison has been drawn between them. Full Adder is implemented in CMOS with 32nm technology and FinFET with 16nm technology along with its working waveform and performance analysis. SPICE simulations are carried out for the design and results are analyzed.

Key Words: *Double-gate FinFET (DGFinFET), Multi-gate High-performance, Independent gate (IG) mode, Logic Gates, Low power (LP) mode, Short channel effects (SCEs),Full Adder.*

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1. INTRODUCTION

In the fabrication of MOSFET, the minimum channel length has been shrinking continuously. The motivation behind this decrease has been an increasing interest in high speed devices and in very large scale integrated circuits. The sustained scaling of conventional bulk device requires innovations to evade the barriers of fundamental physics compel the conventional MOSFET device structure. In the concern of battery-operated portable devices power consumption, chip

Density and operating frequency has increased because of advanced nanometer process technologies [1] - [3]. Even in the case of non-portable devices, power consumption is also very important because of the increased in packaging density and cooling costs as well as potential reliability problems. Thus, power efficiency has assumed increased importance, to meet the performance requirements within a power budget for VLSI [14] designers. Speed and area are also important parameters and proper tradeoff between them should be drawn while designing a circuit. FinFETs (fin-type field effect transistors)[4],offer interesting power-delay tradeoffs and better characteristics (short-channel-effects) in the nanometer regime in order to meet the performance expected by the ITRS (International Technology Roadmap for Semiconductor) for the forthcoming technological nodes [5]. The bulk architecture requires a high channel doping density in order to control the short channel effects, leading to large transversal electric fields and unacceptable abasement of the electron mobility.

Double-gate (DG) FinFETs are broadly classified into two types, there are concomitantly driven double-gate (SDDG) and independently driven double gate (IDDG)[6],[7] FinFETs. SDDG behaves like a three-terminal MOSFET because it has both the gates (front and back) connected each other, whereas the IDDG has two independent gates. SDDG FinFETs have a third gate on top of the gate, called trigate, however the top gate of IDDG FinFET is detached through a thicker oxide layer. IDDG FinFETs has the superiority in threshold-voltage (V) [8] and leakage-current control.

Due to non-planar structure, and the width quantization effect of FinFET devices still agonize from the issue such as process entanglement and additional parasitic capacitance, however it is promising candidate for the nanometer regime. Particularly in analog applications the width quantization effect [9] is important and also where the self-loading dominates. For instance, increasing the active width of the device increases the current and the load capacitance in the same ratio, thereby making the delay invariant. The channel width of the single fin device is restricted by the height of the fin HFIN .The channel width for a multi gate device is given by following [10]:

$$W \sim 2H_{FIN} + W_{FIN} \quad (1)$$

Where WFIN is the fin width. The device having HFIN = 60 nm and W FIN = 10 nm, the effective channel width can be

calculated [from (1)] as 130 nm. The technologies below 20-nm channel length, such a high channel width only increases the static and dynamic power dissipation (due to the higher currents) for a given value of delay.

This paper is well ordered as follows. Section 2 explains the double-gate (DG) FinFET devices structure realization and simulation setup. Designing of different FinFET based logic gates in SG, LP, IG and IG/LP modes are presented in section 3. Section 4 describes design and implementation of the full adder of cmos and FinFET bridge circuits. Section 5 describes the simulation results of arithmetic and logic circuits and finally Section 6 concludes the paper.

2. FINFET STRUCTURE

Fig 1 shows the basic structure of a FinFET and Fig 2 shows the views of the simulated FinFET. The device is formed on a thin silicon on insulator (SOI) finger termed fin. On the top of the silicon fin nitride has been deposited on a thin pad oxide to protect the silicon fin during gate poly-SiGe etching [11]. The gates are formed at the vertical sides of the fin using a thin gate oxide layer. Gate work-function tailoring is essential to adjust the threshold voltage. Therefore, for the gate material poly-SiGe has been chosen. The crucial geometric device dimensions are:

$L_{\mathbf{eff}}$: Effective gate length which is determined by th distance of the junctions.
$T_{\mathbf{fin}}$: Height of the fin.
Wfin: Width of the fin which is the distance between the gate oxides of the two gates.

The key feature in a FinFET is the formation of ultra-thin Silicon (Si) fins which forms the transistor channel to reduce the short channel effects. A FinFET can have multiple fins as per the process design. Multiple fins are usually used to achieve larger channel width [11]. The dimension of this non-planar device affects the performance in terms of power dissipation and delay.

Effective channel length Leff = Lgate + 2×Lext… .....(1)
Effective channel width W = Tfin + 2×Hfin .....(2)

Where H_{fin} and T_{fin} the fin height and thickness respectively, L_{gate} is length of the gate, L_{ext} is extended source or drain region as explained in Figure1. Fin width (T_{fin}) plays a major role for controlling the short channel effect effectively. Therefore $T_{fin} \sim L_{gate}/2$ is followed.

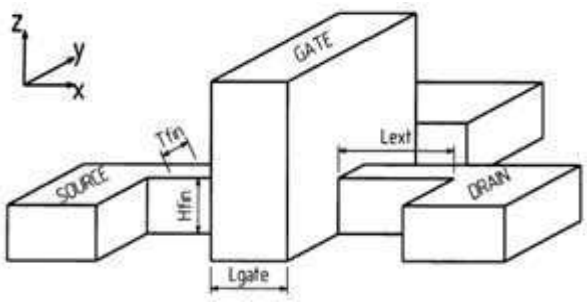

Fig 1: Schematic of a FinFET Structure

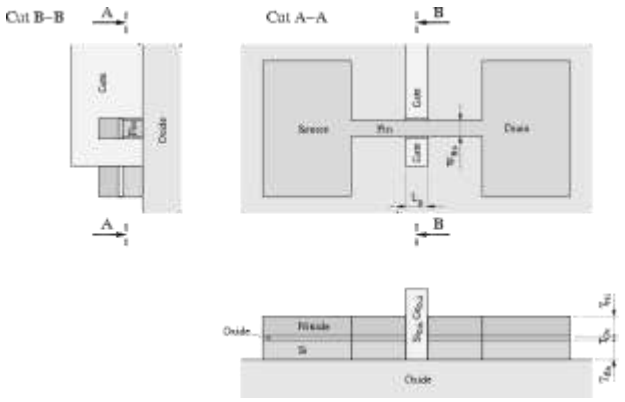

Fig 2: Views of the simulated FinFET

The geometrical channel width is given by for the one fin since both the channels have to be taken into account. To obtain the higher drive currents additional fins must be applied in parallel. Fig 3 shows a Structure of DG-FinFETs and MG-FinFETs. Thus, with this structure a three times higher drive current can be achieved. The gate comb is formed as a small vein which contacts the gates of all fins.

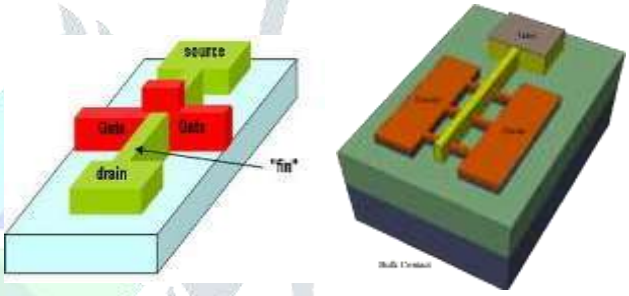

Fig 3: FinFET Structure

The basic electrical layout and the mode of operation of a FinFET doesn't differ from a traditional field effect transistor. There is one source and one drain contact as well as a gate to control the current flow.

In contrast to the planar MOSFETs the channel between source and drain is erect as a three dimensional bar on top of the silicon substrate, called fin. The gate electrode is then wrapped around the channel, so that there can be formed several gate electrodes on each side which leads to reduced leakage effects and an improve the drive current [11].The manufacture of a bulk silicon-based multi gate transistor with three gates (tri gate) is shown in fig 3.

Fig 4 and Fig 5 are simplified depictions of the planar FET and a FinFET respectively. In a planar FET a single gate controls the source-drain channel. Such that the gate does not have good electrostatic field control away from the surface of the channel next to the gate, resulting in leakage currents between source and drain even when the gate is off. By contrast, in the FinFET the transistor channel is a thin vertical fin with the gate fully "wrapped" around the channel formed between the source and the drain. The gate of the FinFET can be thought as a "multiple" gate surrounding

the thin channel. Such a multiple gate can fully deplete the channel of carriers. This results in much better electrostatic control for the channel and thus better electrical characteristics.

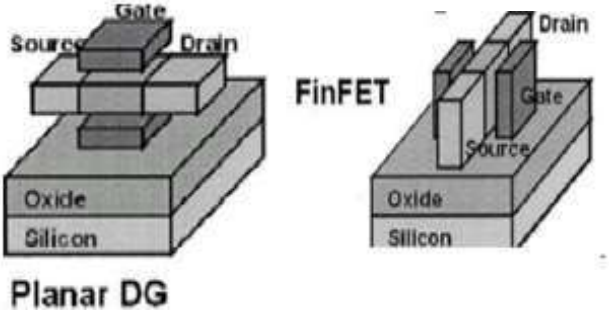

Fig 4 and Fig 5 Planar FET and FinFET

Fig 6 shows the most relevant geometric parameters of a FinFET are its height H, its width (body thickness) Tsi, and its channel length L.

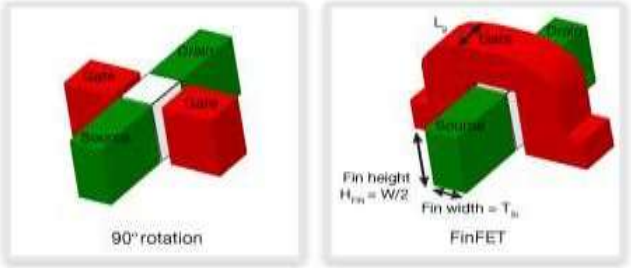

Fig 6: FinFET geometric parameters

The device structure is having two gates (front and back gates). The most common mode of operation of the double-gate(DG) FinFET is to switch the two gates concomitantly. The threshold voltage of the DGFinFET can be varied by applying the bias to any one of the gate terminal based on the application of our design.

3. MODES OF OPERATIONS OF FINFETs

Fig 7 shows the different modes FinFET based NAND gate designs and table 1 shows the truth table for the Nand gate operation.

A. Short Gate (SG) Mode:
In the short gate mode, the front gate and the back gate is shorted together which provides better driving strength. If one of the input voltages is unstable then either the front gate or the back gate will be able to control over the operation even when the other one is affected. This mode improves efficiency and can achieve low leakage [12].

B. Independent Gate (IG) Mode:
The pull up transistors is merged in independent gate mode. The front gate and the back gate are given two independent input voltages respectively. The number of transistors used is reduced, which increases the flexibility in circuit design. The delay is more when compared to ordinary CMOS.

C. Hybrid Gate (IG/LP) Mode**:**

In this hybrid mode, both IG and LP modes are used. Because of this combination, it has the advantageous properties of both the modes. Therefore making the mode more advantageous and efficient. The numbers of transistor used to make this hybrid mode circuit are less in number [12].

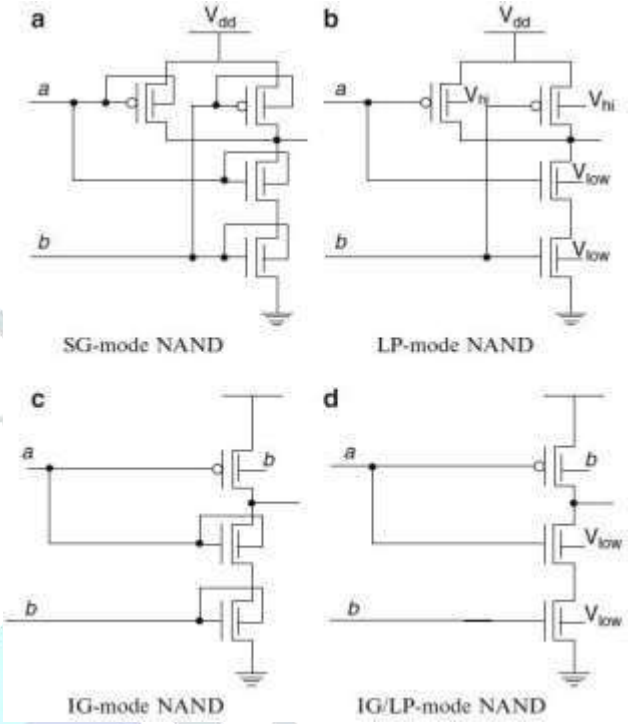

Fig 7: Different FinFET based NAND gate designs (a) SG-mode NAND (b) LP-mode NAND (c) IG-mode NAND (d) IG/LP-mode NAND

Table 1: Truth table for NAND

INPUT 1	INPUT 2	OUT
0	0	1
0	1	1
1	0	1
1	1	0

By using different FinFET methodologies we can design different logic gates. Logic gates can be configured in one of the following modes, (1) Shorted-gate (SG) mode of operation back gate is tied to front gate, in this case we get improved drive strength and have better control over the channel. (2) Independent-gate [9] [10] (IG) mode, in which independent signals drive the two device gates; back gate can have a different voltage from front gate. This may reduce the number of transistors in the circuit. (3) Low power (LP) mode [12], we are applying a low voltage to n-type FinFET and high voltage to p-type FinFET. This varies

the threshold voltage of the devices which reduces the leakage power dissipation at the cost of increased delay. A hybrid IG/LP-mode is a combination of LP and IG modes. The NAND gate circuits implementation of each of the above three modes is shown in Fig 7 and the truth table is shown in Table1. In shorted-gate (SG) mode NAND [shown in Fig 7(a) both p-type FinFET and n-type FinFET transistors back gates are connected to their front gates; this composition is best suitable for high-performance applications. Fig 7(b) shows the Low-power (LP) mode NAND gate; in which both p-type FinFET back gates are biased at high potential and n-type FinFET transistors back gates are biased at low potential. Fig 7(c) shows the IG-mode NAND gate; in which single p-type FinFET transistor has connected to two input signals (one input at the front gate and other at back gate) and the rest of the two n-type FinFET transistors connected in SG mode[12]. This design results in a diminution of one p-type FinFET and useful in area significant designs. At IG/LP mode NAND gate , single p-type FinFET transistor is connected to two input signals (one input at the front gate and other at back gate) and n-type FinFET transistors back gates are biased at low potential. This type of conformation is also ample in area efficient design.

4. FULL ADDER

The fig 8 shows a symmetric design which is called as CMOS-Bridge. This design generates Carry and Sum with 20 transistors, then use two inverters for enhancement of driving capability and produce Carry and Sum. The design uses 24 transistors. The output waveforms are following the truth table2 of full adder.

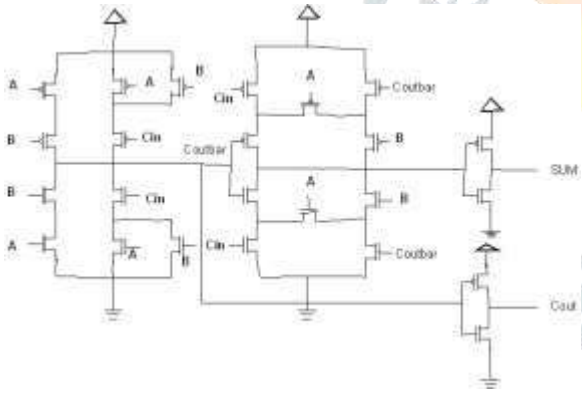

Fig 8: CMOS-Bridge Full Adder

The fig 9 shows a symmetric design Double-Gate Circuit which is called as FinFET-Bridge. This design generates Cout and Sum with 20 transistors, then use two inverters for the improve of driving capability and produce Carry and Sum. The design uses 24 transistors. Back gate is used to control the threshold voltage (V T) of the front gate, which is very important for the performance of the circuit. This is very much helpful in optimization of different circuits in terms of delay, area and power. In this paper we have designed FinFET Full Adder in SG-Mode to obtain a minimum delay.The waveforms are following the truth table 2 of full adder. Here the power dissipation of the circuit in FinFET is least and hence preferred over other CMOS models. The time taken is less which means the speed is also improved using FinFET.

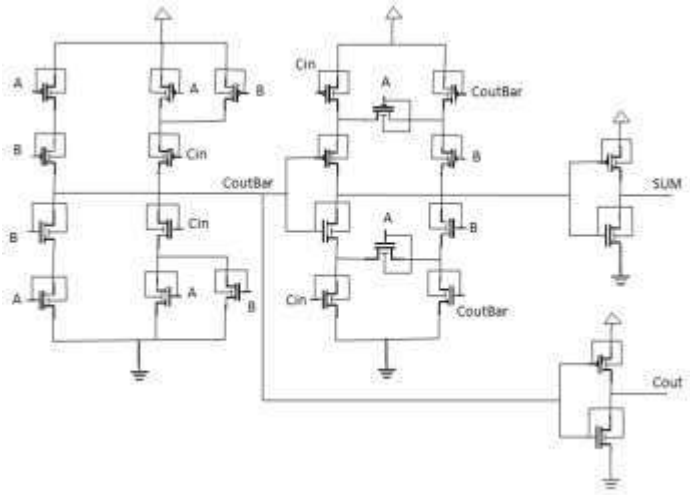

Fig 9: FinFET-Bridge Full Adder

Table 2: Full Adder Truth Table

Input bit for number A	Input bit for number B	Carry bit input Cin	Sum bit output S	Carry bit output Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

5. SIMULATION RESULTS AND DISCUSSION

The two input NAND logic gate using FinFET has been designed in various modes using Hspice simulation Tool by selecting 16nm technology. Power dissipation and delay for 16nm technology for different modes of operation of FinFET has been hereby discussed. Compare to the non-portable devices, the power consumption is very crucial because of the increasing cooling cost and packaging as well as reliability problems. To achieve performance requirements within a power budget was the aims of VLSI (very-large scale integration) designers.

Fig 10 shows the transient input/output characteristics of NAND gate FinFETs, there is no threshold voltage loss at the output. All design modes of gates are simulated with minimum size, The Delay measurement of FinFET based gates are calculated for each mode and the average delay and power dissipation is tabulated in Table 3.

The Simulation waveforms for full Adder using FinFET 16nm technology is shown in fig 11. The fig 12 and fig 13 shows the CMOS 32nm graph for different i/o bits of full adder versus the delay measurement. The fig 14 and fig 15 shows the FinFET 16nm graph for different i/o bits of full adder versus the delay measurement. The table 4 shows the power dissipation comparision between CMOS 32nm and FinFET 16nm technology.

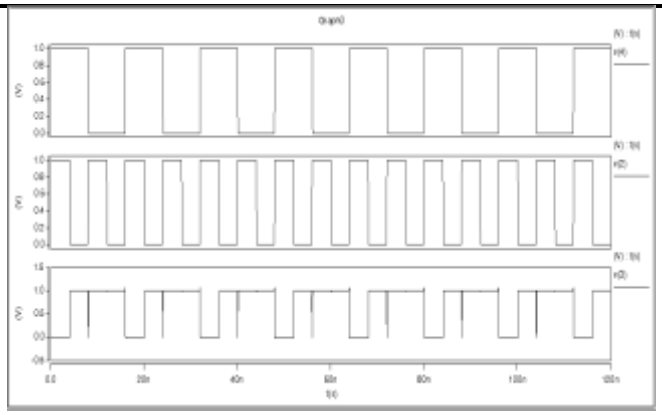

Fig 10: Transient input/output characteristics of NAND gate for FinFET 16nm of different mode using Hspice Simulator.

Table 3: Parameter measurement using FinFET 16nm technology

FinFET Modes of Operation	Delay(ns)	Total Power Dissipation
SG-Mode	3.859	467.0569fW
LP-Mode	3.850	901.3563fW
IG-Mode	3.865	58.7207pw
IG/LP Mode	3.862	59.1653pw

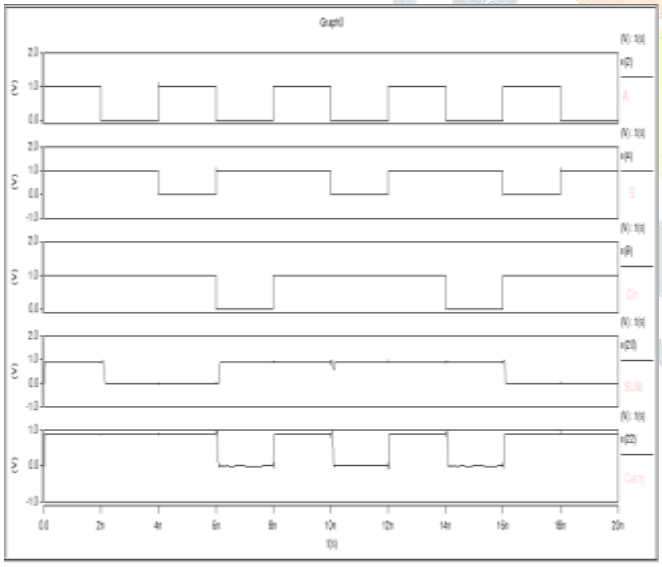

Fig 11: Full Adder using FINFET 16nm Technology

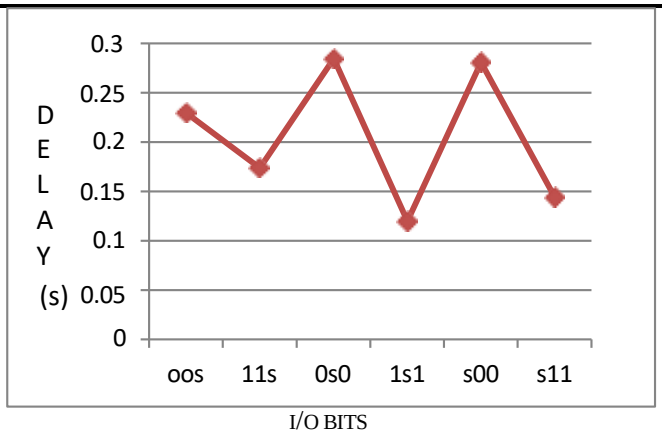

FIG 12: GRAPH FOR FULL ADDER I/O BITS VERSUS DELAY MEASUREMENT USING CMOS 32NM TECHNOLOGY

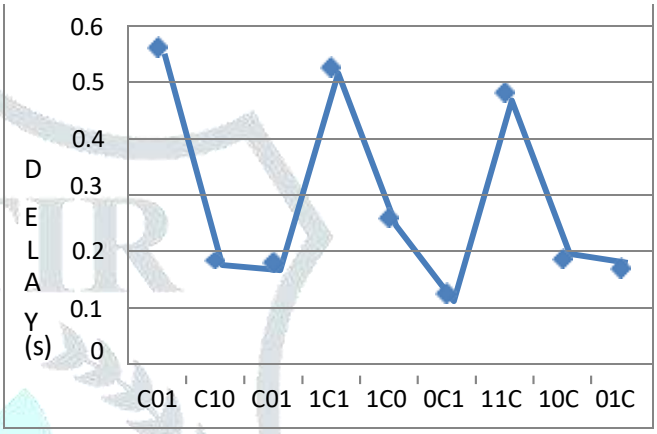

FIG 13: GRAPH FOR FULL ADDER I/O BITS VERSUS DELAY MEASUREMENT USING CMOS 32NM TECHNOLOGY

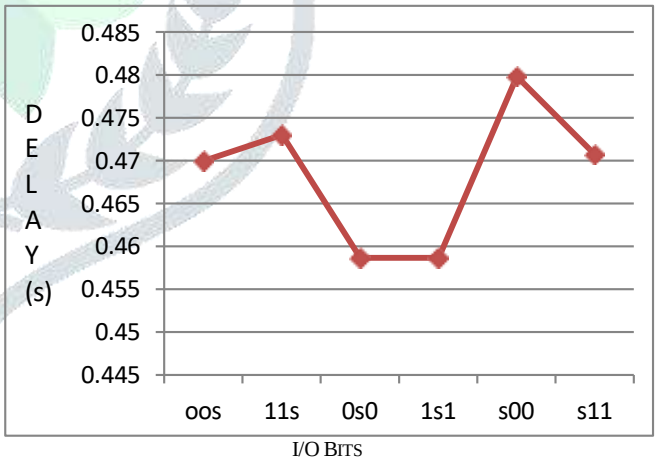

FIG 14: GRAPH FOR FULL ADDER I/O BITS VERSUS DELAY MEASUREMENT USING FINFET 16NM TECHNOLOGY

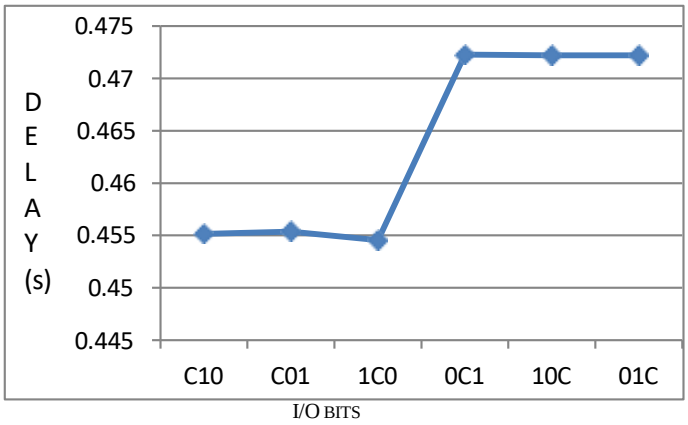

FIG 15: GRAPH FOR FULL ADDER I/O BITS VERSUS DELAY MEASUREMENT USING FINFET 16NM TECHNOLOGY

Table 4: Parameter measurements between CMOS 32nm and FinFET 16nm

ABC	POWER DISSIPATION(MICRO WATT) FOR CMOS 32nm	POWER DISSIPATION(PW) FOR FinFET 16nm
000	1.1012	11.0337
001	6.208	13.1109
010	6.481	12.0759
011	16.933	11.1652
100	7.0225	10.5927
101	15.4115	11.1273
110	14.9081	12.2739
111	23.396	7.8950

6. CONCLUSION

FinFET are the new challenge for the new material nowadays. This project is mainly focussed on the modelling FinFET using PTM card. The FinFET model has been developed by the following parameter from nanoscale design. A new generation of the Predictive Technology Model for Multi-gate (PTM-MG) devices has been developed for the early-stage design-technology exploration. The DG model of FinFET is successfully constructed and the performance of the device was being analysed. In this paper, FinFET device has been simulated using Hspice tool and its various transient characteristics are plotted. The simulation of different modes of NAND gates with 16nm FinFET shows that, we can get a minimum delay in SG mode, low power is obtained in LP configuration at the expense of increased delay while in the IG mode we can give inputs to the two different gates and the number of devices in a circuit can be reduced, while reducing the area requirement of the circuit. The IG / LP mode is a combination of the IG and LP modes and also results in a low leakage, reduced area and higher delay. Bridge-Full adder is designed in SG-Mode using FinFET 16nm technology which is shown in the above simulated waveforms & tables. By using FinFETs in VLSI circuits power dissipation can be reduced and speed can be improved. By using the FinFET 16nm technology, simulation results shows that the total power dissipation & delay are much better compared to 32nm CMOS model. Hence we can say that the use of FinFETs in VLSI circuits is vital.

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