JETIR.ORG ISSN: 2349-5162 | ESTD Year : 2014 | Monthly Issue
JOURNAL OF EMERGING TECHNOLOGIES AND INNOVATIVE RESEARCH (JETIR)
An International Scholarly Open Access, Peer-reviewed, Refereed Journal

FPGA IMPLEMENTATION OF DIGITAL MODULATION SCHEMES USING VERILOG HDL

Rashmi A
Department of electronics and communication Engg
EAST POINT college of Engineering and technology
Bangalore,India

Dr.Yogesh G S
Department of electronics and communication Engg
EAST POINT college of Engineering and technology
Bangalore,India

ABSTRACT
This paper describes the design and development of an FPGA-based digital Modulation Scheme for high-resolution Communication Application. We are focusing on implementation of Verilog based code simulation for fundamental and widely used digital modulation techniques such as Binary Amplitude-shift keying (BASK), Binary phase-shift keying (BPSK) In this work the idea of sinusoidal signals that have been generated is plain sailing in nature and based on fundamentals of signal sampling and quantization. Such concept of sinusoidal signals generation is not unfamiliar but somehow simplified using sampling and quantization in time and amplitude domain, respectively. The whole simulation is done on Modelsim and Xilinx-ISE using VERILOG Hardware descriptive language. The work has been accomplished on Thirty two bit serial data transmission with self-adjustable carrier frequency and bit duration length.

Keywords—Modulation schemes, FPGA.

I. INTRODUCTION

In general communication modulation is “the process of varying one or more properties of a periodic waveform i.e., the carrier-signal, for transmitting a modulating signal that contains information”. Modulation of a sine waveform is used to transform a baseband message signal into a pass band signal. A device that performs modulation is known as a modulator. A device that performs the inverse operation of modulation is known as a demodulator. A device that performs operations as modulator and demodulator is known as modem. The digital modulators major work is to transfer a digital bit stream over an analog band pass channel, for example over the wireless network, or over a limited radio frequency band. Digital modulation facilitate frequency division multiplexing (FDM), where several low pass information signals are transferred simultaneously over the same shared physical medium, using separate pass band channels (several different carrier frequencies). And the line coding, is to transfer a digital bit stream over a base band channel, typically a non-filtered copper wire such as a serial bus or a wired local area network as it is one of the aim of digital modulators.

The aim of digital modulation methods is to transfer a narrow band digital signal, in this scheme, as a bit stream over another digital transmission system. Despite simple transmitter and receiver architecture of Digital modulators and its modulation technique is still commonly used in wireless communication such as

WPAN (Wireless Personal Area Network). Amplitude shift keying (ASK) is data transfer technique with different amplitude of carrier frequency. As it is sensitive to propagate the channel variation, thus it is has been widely used in low- power wireless transceiver for system simplicity. For low power consumption, wireless communication systems exist in implantable medical devices, ingestible capsule endoscopy and multichannel neural recording. The ASK modulation/demodulation scheme, for both RF-band and baseband transceiver, was presented. This design is realized on future mobile memory I/O interface for energy efficient. However, is as well as showing better Bit. These digital modulation techniques were implemented on FPGA device. Simulation results consist of bit error rate of digital signals of modulators, source consumption of BASK, BFSK and QAM FPGA-based, bit rate of BPSK, BASK and on Xilinx ISE suite complier using verilog language. Thus digital modulators were implemented on FPGA. In addition to, bit error rate of BASK and modulation techniques was compared using Xilinx. In this paper, for and BASK modulation, FPGA based modulator is presented. Finally, simulation results are obtained.
Whereas BASK, BPSK, , are the permitted modulation schemes. Our work includes multimode inter leaver design with all possible modulation scheme permitted. The inter leaver comprises of two blocks: address generator and inter leaver memory. The former is FSM based and the later is implemented using internal memory of FPGA. The FSM based address generator operates at higher frequency and can provide better FPGA resource utilization. Use of internal memory always provides better results in terms of memory access time, power consumption and real estate occupancy of circuit board compared to external memory. Two approaches have been adopted to model the inter leaver memory: using dedicated internal memory and using distributed internal memory. Comparative analysis between the two techniques in terms FPGA resource utilization and maximum operating frequency shows that the former technique out performs the later

except the use of dedicated internal memory. The estimated power consumption of both techniques is equal and found to be 56mW. In addition our approach supports on the fly computation of inter leaver addresses. The Digital Signal Processing and the Channel Coding Stages where implemented within a FPGA (Spartan 3 line, from Xilinx) to take advantage of the massive parallel computation power of these devices and to have the possibility to scale up to ASIC devices.

II. RELATED WORK

This paper describes the design and development of an FPGA-based digital Modulation Scheme for high-resolution Communication Application [1]. The paper presents the comparison performance in terms of error performance between two modulation techniques, the BPSK and QPSK modulation. [2]. Field-programmable gate-array (FPGA) implementations of binary amplitude-shift keying (BASK), binary frequency-shift keying (BFSK), and binary phase-shift keying (BPSK) digital modulators are presented in this paper [3].This paper suggests the implementation of various modulation schemes using FPGA that can be ued in communication systems for lossless transmission of data[4].This paper suggests the vlsi implementation of Oqpask in biomedical devices [5].

III. PROPOSED SYSTEM

The proposed method produces the BASK/BFSK signal which is based on stored BASK/BFSK data in ROM. This method eliminates completely the DDS and multiplier blocks of the modulator. The modulator design has been made generic so that it can be used as either BASK or BPSK by use of single operational switch.

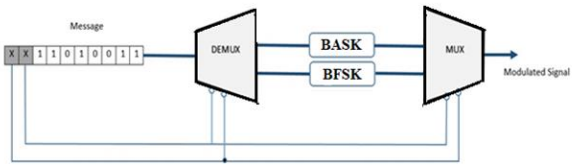

Fig1. Proposed block diagram

Here one 1:3 multiplexer and one 1:2demultiplexer is used .Here,there will be two modulation techniques, namely ASK and PSK. There will be 10 bits of message signal where first two bits comprises of selection line and rest of 8 bits will be treated as message signal.

Since selection line is of one bits, so there will be four combinations (2^1=2) in generel. Combinations are 0,1. Here this combination will be ignored because only three types of combinations of needed for three modulation techniques. So first combination will be ignored. The select line combination 0 will active the BASK module, 1 will active for BPSK module.

Now the above mentioned 1 bits will enter into the demultiplexer.0,1 bits will enter serially in the demultiplexer. Actually in this case serial communication system is used for data transmission. Now the modulation technique will be selected as per the select line bit will enter into the demultiplexer through meassage bits. Now for example if 0 select line is entered through the message bit in the demultiplexer, then BPSK module path will get activated, that means BPSK modulation technique will be selected Now whichever modulation technique will be selected from the above process for example either BPSK, BASK their modulated ouput bits will enter into the multiplexer. Here single output multiplexer is used. Now as the output we got the message bits which we had given as the input (8 bit). The final output will be in the form of modulated sinusoidal waveform according to the modulation scheme used.

IV. SOFTWARE DESCRIPTION

The simulation tool used for used in this system is Isim simulator Isim provides a complete, full featured HDL stimulator integrated within ISE. HDL simulation now can be an even more fundamental step within you are design flow with the tight integration of the Isim within thedesign environment.

The key features of Isim simulator are mixed language support, power analysis and optimization using SA IF, native support for all RIP blocks, memory editor for viewing and debugging memory elements, no special license requirement single click recompile and relaunch of simulation, integrated with IS design suite and plan ahead application multithread complete compilation, post processing capabilities, easy to use one click compilation and simulation.

The synthesis tool used is Xlinix ISE 14.7

Therearefour fundamental steps in all digital logicdesign.Theseconsist of:

1. Design – Theschematicor codethat describes the circuit.
2. Synthesis – Theintermediate conversion ofhuman readable circuit description to FPGA code(EDIF) format. It involves syntaxcheckingand combiningof all theseparatedesign files into asingle file.
3. Place&Route– Wherethelayout ofthe circuit is finalized. This is the translation oftheEDIFinto logicgates on theFPGA.
4. Program – TheFPGAis updated to reflect thedesign through theuseof programming (.bit) files.

The flow chart for gesture recognition is as shown below

V IMPLEMENTATION

The simulation results for BASK/BPSK modulation is shown below,.

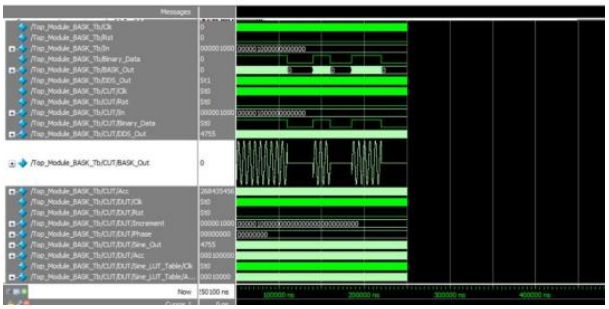

Fig 2. Simulation results

Fig 2. Shows Simulation result for BASK modulation.

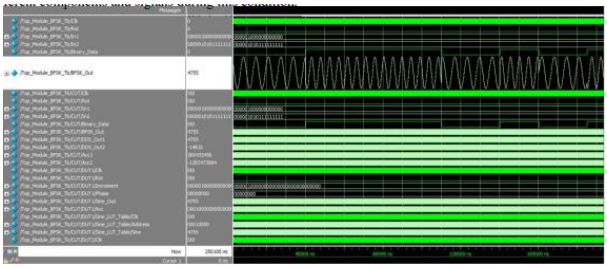

Fig 3.Simulation result for BPSK modulation

Fig 3. Shows the simulation result for BPSK modulation.

VII RESULTS

Table 1. Device utilization summary

Logic Utilization	**Used**	**Utilization**
Number of Slice Flip Flops	16	1%
Number of 4 input LUTs	32	1%
Logic Distribution		
Number of occupied Slices	16	1%
Number of Slices containing only related logic	16	107%
	0	0%

Table above indicates the device utilization summary.

VII CONCLUSION

The work can be concluding that the implemented four types of modulators in the Simulation environment like BASK, BPSK using system generator on FPGA. The will be like to extend my current work by implementing all modulation techniques thus whole digital laboratory can be done on a single kit. FPGA implementations of BASK, BPSK digital modulators could be demonstrated. The main advantage of the implementations is the minimum numbers of digital blocks used for performing digital modulations, the ability to integrate with modules in FPGA boards, and the user controllability of the input signal's frequencies. The implemented FPGA designs are suitable for realization of the digital baseband-modulation part of software-defined radio systems. In addition, usage of this kind of implementation for educational purposes in digital communications laboratories or courses clearly emphasizes the correlation between different courses in electronics engineering. BASK, BPSK system (modulation) is designed using Verilog HDL and implemented on Spartan-3 FPGA kit.

VIII REFERENCES

[1] F. Quadri and A. D. Tete, "Fpga implementation of digital modulation techniques," in Communications and Signal Processing (ICCSP), 2013 International Conference on. IEEE, 2013, pp. 913–917. [2] E. A. Lee and D. G. Messerschmitt, Digital com

[2] S.O.POPESCU, A.S. GONTEAN, "Performance comparison of the BPSK and QPSK Modulation Techniques on FPGA", IEEE 17th International Symposium for Design and Technology in Electronic Packaging (SIITME), 2011.

[3] C. Erdoğan, I. Myderrizi, and S. Minaei, "FPGA Implementation of BASK-BFSK-BPSK Digital Modulators," IEEE Antennas and Propagation Magazine, Vol. 54, No. 2, April 2012.

[4] Thotamsetty M Prasad, and Syed Jahingir, "Simulation and implementation of a BPSK modulator on FPGA," International Conference on Electronics and Communication Engineering (ICECE), 16th Sept, 2012, Pune- ISBN: 978-93-82208-18-1.

[5] Anitha and R. Kanchana, "VLSI Implementation of Oqpsk for Biomedical Devices Applications," International Journal of Technology and Engineering System (IJTES), Jan- March 2011, Vol 2, .No1.