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A Low Area and High Speed VLSI Architecture of the Wavelet Filter for Image Denoising

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Abstract : Image and video signals are corrupted by impulse noise during acquisition or transmission. This paper presents a VLSI architecture for efficient wavelet filter implementation tailored to image denoising applications. The proposed architecture achieves a balance between low chip area and high processing speed, addressing the inherent trade-offs in VLSI design. Leveraging the wavelet transform's multi-scale analysis, the architecture employs innovative techniques to enhance denoising performance while maintaining real-time processing capabilities. Simulation is performed using MATLAB and VLSI –Xilinx 14.7 software. The image process to be visualizes using the MATLAB software and the filter architecture to be optimized using the Xilinx.

Index Terms **– Wavelet, MATLAB, Image, Denoising, VLSI, Filter, Noise, FPGA.**

I. INTRODUCTION

Digital image interpolation or scaling is an issue that has recently received great attention. Image scaling is a process of resizing a digital image, and it is a nontrivial process that involves a tradeoff between efficiency, smoothness, and sharpness. Nowadays, the image scalar is widely adopted in portable healthcare devices, digital electronic equipment, digital camera, digital photo frame, mobile phone, touch panel computers, etc [1]. It has become a significant trend to design a low-cost, high-quality, and high-performance image scalar by the VLSI technique for multimedia products. As the graphic and video applications of mobile handset devices grow up, the demand and significance of image scaling are more and more outstanding. The image scaling algorithms based on interpolation are basically of two types: linear and nonlinear interpolation methods[2].

The simplest linear interpolation method is a nearest neighbour algorithm which is a low-complexity algorithm, but it results in scaled images with blocking and aliasing artifacts. The most widely used scaling method is bilinear interpolation algorithm by which the target pixel can be obtained by using the linear interpolation model in both horizontal and vertical directions. Another popular polynomial-based method is bicubic interpolation algorithm, which uses an extended cubic model to acquire the target pixel by a 2D regular grid. The nonlinear interpolation methods such as weighted median interpolation, curvature interpolation, bilateral filter, and autoregressive model greatly improve image quality by reducing blocking, aliasing, and blurring effects compared to linear methods [3][4].

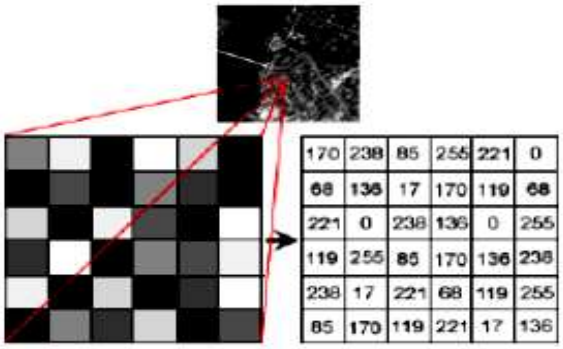

Figure 1: Digital Image

Image analysis is concerned with making quantitative measurements from an image to produce a description of it. In the simplest form, this task could be reading a label on a grocery item, sorting different parts on an assembly line, or measuring the size and orientation of blood cells in a medical image. More advanced image analysis systems measure quantitative information and use it to make a sophisticated decision, such as controlling the arm of a robot to move an object after identifying it or navigating an aircraft with the aid of images acquired along its trajectory.

The 2D continuous image f(x,y) is divided into N rows and M columns. The intersection of a row and a column is called as pixel. The value assigned to the integer coordinates [m,n] with {m=0,1, 2,...,M-1} and {n=0,1,2,...,N-1} is f[m,n]. In fact, in most cases f(x,y)—which we might consider to be the physical signal that impinges on the face of a sensor. Typically an image file such

as BMP, JPEG, TIFF etc., has some header and picture information. A header usually includes details like format identifier (typically first information), resolution, number of bits/pixel, compression type, etc.

II. PROPOSED METHODOLOGY

The goal of proposed work is to present VLSI based filter for the image denoising.

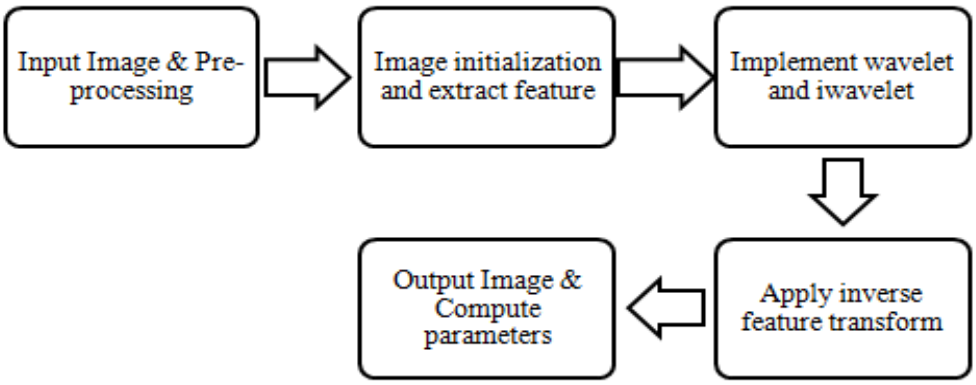

Figure 2: Flow Chart

Digital VLSI architectures employing parallel channels are proposed, physically realized and tested. The multi-encoded AI framework allows a multiplication-free and computationally accurate architecture. A multiplier-less architecture based on algebraic integer representation for computing the Daubechies 6-tap wavelet transform for 1-D/2-D signal processing is proposed. This architecture improves on previous designs in a sense that it minimizes the number of parallel 2-input adder circuits compare to existing system. The proposed method is to find the algebraic integer values for the filter bank process and to optimize the circuit complexity, and to improve the system performance. This type of architecture is to reduce the adder count in overall filter architecture, and to modify the reconstruction step and to enhance the filter image. The proposed to increase the system speed due to the filter and transformed process and this process to implement the image compression process.

The proposed work is Daubechies 6-tap wavelet technique used for the wavelet transform. Orthogonal filter banks give perfect reconstruction filter banks for any number of channels. Orthogonal filter banks are also called paraunitary filter banks. This Daubechies 6-tap wavelet transform used to reduce the adder counter for the filter architecture. And reduce the path delay also. We propose an efficient image denoisng compression technique that addresses the problem occurred in above discussed existing image compression technique.

Our proposed approach exploits the use of orthogonal filter to efficiently reconstruct the image from the original image. The working procedure of this proposed scheme is halved into following process namely, selection of input image (Original image), and acquisition of binary points, apply Feature transform to obtain the Feature points, Encode the orthogonal filter using DWT computation, Decode the Feature points using inverse DWT, image reconstruction through inverse Feature transform.

This work presented an efficient architecture for the implementation of a delayed wavelet filter. For achieving lower adaptation delay and area delay power efficient implementation, we use a novel partial product generator and propose a strategy for optimized balanced pipelining across the time consuming combinational blocks of the structure.

The proposed system is to improve image filtering process. And the compression result quality to be high. The proposed daub-6 wavelet transform have less multiply operator and reduce the adder circuit complexity. The proposed system reduces the hardware complexity. The path delay is to be low and the area to be optimized. The design approach of the proposed framework to minimize the adaptation delay in the error-calculation block. A bit level pruning of the adder tree is also prospective to reduce the hardware intricacy without noticeable deterioration of steady state MSE. Variation delay of N cycles for filter length N, which is quite high for great order filters. The proposed scheme could achieve less area and more power reduction correlated with by removing redundant pipeline latches. To increase the PSNR value for the image filtering process and reduce the mse value also. The image quality to be high compares to the existing architecture and reduces the filtering time.

III. SIMULATION AND RESULT

The simulation is performed using MATLAB and Xilinx software.

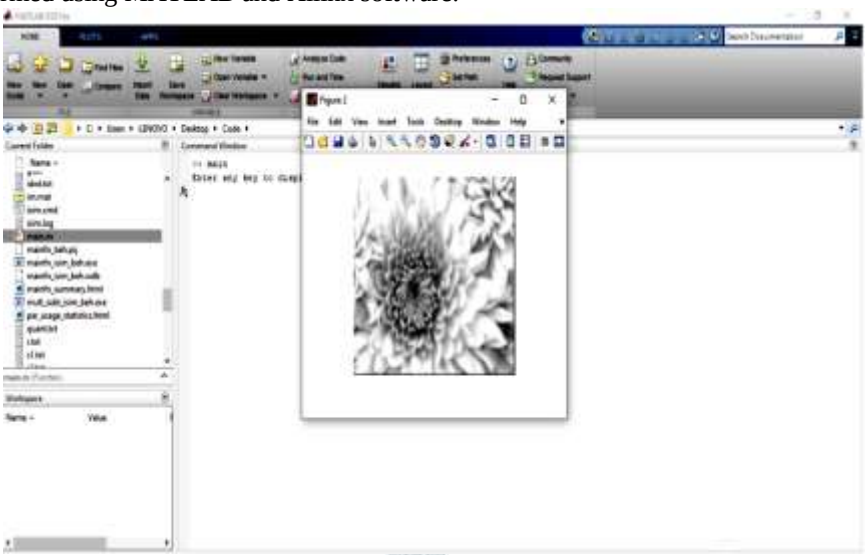

Figure 3: Extract Feature points

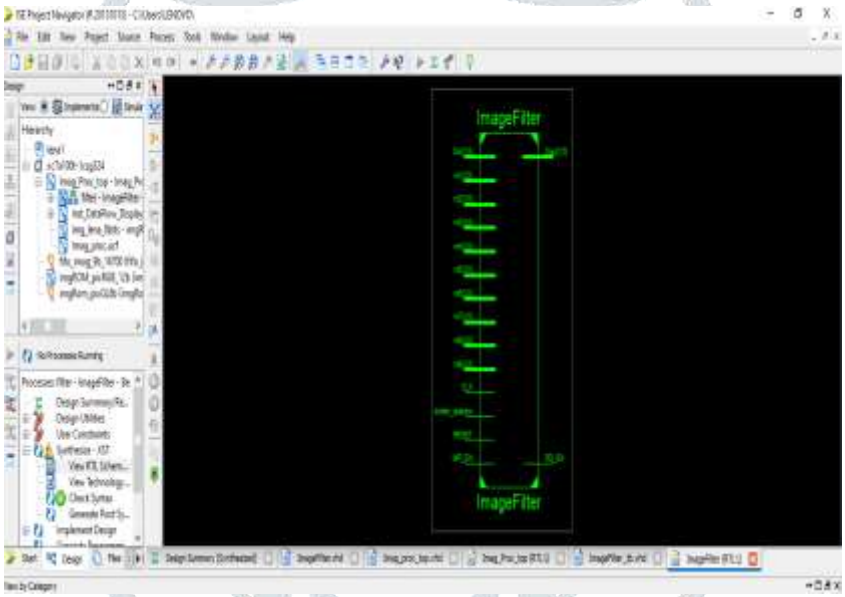

Figure 4: Top module of filter in xilinx environment

Figure 4 is showing the top module of the filter design, where see the various input and output combinations.

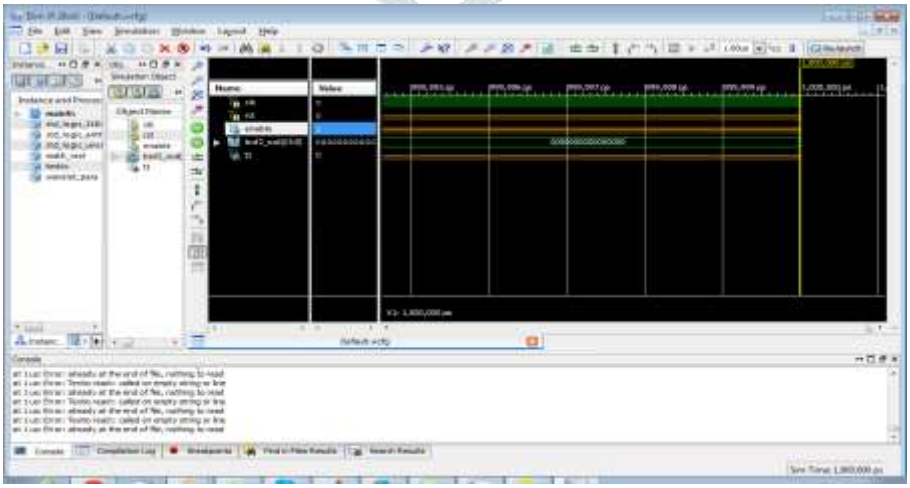

Figure 5: Assign clock and reset

Figure 5 shows the clock and reset pulse, the clock pulse and reset is set at 1 to trigger.

Table 1: Result Comparison

Sr No.	Parameter	Previous Work [1]	Proposed Work
1	Filter Type	Bilateral Filter	Wavelet Filter
2	Delay	NA	0.897 ns
3	Frequency	236.697 MHz	1114 MHz
4	Slice look up table	5142	418
5	Fully used look up-flip flop pair	1782	254
6	Bounded I/O boxes	69	57
7	Number of DSP48E1s	36	8
8	Throughput	59171103 pixels/sec	89120000 pixels/sec

Table 1 is showing comparison of proposed work with previous work, so it can be seen that proposed work gives better result than existing work.

IV. CONCLUSION

Image denoising is the technique of removing noise or distortions from an image. The filter architecture is to optimization for improvement in the filtering performance level; reduce the delay level compare to the proposed methodology and to reduce the power consumption also. The filter architecture requires less time due to the image filtering process. The frequency achieved by the proposed filter is 1114 MHz while previous it is 236.697 MHz. The slice look up table is using 418, fully used look up-flip flop pair 254, Bounded I/O boxes 57 and number of DSP48E1s is 8. The overall throughput achieved by the existing work is 89120000 pixels/sec, while previous it is 59171103 pixels/sec.

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